R&D Status and Key Technical and Implementation Challenges for EUV HVM

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Intel Corporation

Agenda

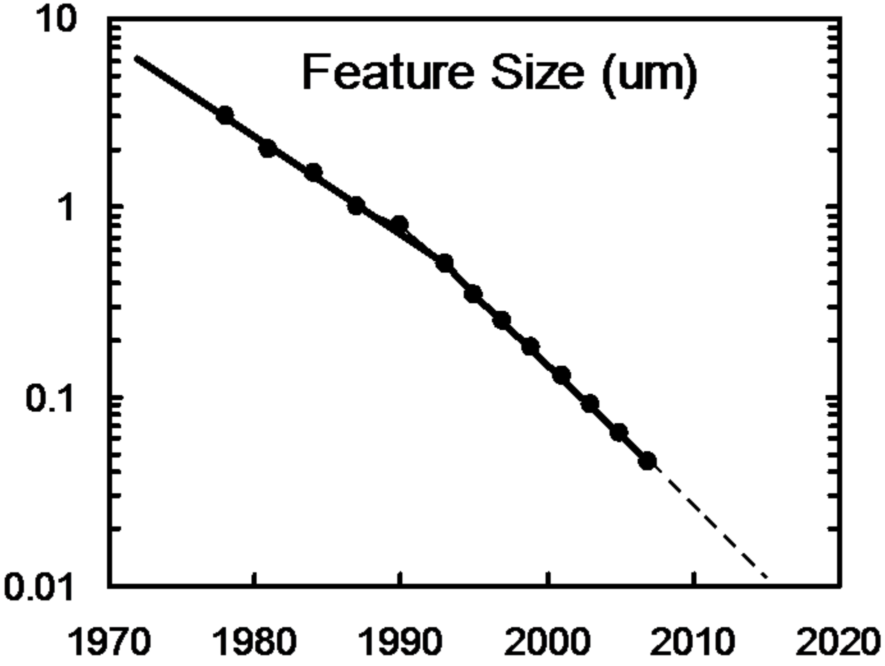
Requirements by Process Node

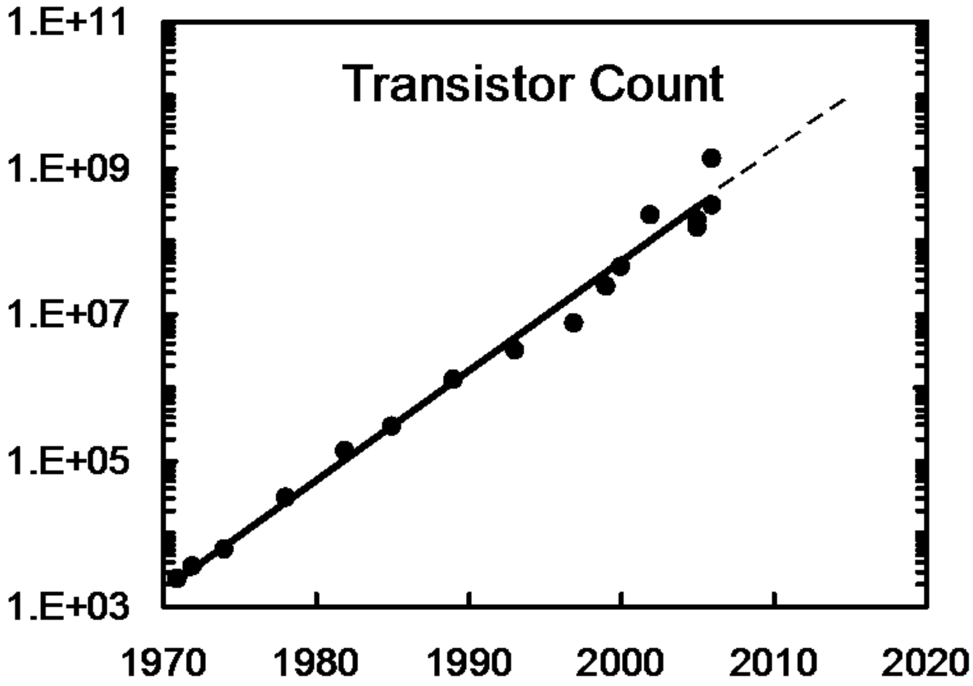
EUV Technology Status and Gaps

- Photoresists
- Tools
- Reticles

Summary

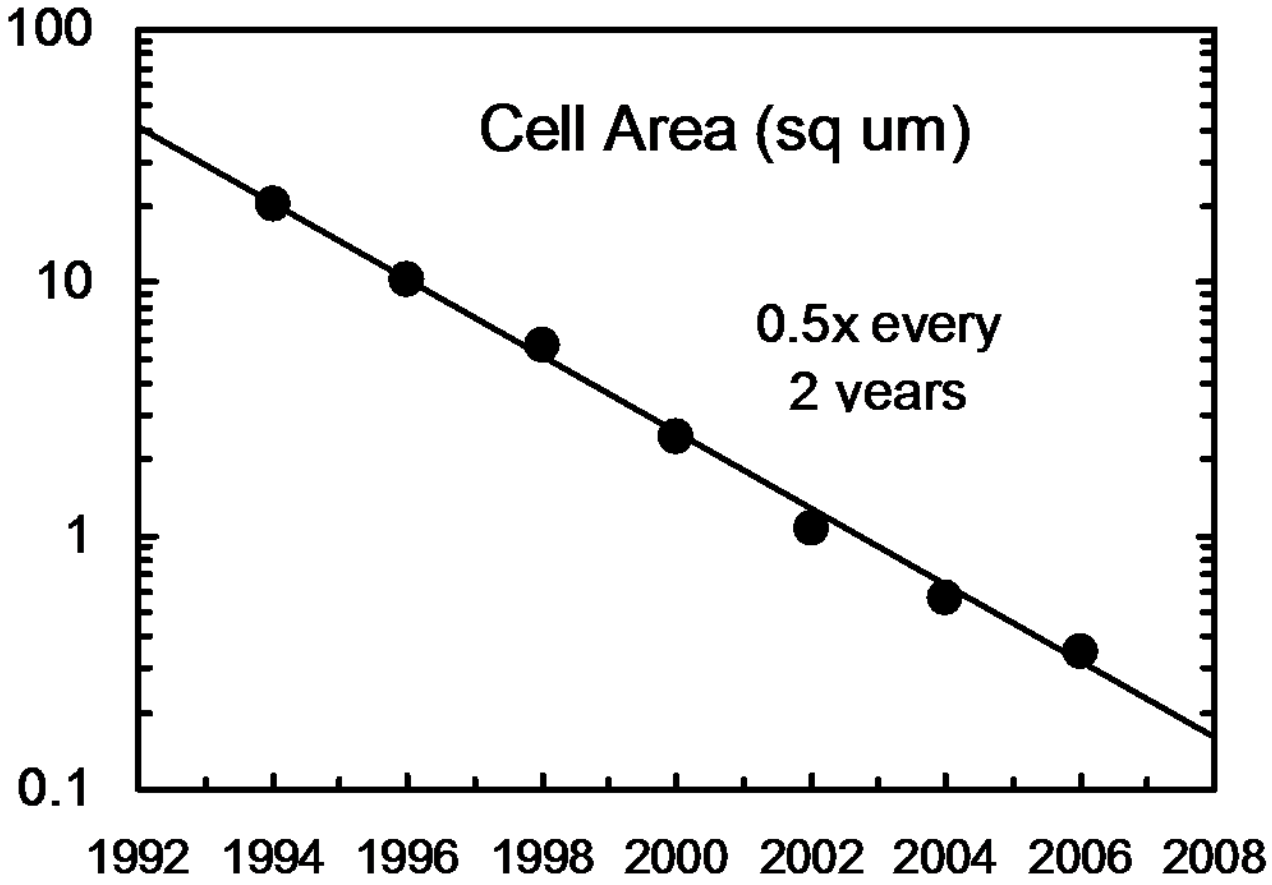
Moore’s Law at Intel





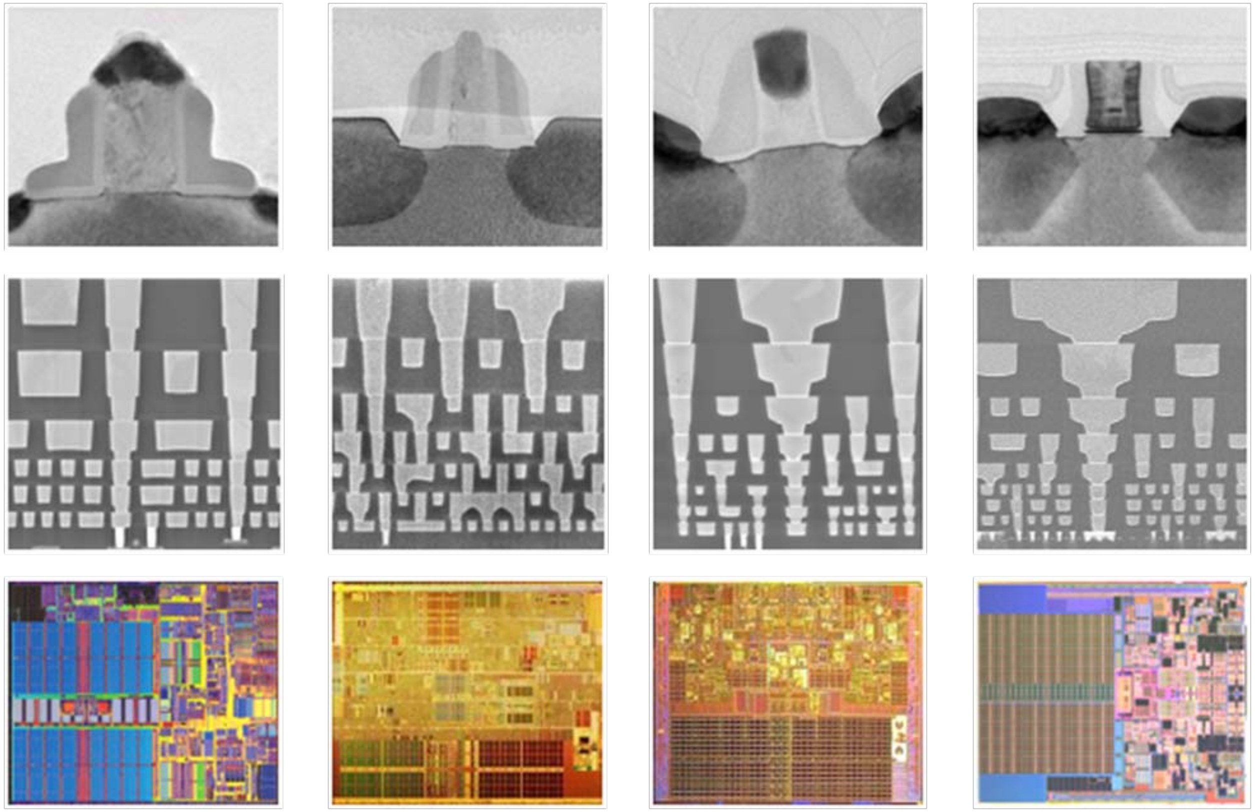
The trend is expected to continue

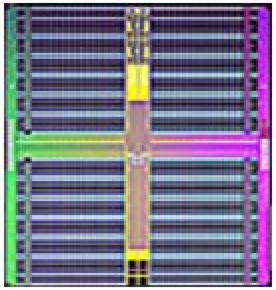
Transistor Density Trend



On-Time 2 Year Cycle

130 nm	90 nm	65 nm	45 nm	32 nm	22 nm
2001	2003	2005	2007	2009 forecast	2011 forecast





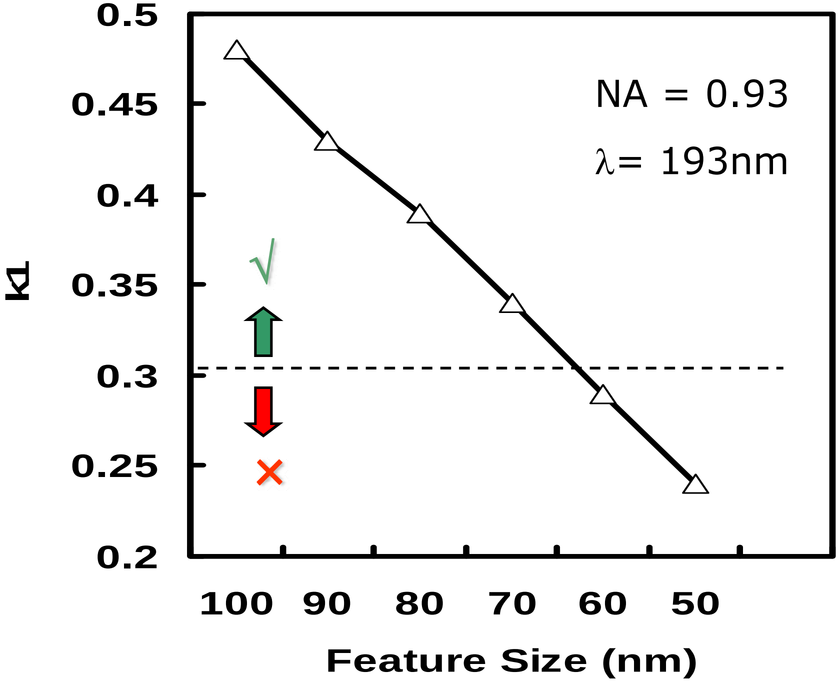
291 Mb
SRAM

2^{ND} gen.
HK+MG

In
Development

Paths to Feature Size Scaling

$$d = k_1 \frac{\lambda}{NA}$$



Increase NA

Enable reduced pitches through process options (like double patterning)

Reduce Wavelength

k_1 < 0.3 tends to have manufacturability issues

Lithography Transitions

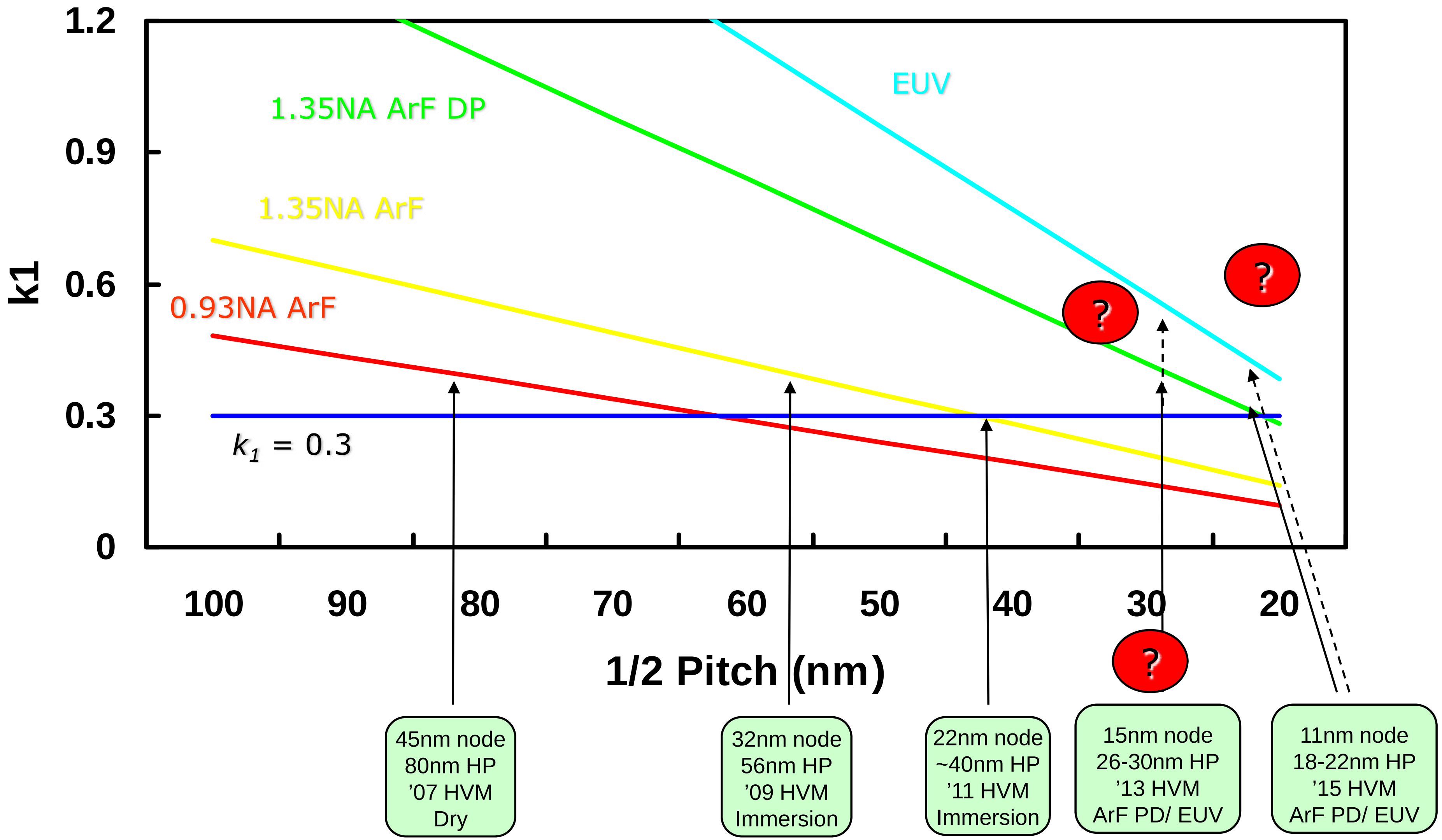
If current lithography is capable of delivering a manufacturable process, use it

If not:

- If new lithography technology is ready, manufacturable and cost-effective, use it (increase NA, reduce λ)
- If not:
  - need to make alternative decisions to enable scaling without litho improvements (operate more effectively at lower k_1)

Managing litho transitions is key! Requires significant planning

ArF Pitch Division vs. EUV



45nm node
80nm HP
’07 HVM
Dry

32nm node
56nm HP
’09 HVM
Immersion

22nm node
~40nm HP
’11 HVM
Immersion

15nm node
26-30nm HP
’13 HVM
ArF PD/ EUV

11nm node
18-22nm HP
’15 HVM
ArF PD/ EUV

Patterning Choices for 15nm and 11nm

ArF Pitch Division

Advantages:

- Known technology
- Well-established infrastructure
- Mature photoresist and tooling

Disadvantages:

- Complex process flow
- Very expensive
- Complicated DRs

EUV

Advantages:

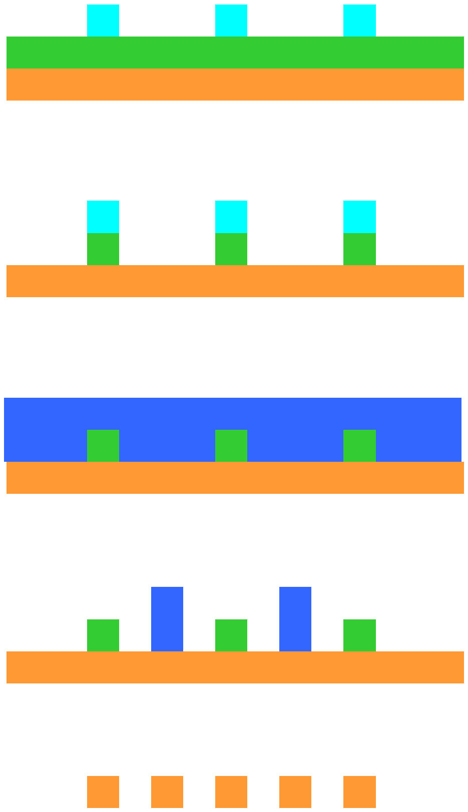
- Single exposure
- Simpler DRs

Disadvantages:

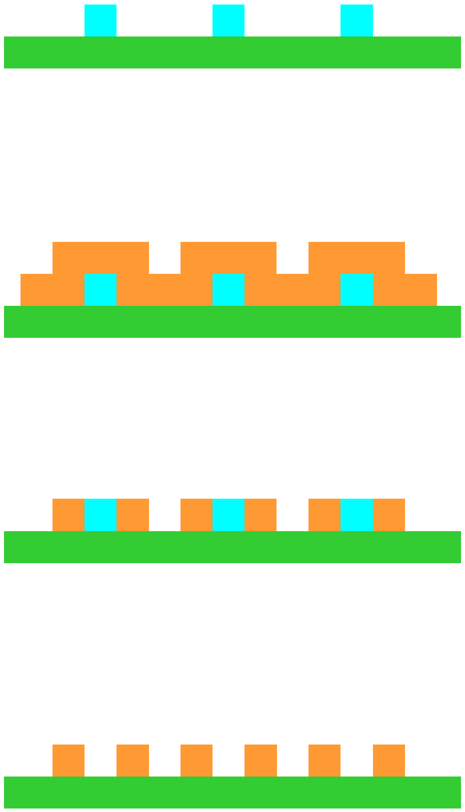
- Unknown technology
- Infrastructure needs to be developed
- Immature photoresist, tooling

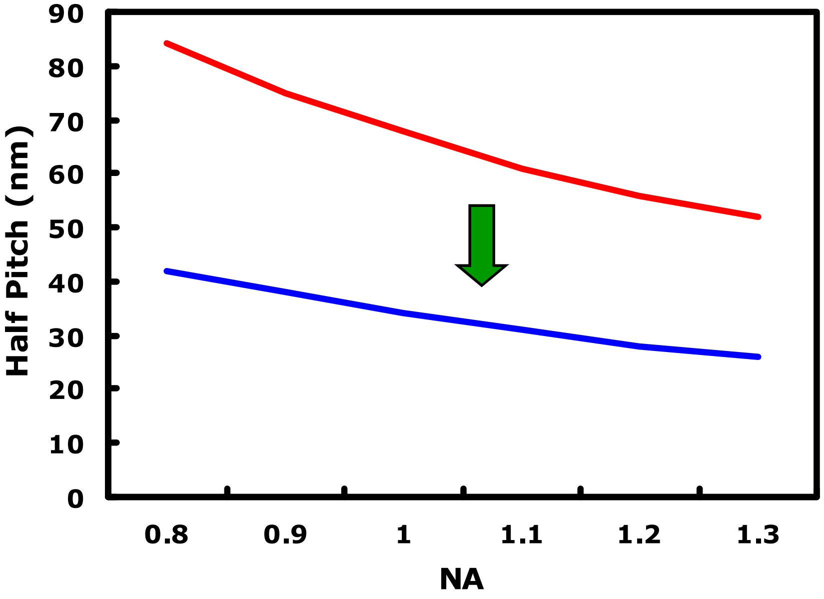
ArF Pitch Division

**Double Patterning
Pitch Division (DPPD)**



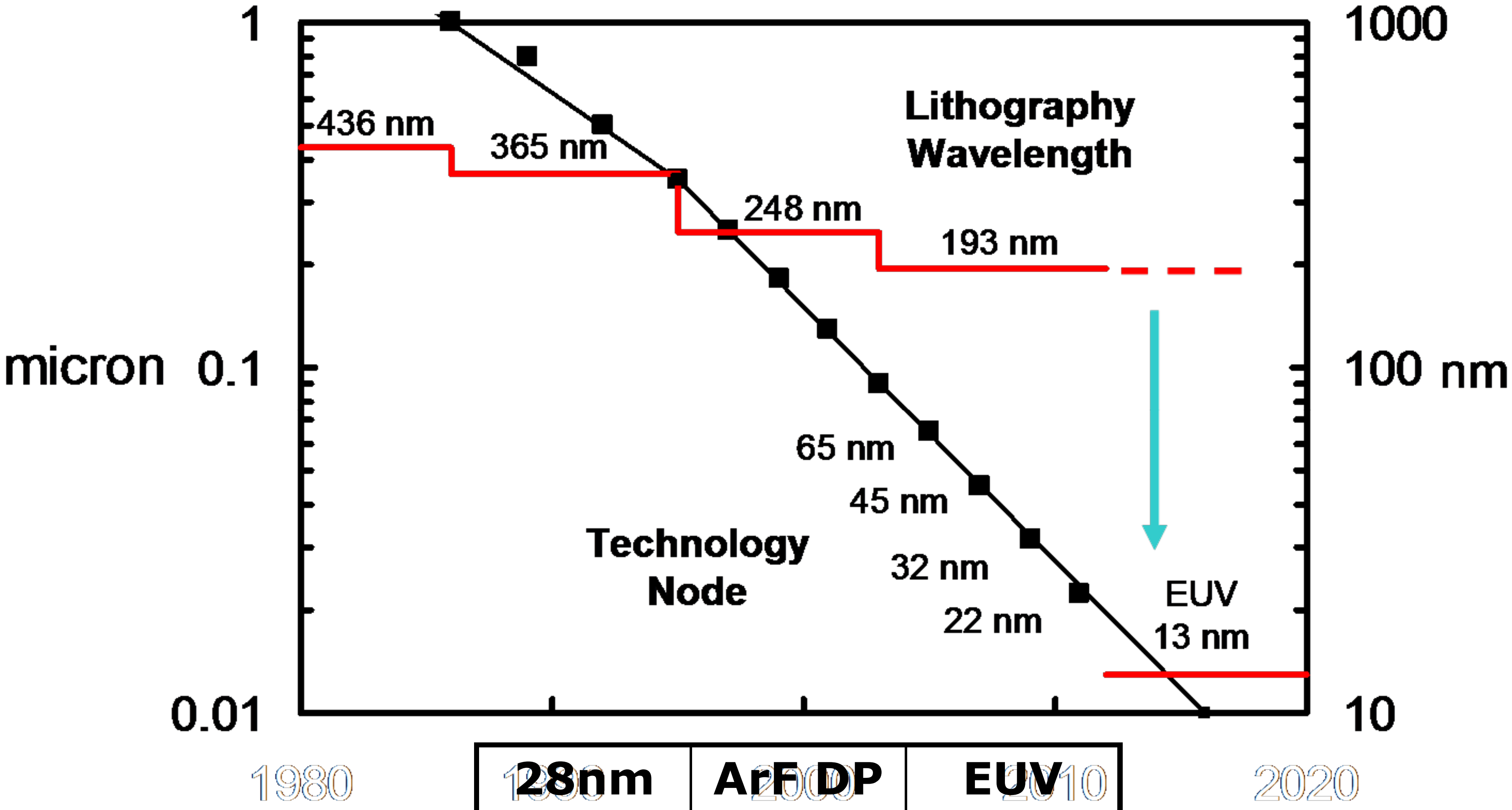
**Spacer Based
Pitch Division (SBPD)**





ArF PD gains significant resolution at the expense of process complexity

λ Scaling – The Case for EUV



28nm HP k_1	ArF DP	EUV
	0.39	0.54

EUV HVM – Key Requirements

Stable hardware
- Scanner platform
  - Optics
  - Overlay/stage
  - System (vacuum)
- Source
  - Reliability and uptime
  - Power

Photoresist that meets requirements
- Resolution, sensitivity, LWR
- Etch interactions

Reticles
  - Defectivity
  - Infrastructure (cleans, inspections, handling)

Success of EUV in HVM will depend on progress on all these fronts

Exposure Tooling

EUV Exposure Tooling

External

- **Nikon EUV1 alpha tool**
  - 0.25NA full field scanner
  - Currently installed at Nikon and SELETE

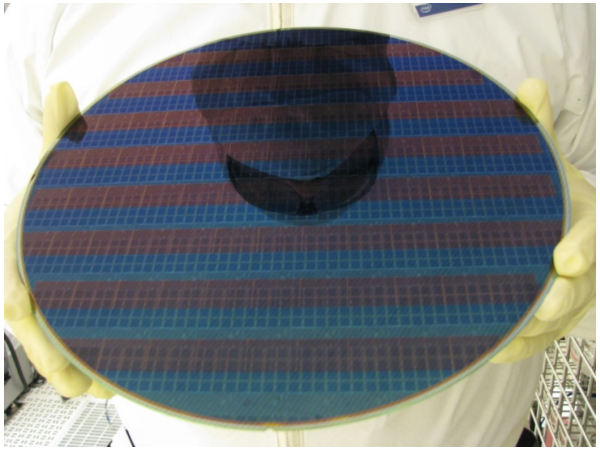
- **ASML Alpha Demo Tool (ADT)**
  - 0.25NA full field scanner
  - Currently installed at IMEC and SEMATECH

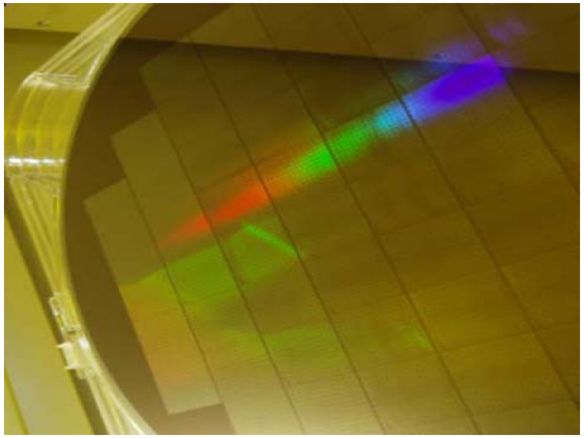
Intel Internal

- MET small-field exposure tool
- Target application is resist development

EUV HVM Exposure Tooling Development

ASML ADT printed wafer

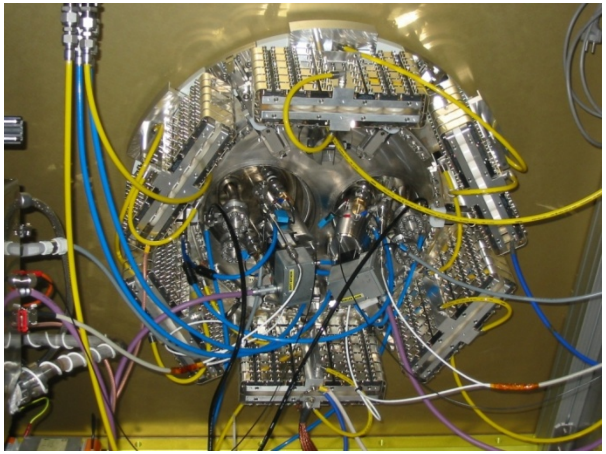




Nikon EUV1 printed wafer

EUV Source Suppliers are competing towards HVM tool development

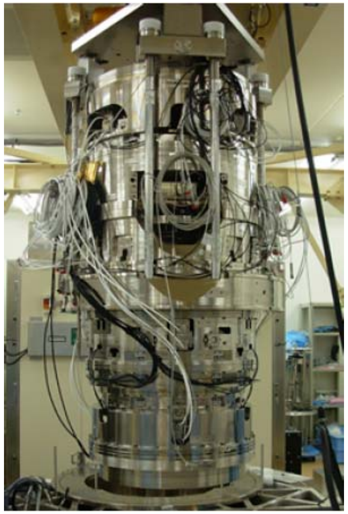
Cymer beta source

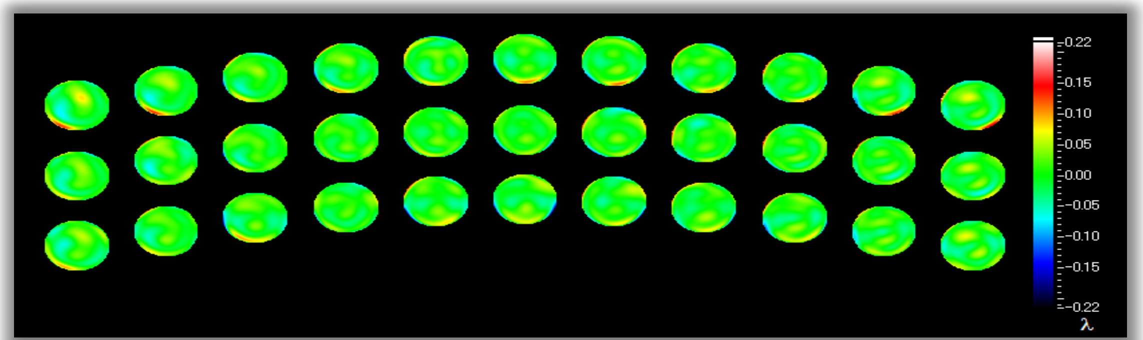


Philips beta source

Nikon EUV1 Tool

Field Size	26 x 33 mm^2
NA and Magnification	0.25, x1/4
Illumination Sigma	Adjustable
Overlay	10 nm



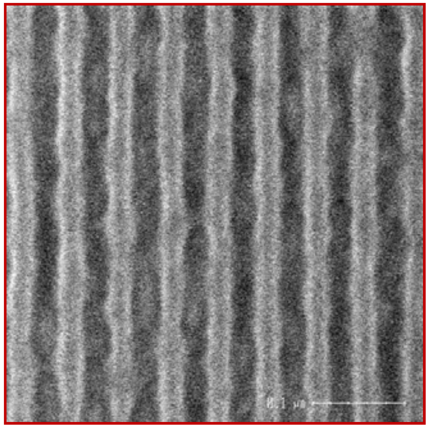


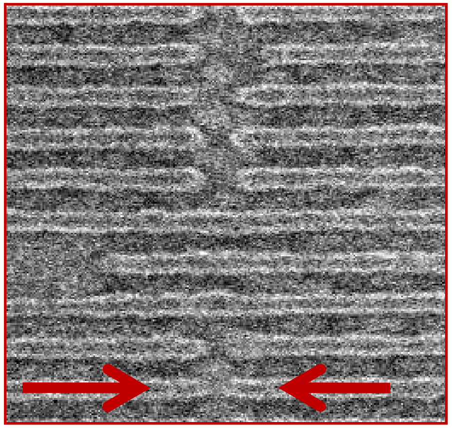
WFE 0.4 nm RMS (average)

Min. 0.3nm RMS ~ Max. 0.5nm RMS

Nikon EUV Tool Data – Lines (Static)

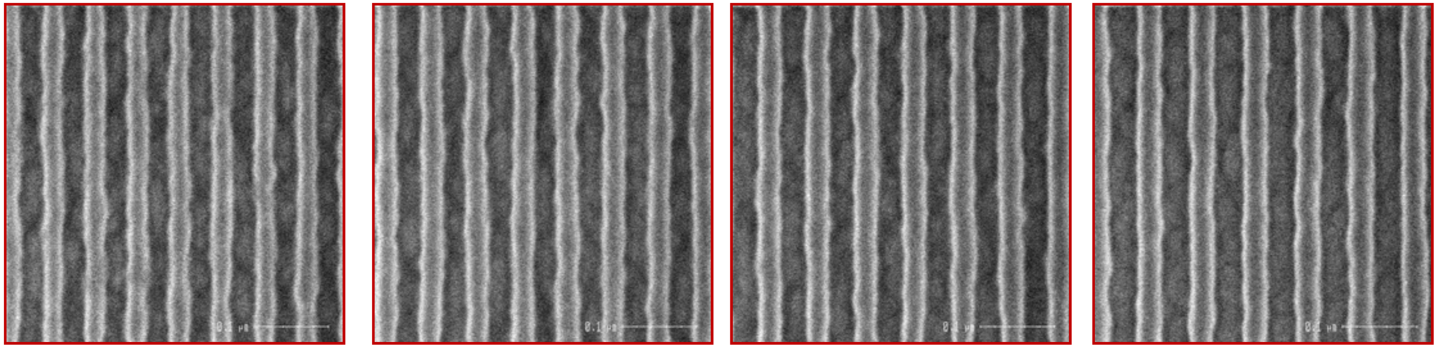
Ultimate Resolution
26nm HP
LWR
7.05nm
Esize
17.8mJ/cm^2





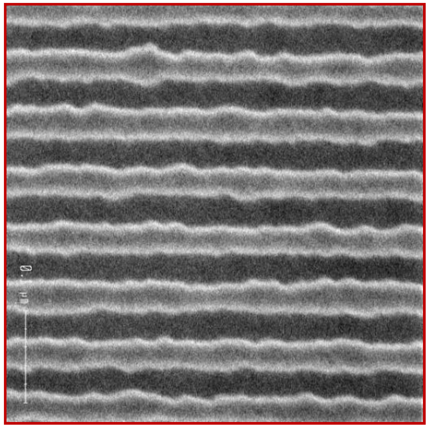
32/64nm
Line Ends

Vertical lines through HP at best dose/focus
$\sigma = 0.5$

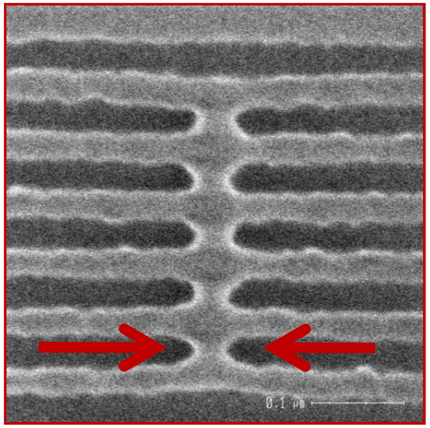


HP (nm)	28	30	32	35
LWR (nm)	5.33	5.25	4.56	4.52
DOF (nm)	140	>210	>210	>280

Nikon EUV Tool Data – Trenches (Static)

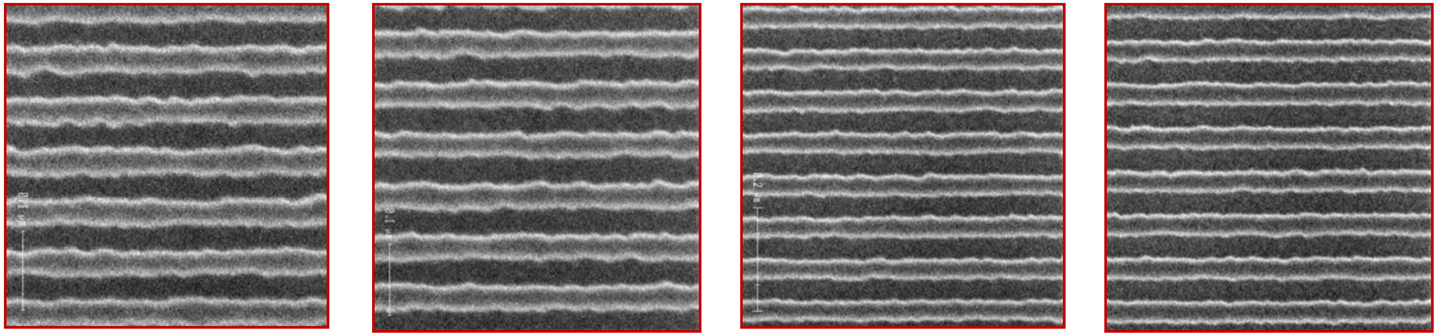


Ultimate Resolution
31nm HP
LWR
7.22nm
Esize
16.2mJ/cm^2



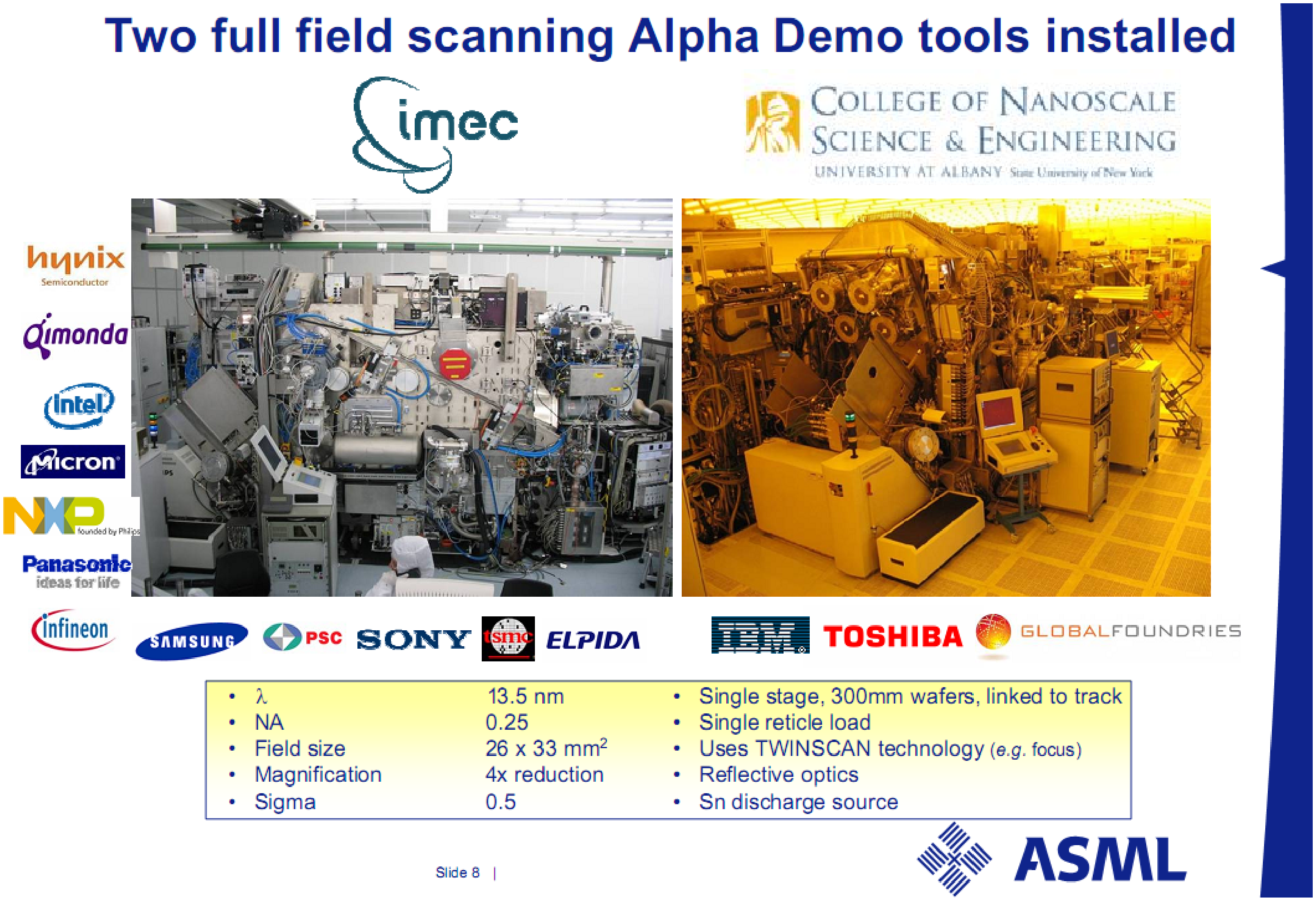
32/64nm
Line End Trench

Horizontal
trenches
Through HP at
best dose/focus
σ=0.5



HP (nm)	32	35	40	45
LWR (nm)	6.46	5.98	5.58	5.63
DOF (nm)	>100	>140	>160	>180

ASML Alpha Demo Tool (ADT)



Two full field scanning Alpha Demo tools installed

imec

COLLEGE OF NANOSCALE SCIENCE & ENGINEERING
UNIVERSITY AT ALBANY State University of New York

hynix Semiconductor
qimonda
intel
Micron
NXP founded by Philips
Panasonic ideas for life
infineon
SAMSUNG
PSC
SONY
tsmc
ELPIDA

IBM
TOSHIBA
GLOBALFOUNDRIES

λ	13.5 nm
NA	0.25
Field size	26 x 33 mm^2
Magnification	4x reduction
Sigma	0.5

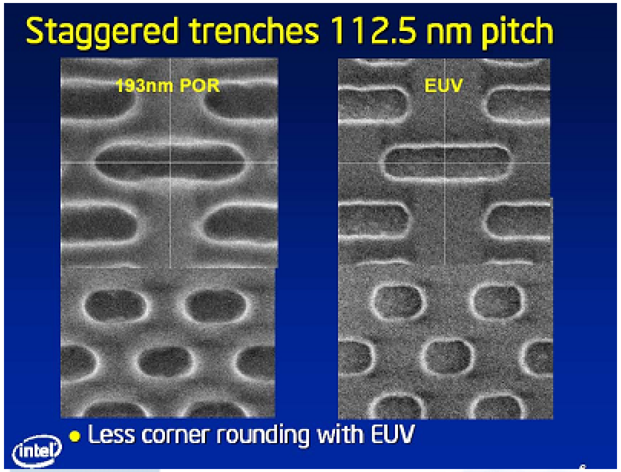
- Single stage, 300mm wafers, linked to track
- Single reticle load
- Uses TWINSCAN technology (*e.g.* focus)
- Reflective optics
- Sn discharge source

Slide 8 |

ASML

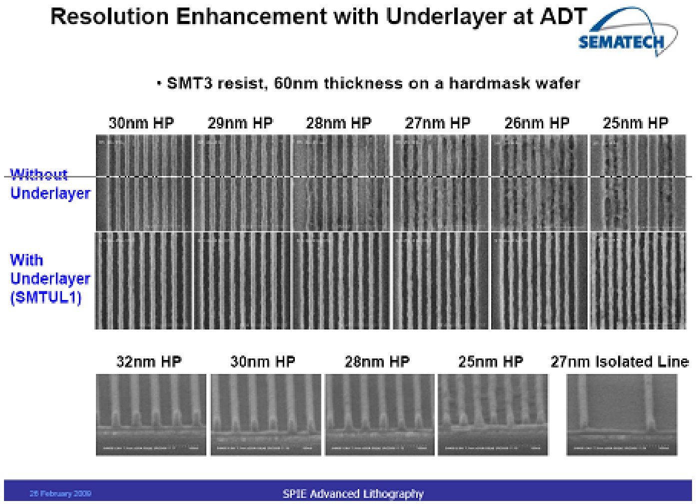
ADT Patterning Results

25 nm HP resolved; imaging results from ADT



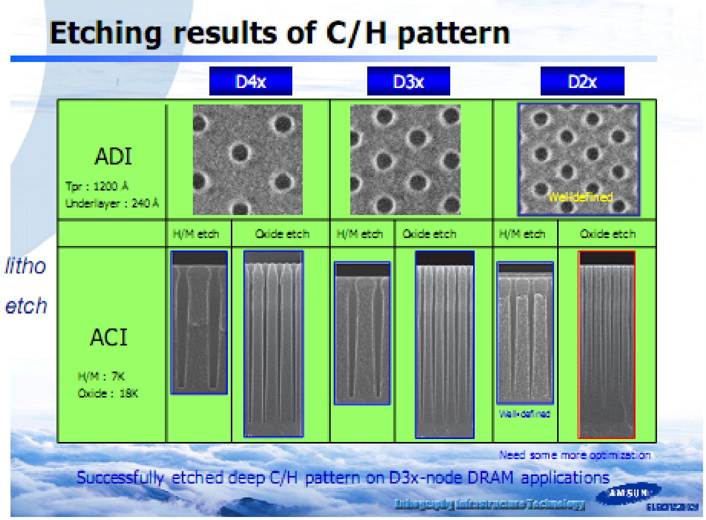
Staggered trenches 112.5 nm pitch

- Less corner rounding with EUV



Resolution Enhancement with Underlayer at ADT

- SMT3 resist, 60nm thickness on a hardmask wafer



Etching results of C/H pattern

	D4x		D3x		D2x	
ADI Tpr : 1200 Å Underlayer : 240 Å					Well-defined	
	H/M etch	Oxide etch	H/M etch	Oxide etch	H/M etch	Oxide etch
ACI H/M : 7K Oxide : 18K					Well-defined	

Need some more optimization

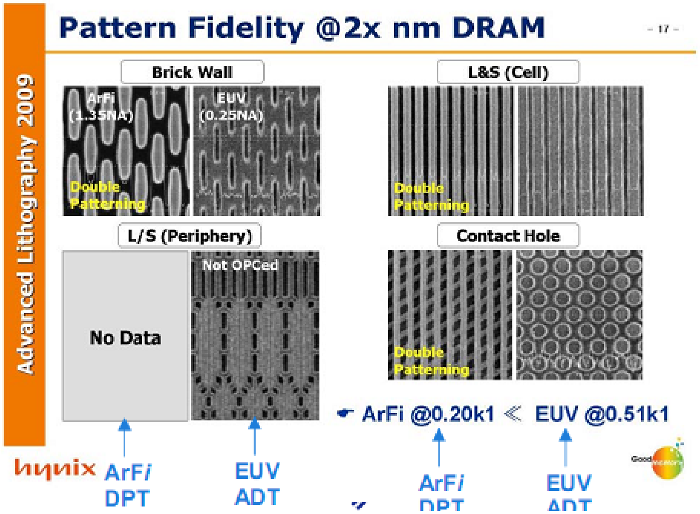
Successfully etched deep C/H pattern on D3x-node DRAM applications

ADI: after litho

ACI: after etch

Source: various SPIE presentations (Feb.'09)

Slide 14



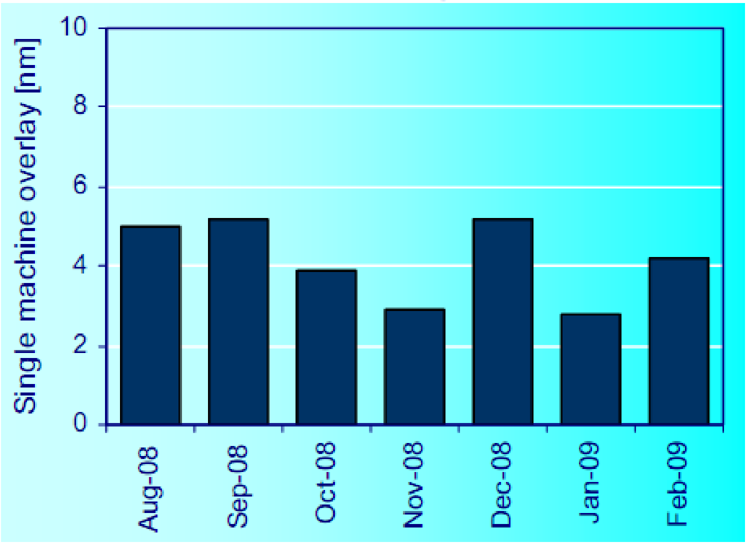
Pattern Fidelity @2x nm DRAM

☛ ArFi @0.20k1 ≪ EUV @0.51k1

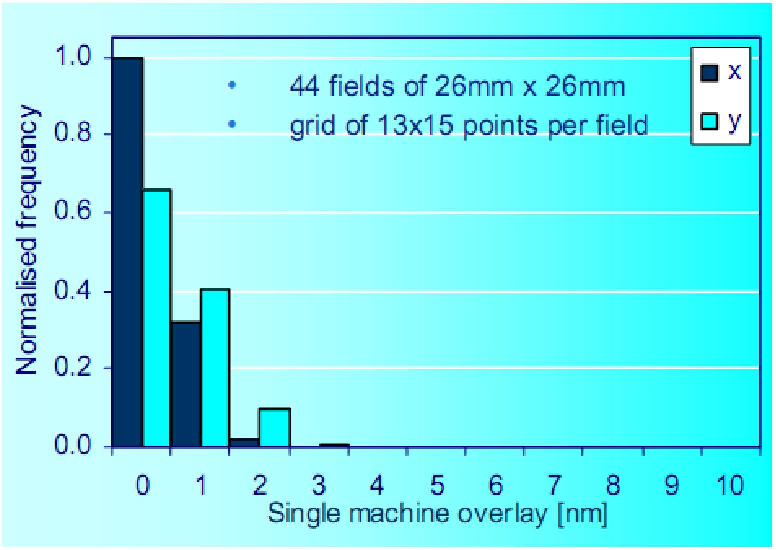
ADT Overlay Stability Data

champion data single machine overlay (SMO) is 2.9 nm

7-month stability of SMO



champion data


- 44 fields of 26mm x 26mm
- grid of 13x15 points per field

system characteristics:
120 W/2π source
~4 wph @ 5 mJ/cm^2 dose

Cymer LPP EUV Source

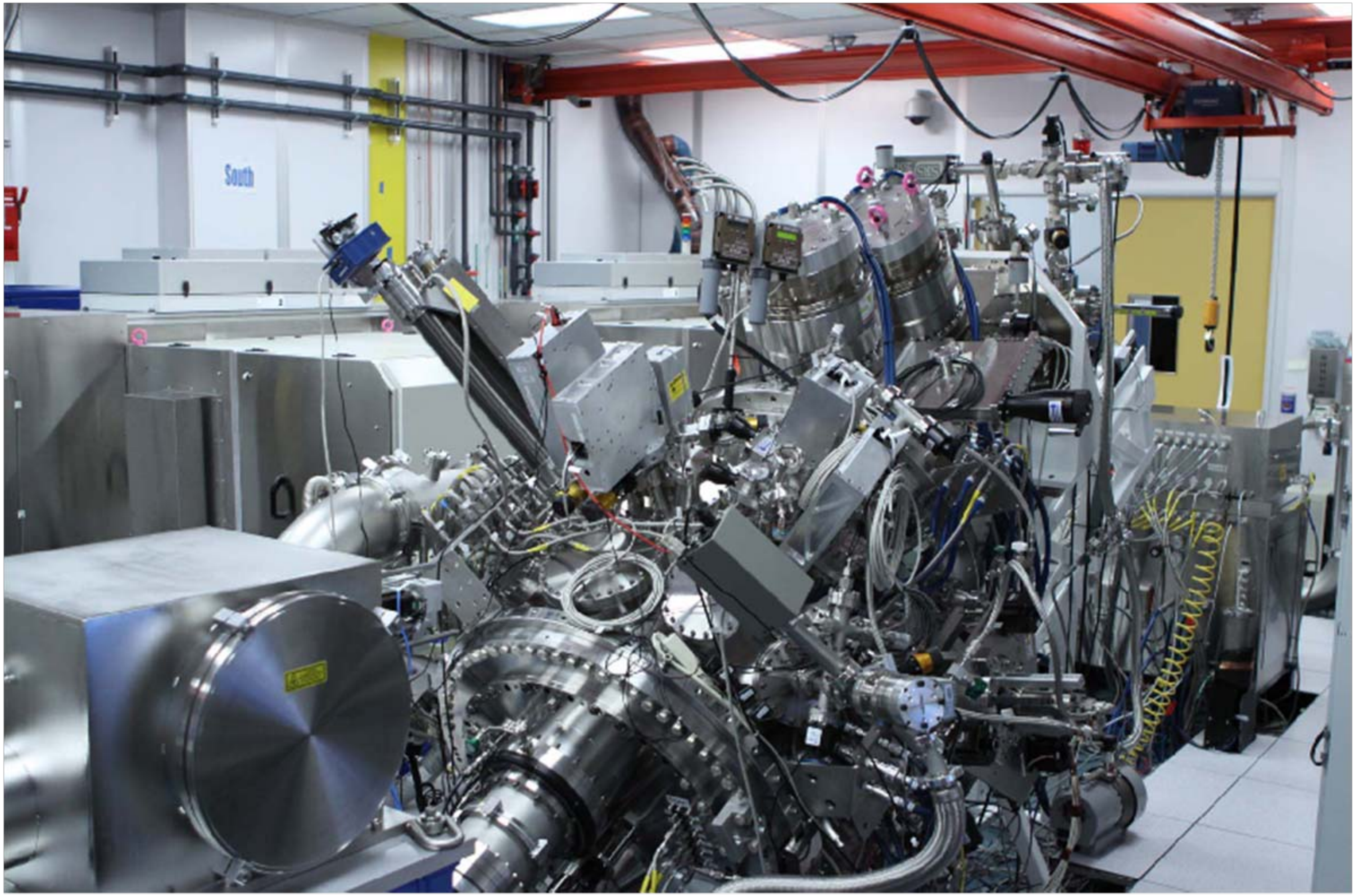
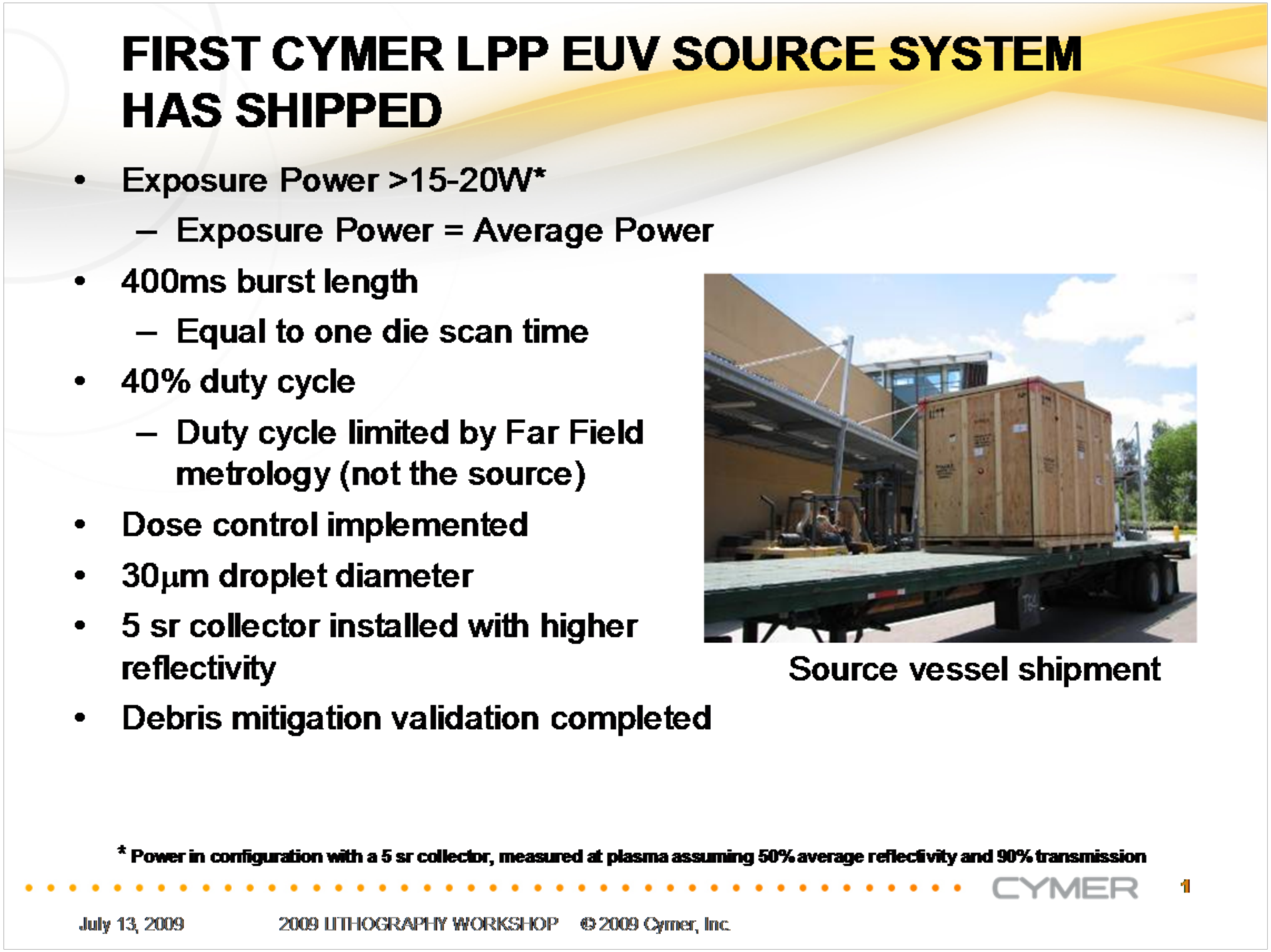


Photo Courtesy of Nigel Farrar, Cymer, Inc.

Cymer EUV Source



FIRST CYMER LPP EUV SOURCE SYSTEM HAS SHIPPED

- Exposure Power >15-20W*
  - Exposure Power = Average Power
- 400ms burst length
  - Equal to one die scan time
- 40% duty cycle
  - Duty cycle limited by Far Field metrology (not the source)
- Dose control implemented
- 30µm droplet diameter
- 5 sr collector installed with higher reflectivity
- Debris mitigation validation completed

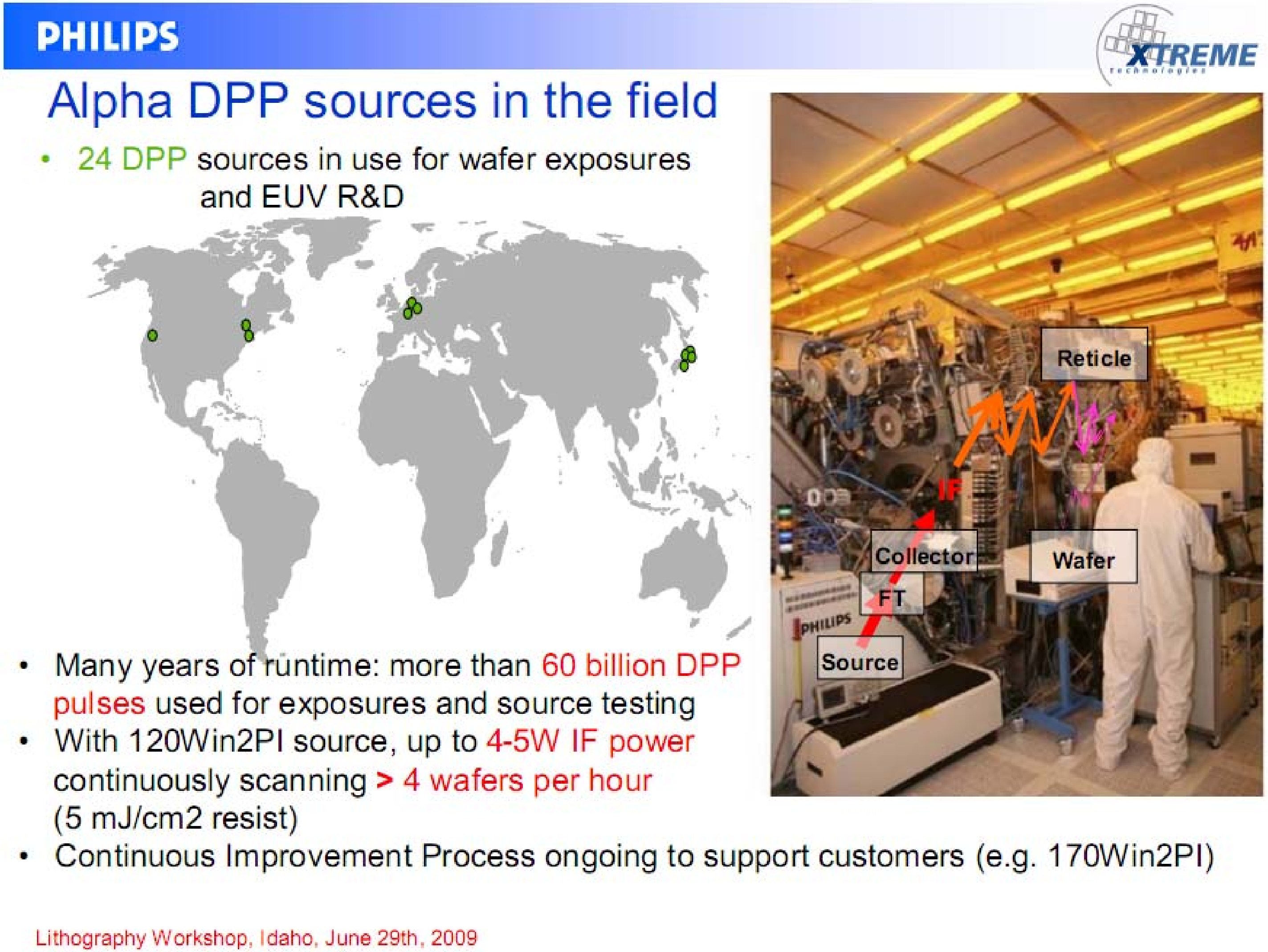
Source vessel shipment

* Power in configuration with a 5 sr collector, measured at plasma assuming 50% average reflectivity and 90% transmission

CYMER 1

July 13, 2009 2009 LITHOGRAPHY WORKSHOP © 2009 Cymer, Inc.

Philips DPP EUV Source



Alpha DPP sources in the field

- 24 DPP sources in use for wafer exposures and EUV R&D

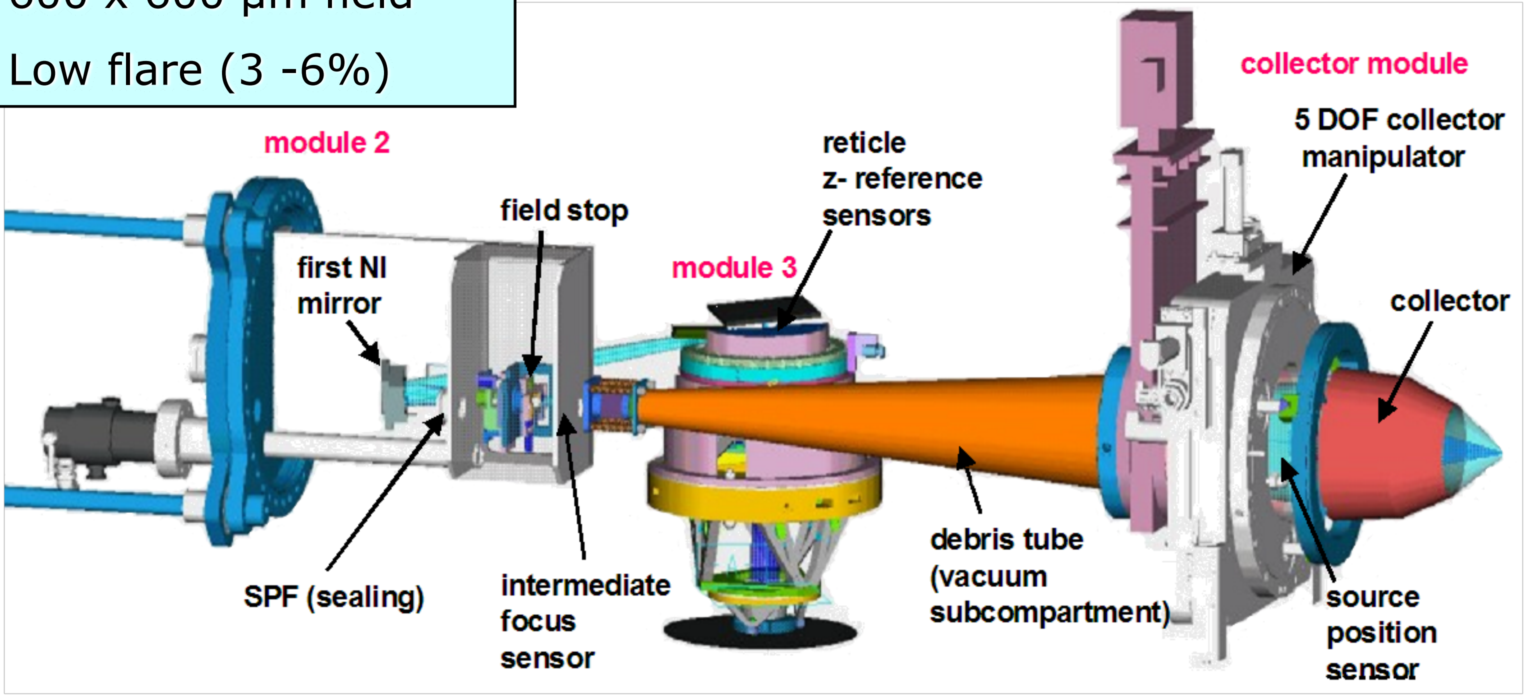
- Many years of runtime: more than 60 billion DPP pulses used for exposures and source testing
- With 120Win2PI source, up to 4-5W IF power continuously scanning > 4 wafers per hour (5 mJ/cm2 resist)
- Continuous Improvement Process ongoing to support customers (e.g. 170Win2PI)

Lithography Workshop, Idaho, June 29th, 2009

Photoresists

- 0.3NA capability
- 600 x 600 µm field
- Low flare (3 -6%)

Intel MET



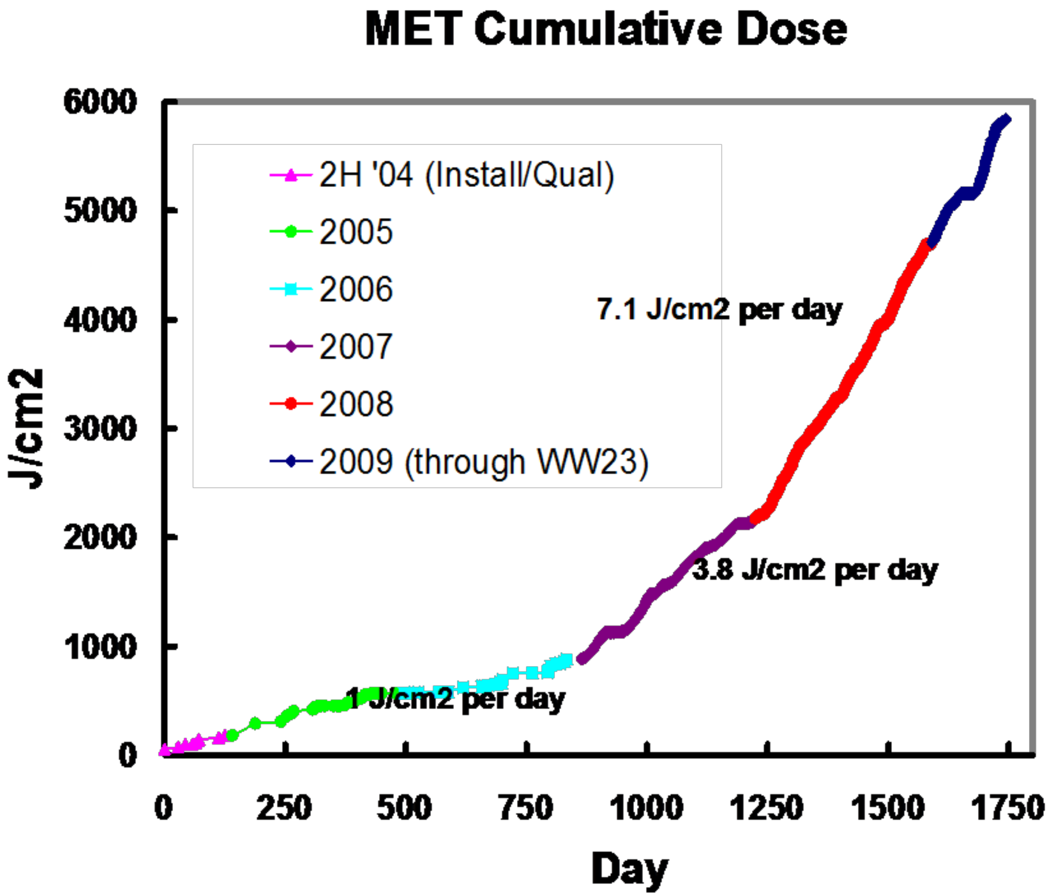
Source: (XTREME DPF Source)

0.5mm x 2mm (FWHM)

35W EUV in 2π

- New EUV collector installed
- New outer shell extended σ outer from 0.55 to 0.65, 22nm HP resolution with quadrupole illumination
- First step in preparation for 0.5 NA MET projection optics (2010) that will enable ~10nm HP resolution

Intel MET Status



Uptime average: 67% in '07, 85% in '08, 63% through WW22 in '09

Continuous improvement in output efficiency – 13J/cm^2/day currently

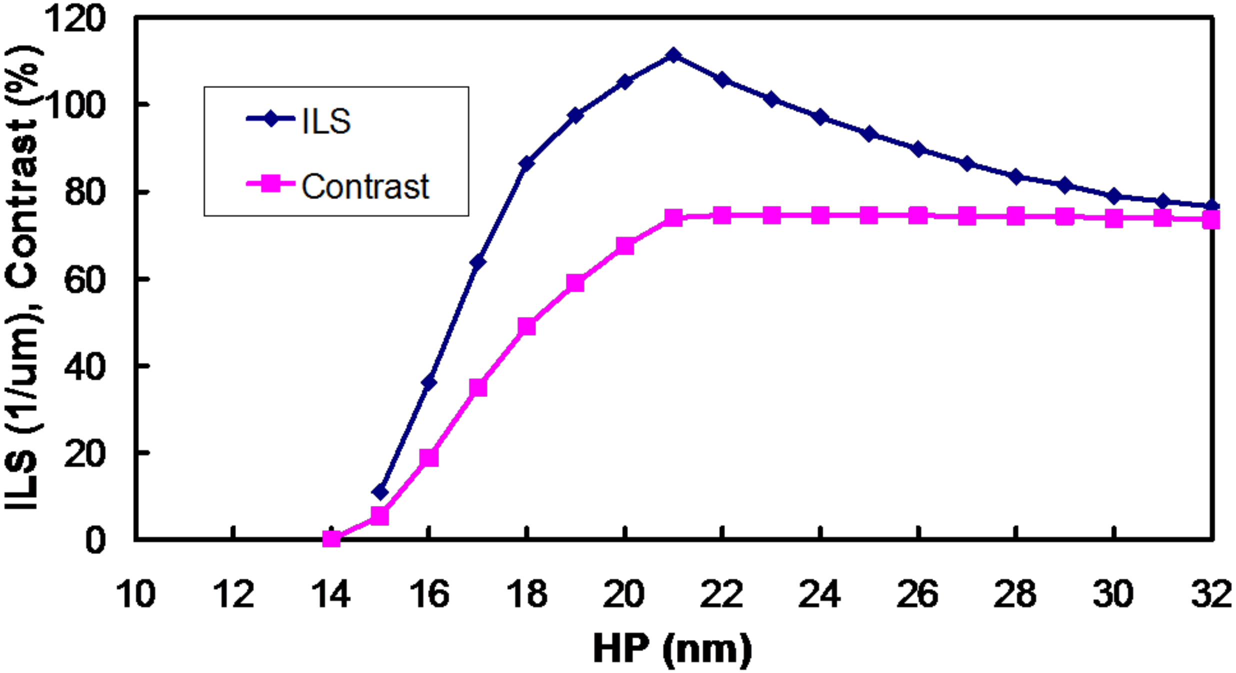
On track to deliver more dose in 2009 than in 2008

Improved resolution and expanded process window

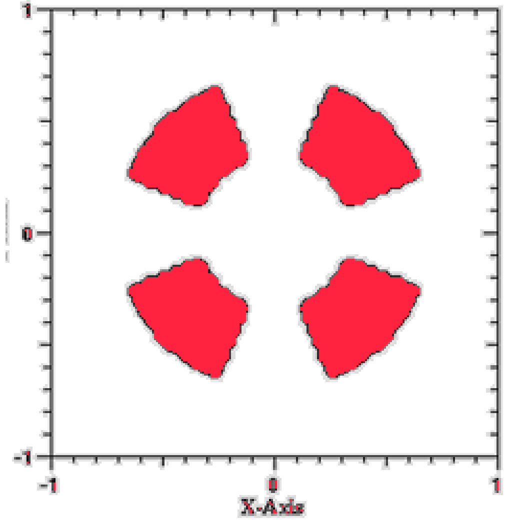
Long term upgrade path defined down to ~10nm HP

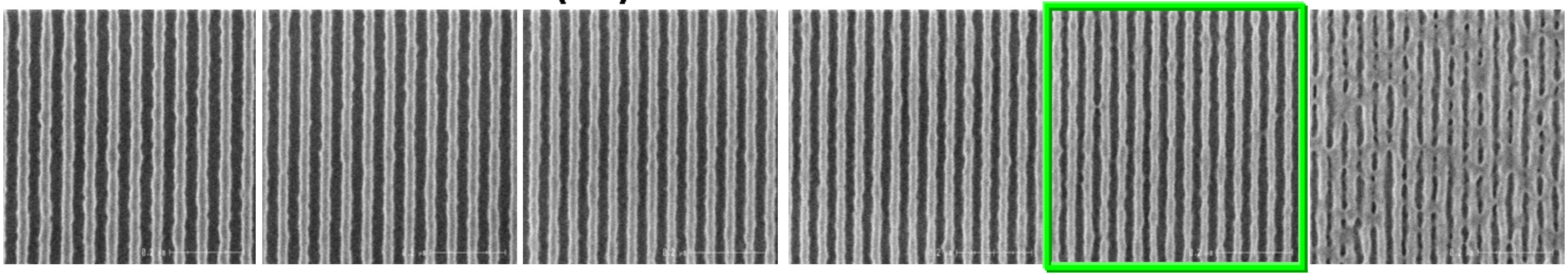
> 250 Resists Screened in '08. Goal ≥ 500 in '09

New MET Quad Source Enables 22nm HP



Quad 0.68/0.36





30nm HP

28nm HP

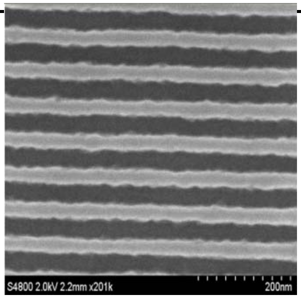
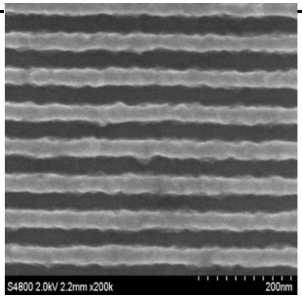
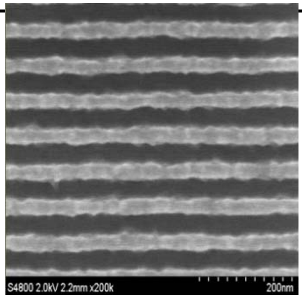
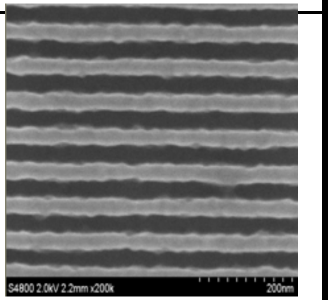
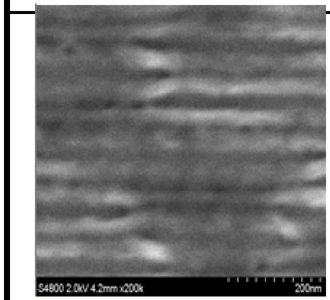
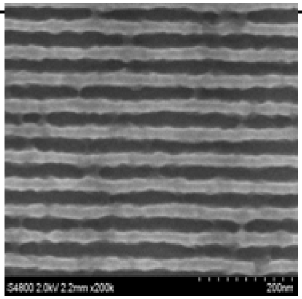
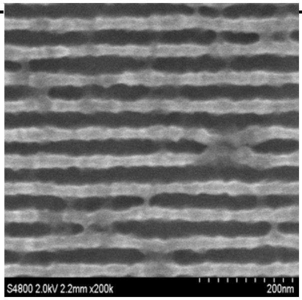
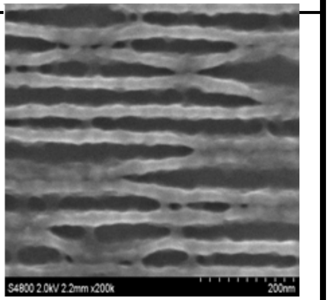
26nm HP

24nm HP

22nm HP

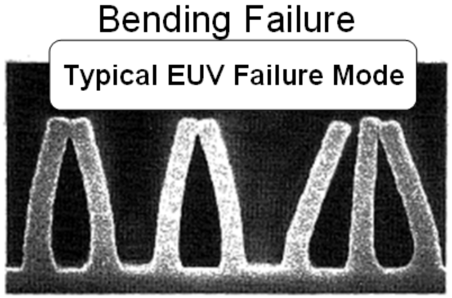
20nm HP

Berkeley ALS-MET (Rotated Dipole) :: Champion RLS Summary for 30 + 22 hp

	Resist D Esize = 13.75 mJ Min LWR = 4.8 nm UR ~ 28 nm HP	SMT01 Esize = 10.80 mJ Min LWR = 6.2 nm UR ~ 24 nm HP	Resist E Esize = 9.95 mJ Min LWR = 6.3 nm UR~ 24 nm HP	Resist F Esize = 6.85 mJ Min LWR = 5.3 nm UR~ 26 nm HP
30 HP				
22 HP				

Champion CAR platforms Nominally Meeting 22nm HP R/S Targets but Failing for LWR/PC

Pattern Collapse Margin Improvement



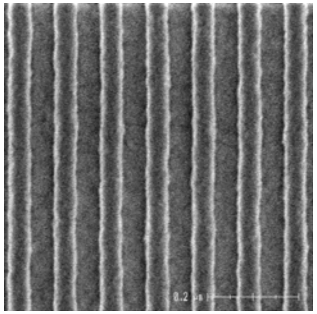
Capillary force exceeds the critical modulus of resist material.

Pattern Collapse Mitigation is primary focus for 2009

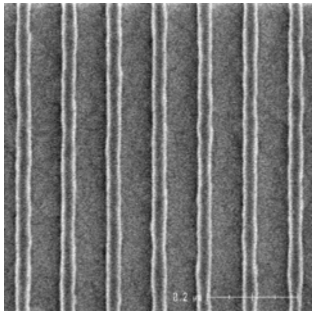
Multiple approaches may be needed to address problem

- Modify Aspect Ratio
- Surface (Energy)Optimization: Hydrophobicity, Multilayer stacks
- Increased resist modulus, Negative Tone & Semi-organic Resists
- Decreased Surface Tension: Rinse agents, Organic Developers, Develop/Rinse/Spin Dry Process Optimization

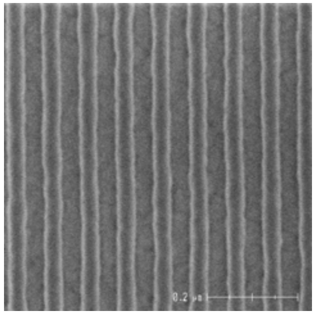
LWR Reduction Techniques



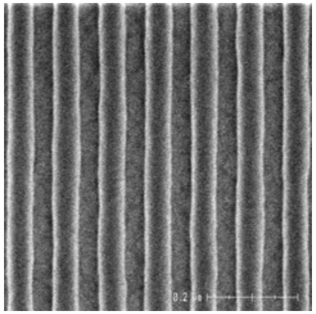
No Treatment



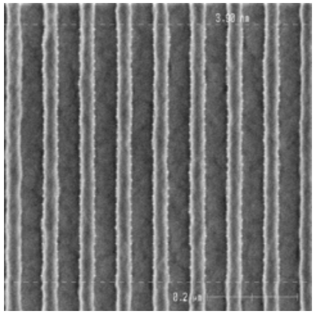
Etch/Trim



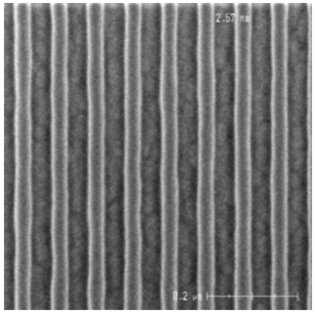
Vapor



Hardbake



Ozonation



Rinse

Chandhok *et al*, J. Vac. Sci. Technol. B, (Nov 2008)

Technique	Reduction (nm)	Reduction (%)
Etch/Trim	0.5	10
Vapor Smoothing	0.9	18
Hardbake	0.6	12
Ozonation	0.5	10
Rinse	2	40

Physical (Etch/Trim, Hardbake)

- Photoresist chemistry independent

Chemical (Vapor, Ozonation, Rinse Agent)

- Photoresist chemistry dependent

Multiple techniques may be needed to address LF & HF roughness

Largest LWR Improvement Seen with Rinse Agent

Resist and Tooling Gaps

Photoresists (32/22nm HP)

	Photospeed (mJ/cm²)	3σ LWR (nm)
Current	10/20	3.8/6.4
Target	10	1.9/1.28
Improvement Required	None/2X	2X/5X

Source Power

	Power (W)
Current	~20
Target	200
Improvement Required	10X

Scanner Runrate

	Runrate (wph)
Current	5
Target	100
Improvement Required	20X

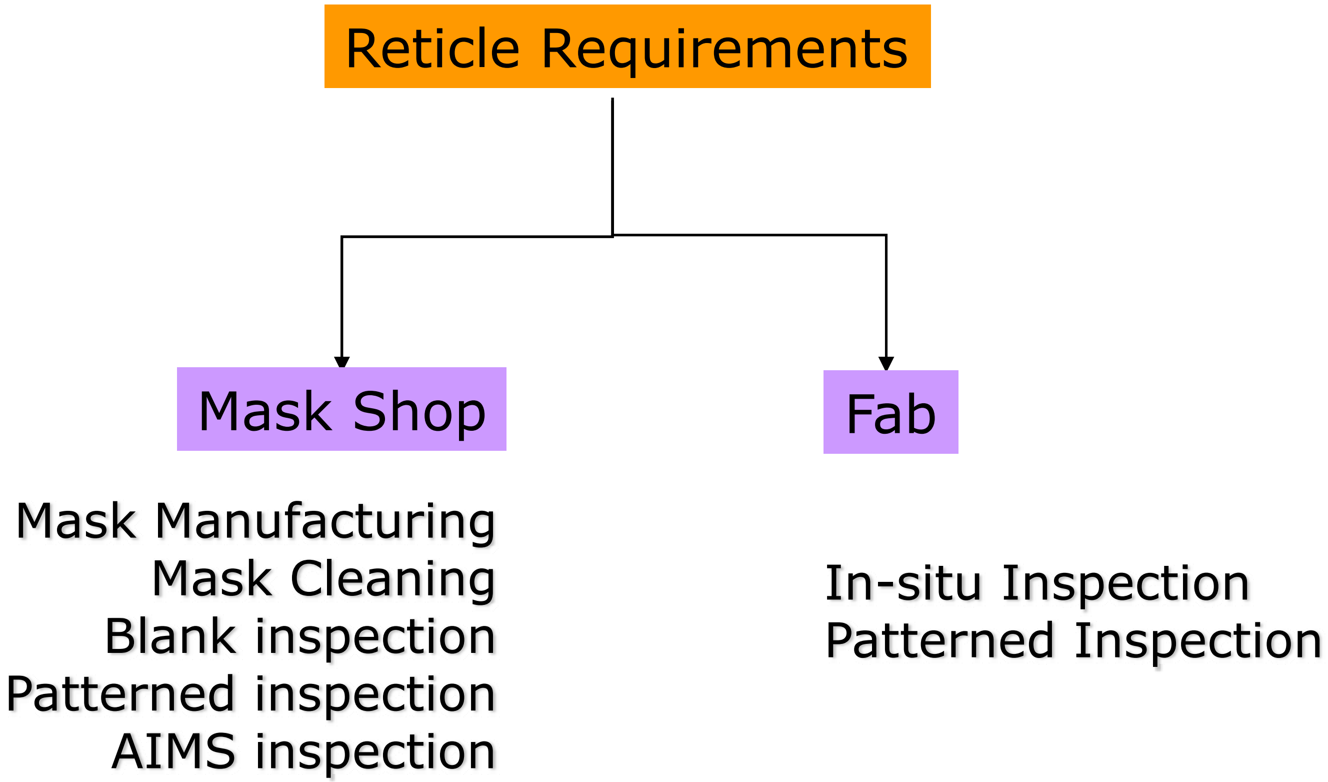
Summary:

Good progress made to date

Need continued work to bridge (or significantly reduce) gaps for both performance and COO

Reticles

HVM Reticle Infrastructure Requirements



Reticle Requirements

Mask Shop

Mask Manufacturing
Mask Cleaning
Blank inspection
Patterned inspection
AIMS inspection

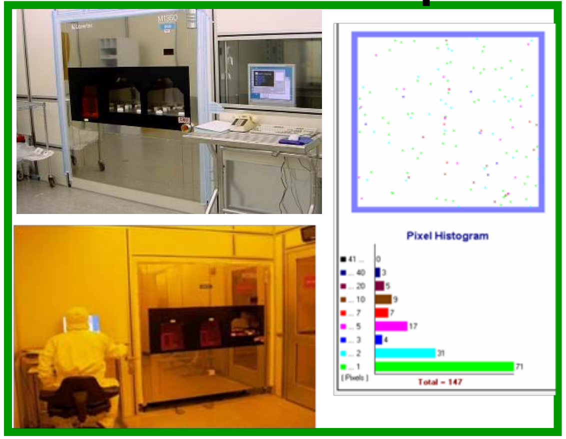
Fab

In-situ Inspection
Patterned Inspection

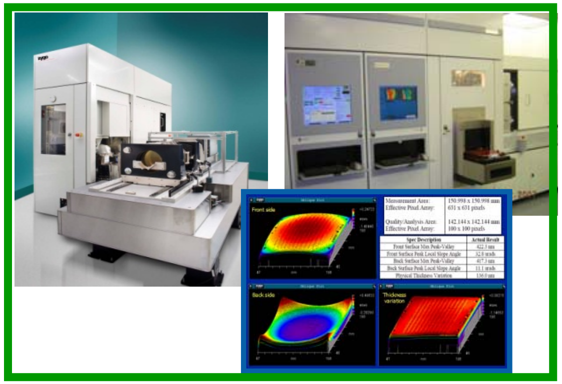
Need inspection capability in both the mask shop and the fab to ensure manufacturable operations

Intel’s Mask Tool Pilot Line

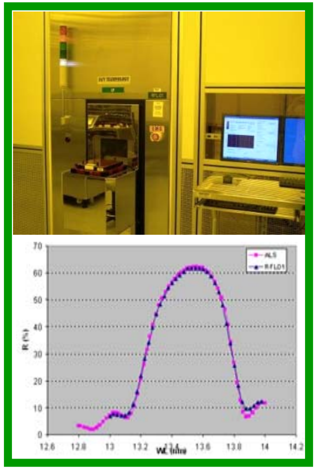
1G & 2G Blank Inspection



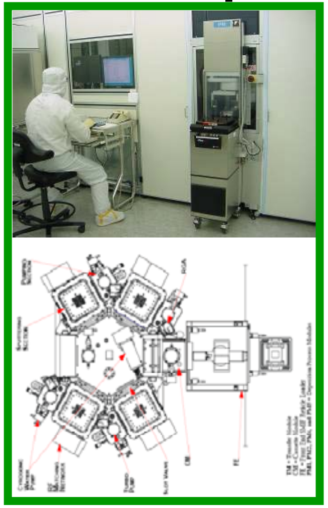
Flatness



EUV Refl



Film Dep



3G Actinic Blank Inspection

Patterned mask inspection

EUV AIMS

Sorter

Mask Clean

Mask Blank Yield Gap for Pilot Line and HVM Introduction

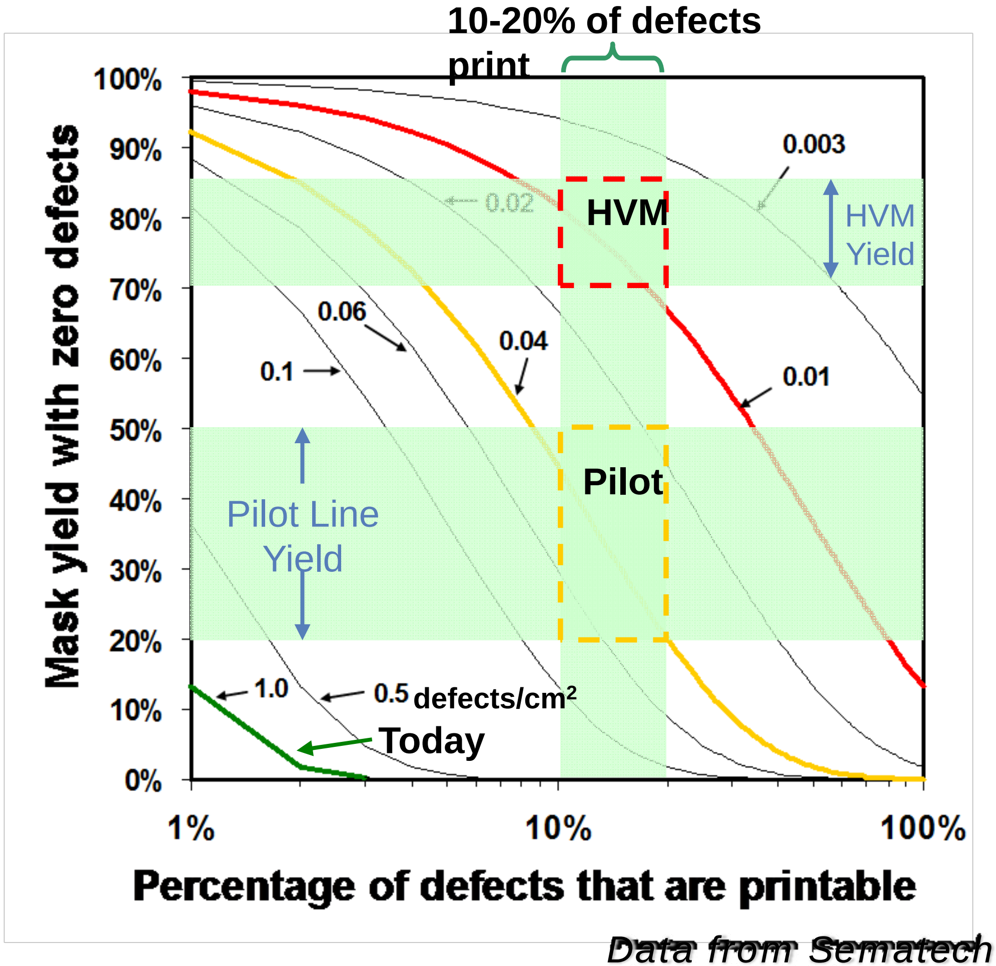
Determine Defect Density Target

- 0.003 defects/cm^2 @ 18 nm is the historical “defect free” target
    - However, recent data suggests only 10-20% of defects print
- The ultimate HVM defect density target might be 0.01 defects/cm @ 18 nm

Today: 1 defect/cm^2@18nm

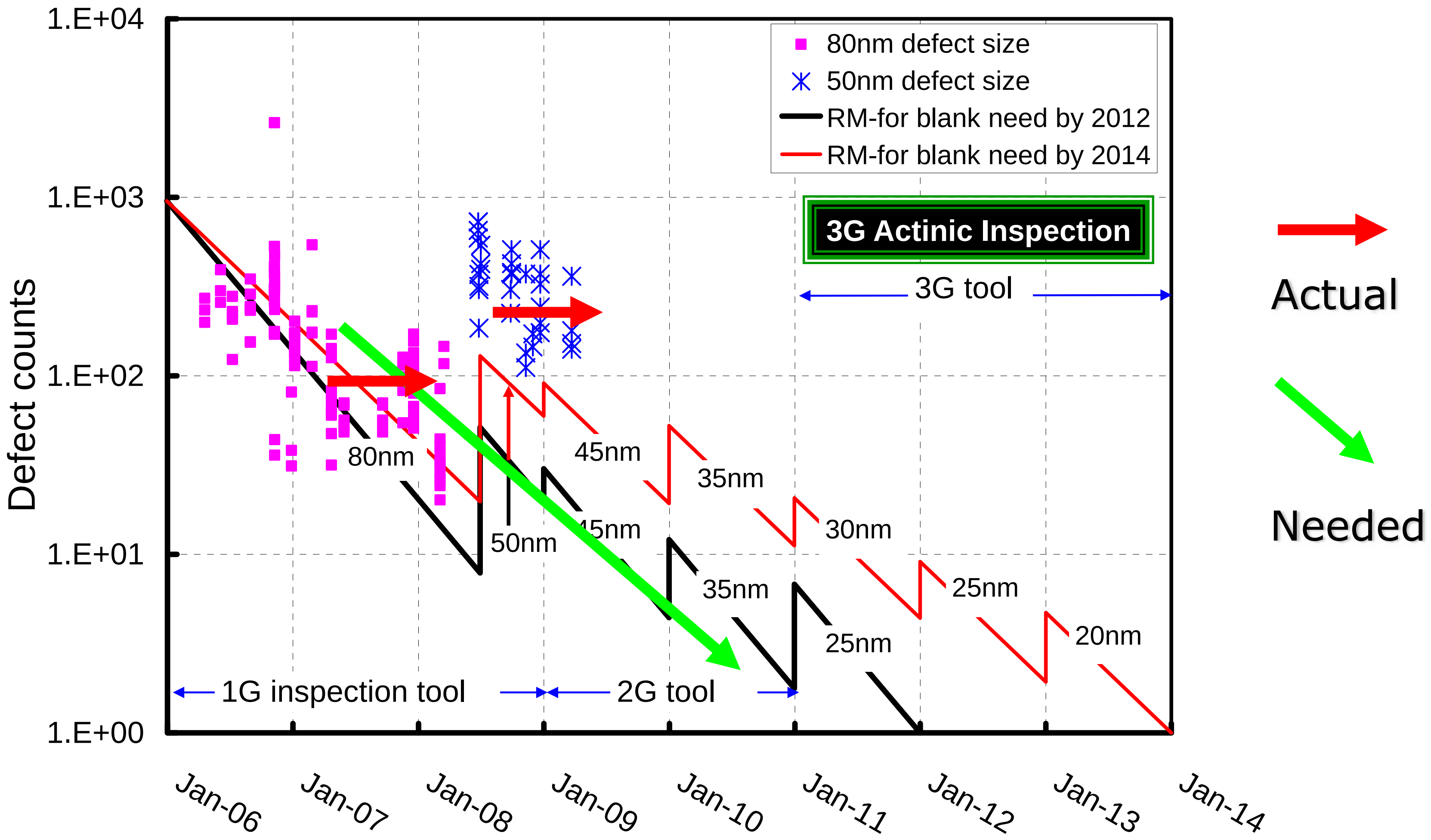
Gap to Pilot: > 25x

Gap to HVM: >100x



Data from Sematech

Mask Blank Defect Trends

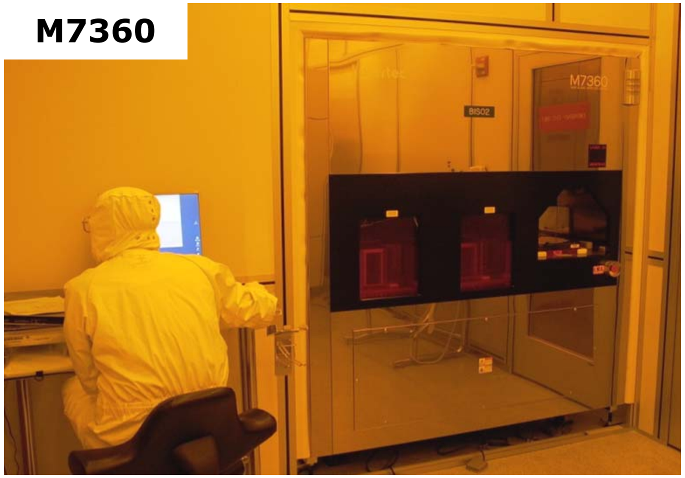


Metrology Tool Gap Limits HVM Insertion!

New Blank Defect Inspection Capability

M1350

M7360



Blank inspection tool	**G1 (M1350)**	**G2 (M7360)**	
Laser source λ	488 nm	266 nm	
> 98% capture rate	2004-Q2’08	Q3’08	Q1’09
Def. on quartz substrate	70 nm	45 nm	35 nm
Def. on ML blank	80 nm	50 nm	40 nm

- 2nd-gen mask blank inspection tool successfully installed in June
  - Inspectability will be further extended with spatial filter upgrade in Q4
- Moving toward ultimate 25nm inspection requirement for 2010-11

AIMS and Patterned Defect Inspections

AIMS:

- Industry requirement:
  - 22nm hp+ defect repair verification with scanner conditions
- Strategy for 2013 HVM:
  - HVM tool requires commercial partner, but market is small
  - Consortium model attempts underway – July summit

Patterned:

- Industry Requirement:
  - Patterned defect inspection at 22nm HP
  - KLA6XX will achieve 32nm and some 22nm HP performance
- Strategy for 2013 HVM:
  - Market is sizeable and tool cost significant
  - Suppliers unwilling to bear $250M NRE cost alone – July summit
  - SEMATECH contribution will be to broker funding model

EUV Mask Inspection Tools Summary

Development

Pilot

HVM

Size

Substrate	Blank
51	67
41	53
35	40
20	25
15	20
	15

Substrate & Blank

Lasertec M1350 (1st Generation)

M1350 & M7360 @ SEMATECH

Lasertec M7360 (2nd Generation)

2.5 Generation Substrate Inspection Tool (2.5G)

(Supplier TBD)
(can also be used for destructive blank inspection)

SEMATECH Berkeley AIT

Selete MIRAI

3rd Generation Blank Inspection Bridge Tool (3G)

(Supplier TBD)

Commercial 3G Inspection Tool

(Supplier TBD)

AIMS & Patterned

SEMATECH Berkelev AIT
- **88 nm mask CD resolution**
- **Key for defect printability understanding**

KLA 5XX

SEMATECH Berkeley AIT2
- **60 nm mask CD resolution**
- **AIMS Bridge tool**

KLA 6XX

Commercial AIMS Tool

(Supplier TBD)

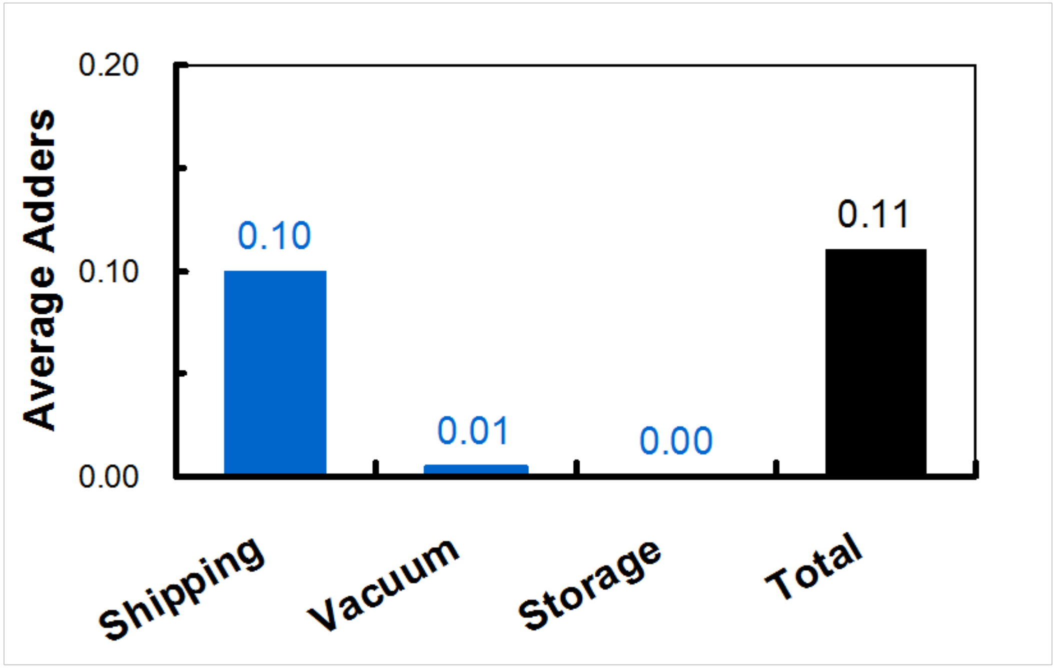
Actinic Patterned Inspection

(Supplier TBD)

ABC = Existing Tools ▭ = Actinic Inspection Tools

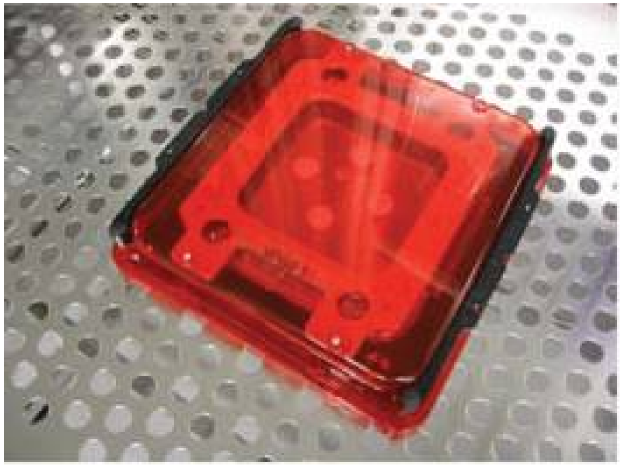
Table from Sematech

Particle-free Reticle Handling Progress

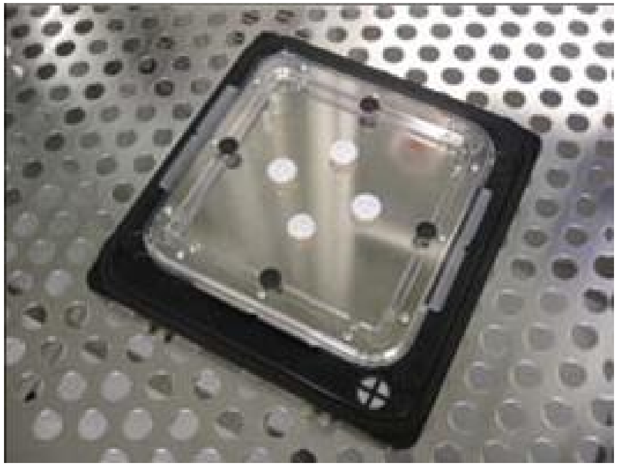


He, et al. – Proc. SPIE 6921, 69211Z (March 21, 2008)

E152 standard compliant prototype (sPod) shows reticle protection down to 0.1 added particles per lifecycle @53 nm.

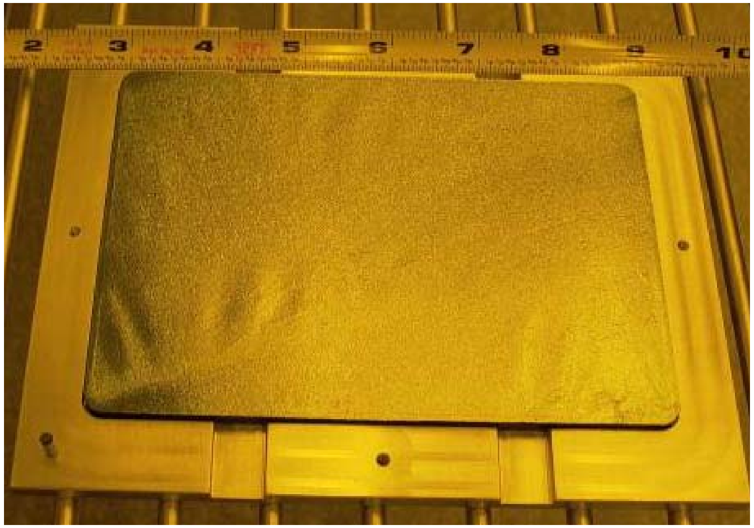


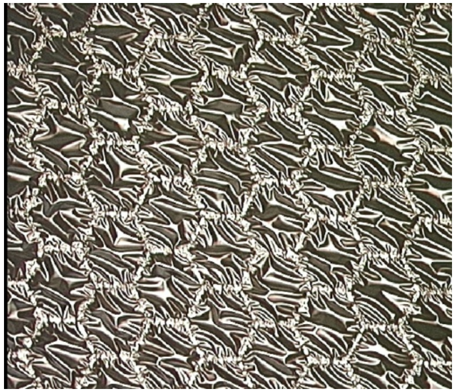
sPod Carrier



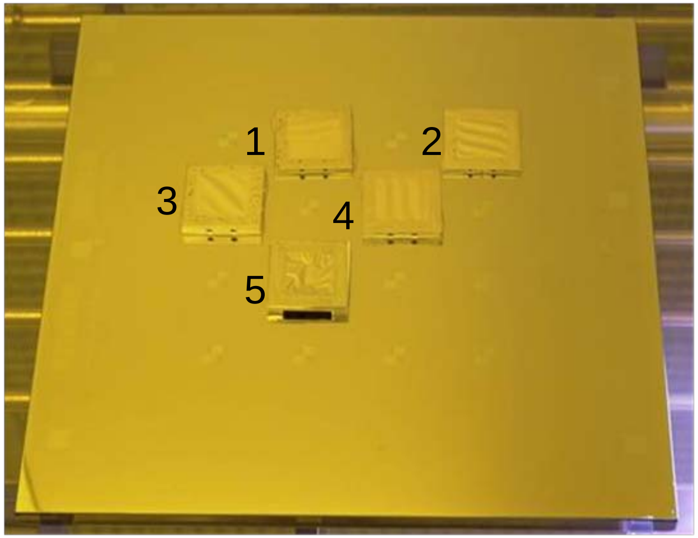
with Inner Pod Exposed

EUV Pellicle Demonstration





Hexagonal Ni mesh + Si membrane



- high risk/cost backup project
- full size pellicle demonstrated
- uniformity impact studies underway varying standoff height and mesh size

In-situ Inspection

Need to verify reticle cleanliness AFTER loading into scanner and BEFORE printing wafers

- Repeater concern is serious due to lack of pellicles
- ArF scanners have in-situ reticle inspection capability

Not having in-situ capability would require printing of defect look-ahead wafers

- Manageable in development and perhaps in pilot line mode
- Unacceptable for HVM

Need focus from tool vendors to have capability avaialable in HVM tooling platforms

Reticle Technical and Infrastructure Gaps

Current reticle defectivity gap is about 25-100X

- Need continuous improvement
- Relaxation of flatness spec might help bridge gap

Inspection gaps

- Actinic blank inspection
- Patterned defect inspection spec vs. actual
- In-situ inspection
- AIMs inspection

SEMATECH is adopting a “bridge” tool solution for actinic blank and AIMS inspection so that some capability will be available for “pilot line” in 2011

Production actinic inspection, AIMS, and patterned inspection will require industry-wide funding (July workshop)

Summing Up

HVM Gaps - Overall

	Suppliers building solutions?	Estimated Cost for HVM Solution	Time to HVM Solution
Full field production scanner	Yes	Funded	2012
Source	Yes	Funded	2011
Resist	Yes	Funded	2011
Mask Blank			
Multilayer Dep	Yes	Funded	2013
Actinic Blank Inspection	No	>50M	2013?
Actinic Defect Review	No	>50M	2013?
Mask Patterned Inspection	No	>100M	2013?

Table from Bryan Rice, Sematech

SEMATECH’s EUV mask infrastructure strategy is:

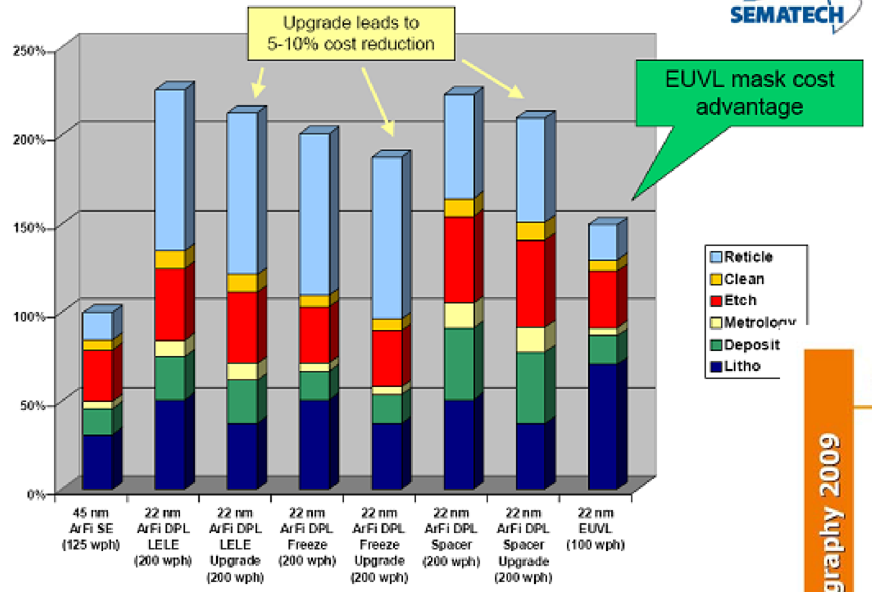
- Obtain support from various partners (public and private)
- Commit most of SEMATECH’s Litho budget to mask infrastructure over next four years

Need industry consensus on required funding to bridge gaps

EUV Cost-Effectiveness

Results – 22 nm (Rigorous, 20,000 wpm)

SEMATECH

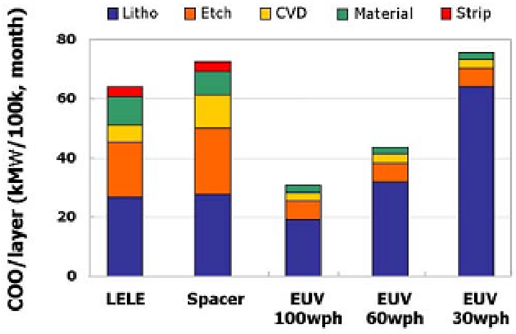


25 February 2009

Advanced Lithography 2009

COO of EUV Lithography

- 5 -



☛ Success or failure of EUV depends on throughput.

hynix

Source: Sematech, Hynix – SPIE 2009

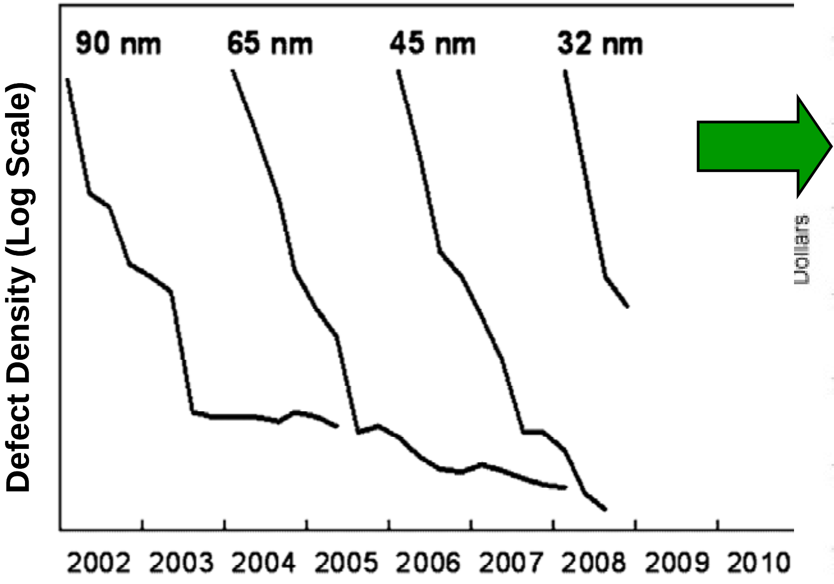
COO!

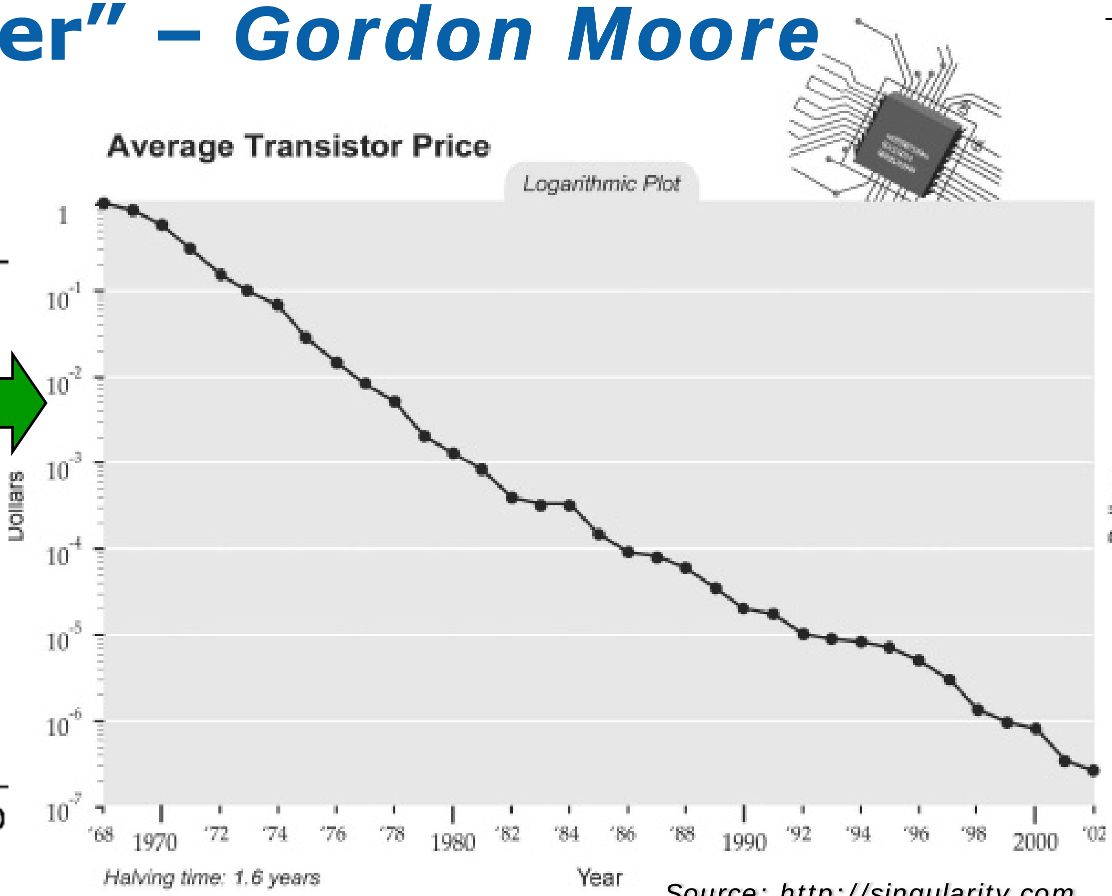
Slide 5 |

ASML

No Exponential is forever, but we can delay “forever” – *Gordon Moore*

Scaling + Yield





Source: http://singularity.com

Will EUV performance and COO enable us to continue to delay “forever?”

Conclusions

Substantial progress made on resist and tooling

- Resists typically about 2X from goal for sensitivity/LWR
- Laser power about 10X from goal
- Overall tool runrate requires ~ 20X improvement to 100wph goal

Reticle defectivity is a major concern

- Blank defectivity needs substantial improvement
- Relaxation of flatness requirement might provide some mitigation
- Reticle inspection capability has major gaps. Need industry funding to enable tooling to be developed in time for HVM

Academic exercise is over!!

- EUV has moved from research to implementation mode
- Problems left to be solved are largely engineering in nature
- Need sustained focus and industry-wide commitment to solve

Ultimately EUV insertion will be based on a COO decision vs. ArF

intel®

Leap ahead™