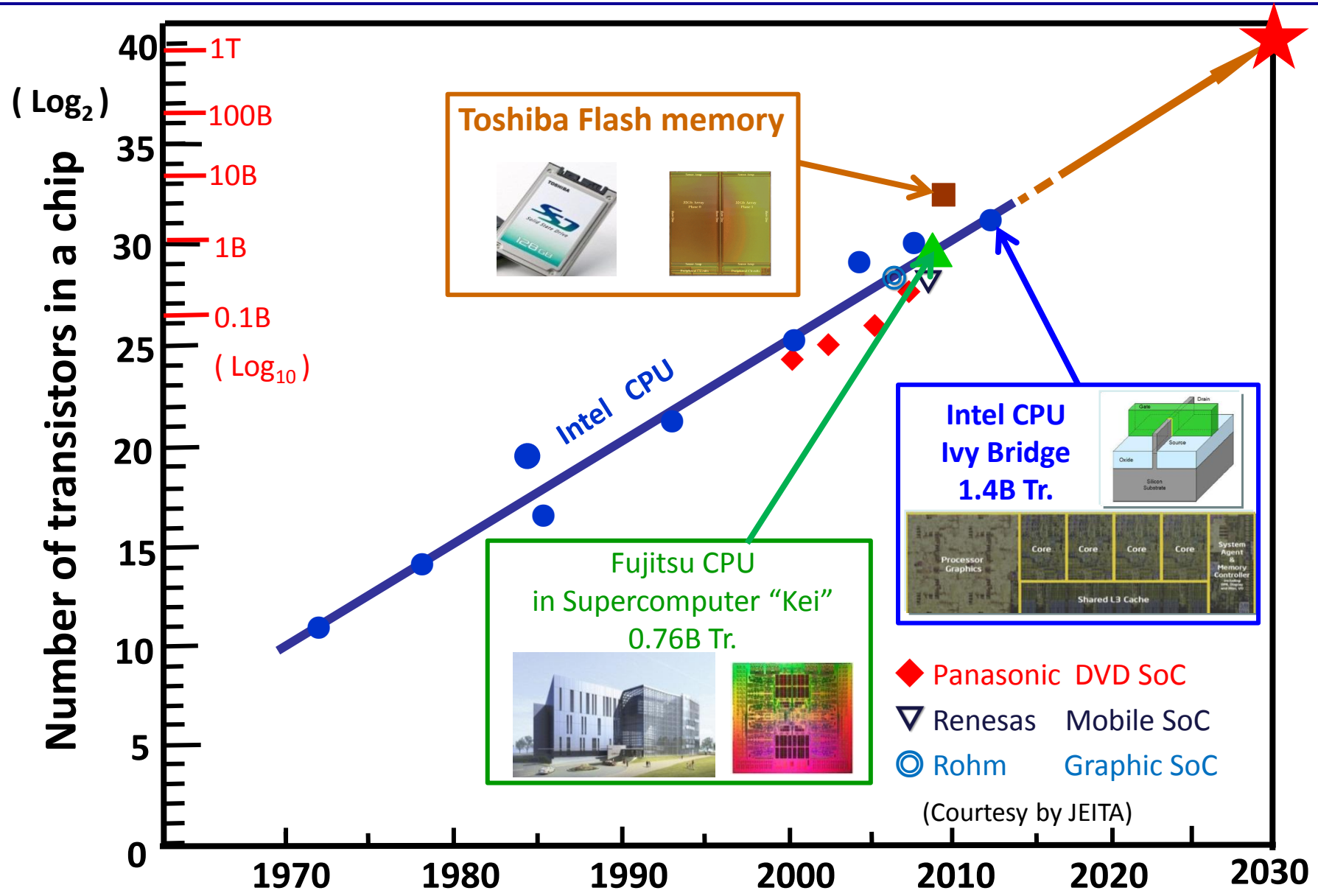
Persistent Efforts to Overcome the Challenge of EUVL

Soichi Inoue
EUVL Infrastructure Development Center, Inc.

Agenda

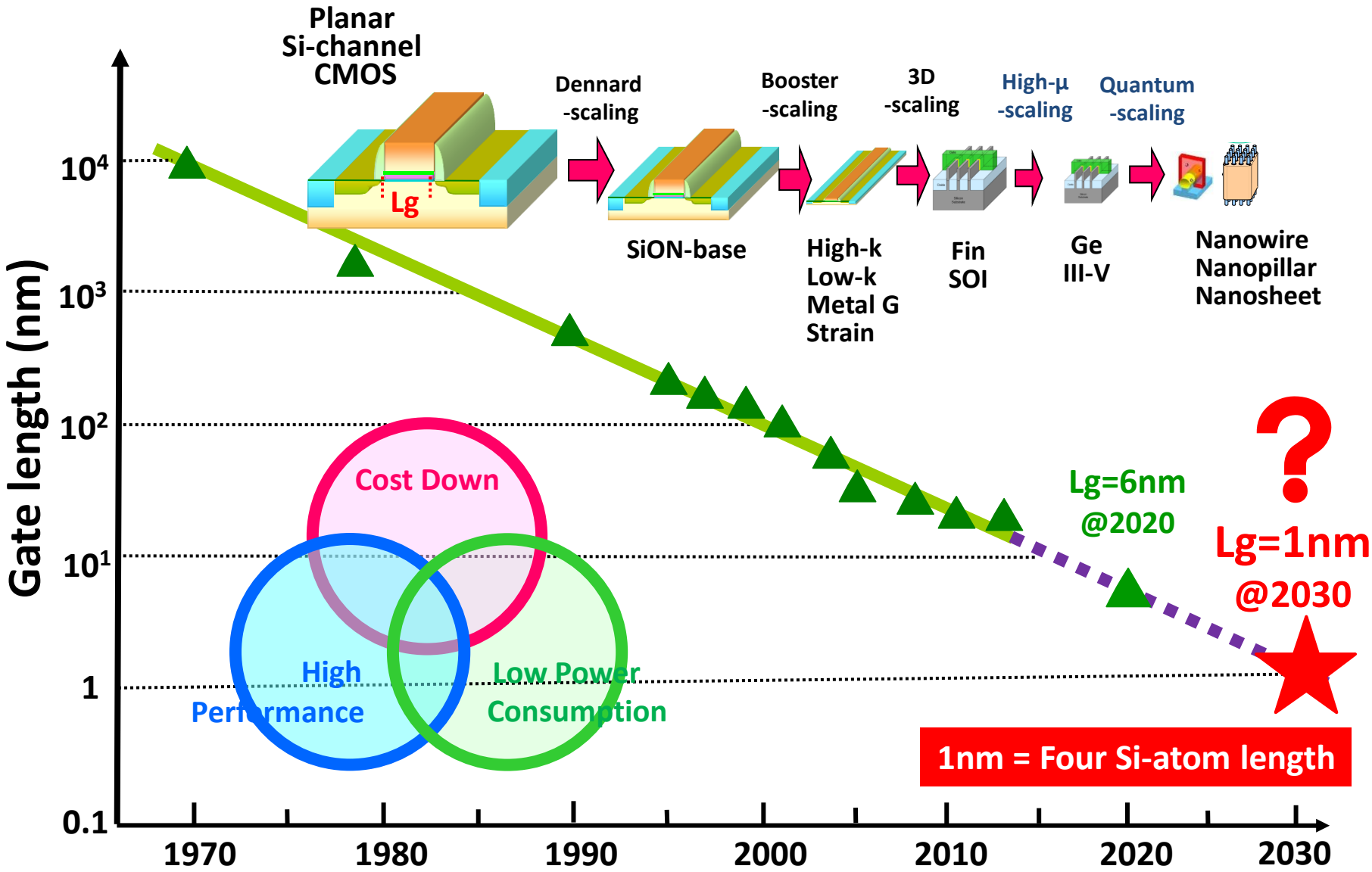
- Trend of LSI Downscaling
- Lithography Prospect
- Technical Challenge for EUVL
- Role of EIDEC
- Persistent Efforts for Each Technology Development
  - Mask
  - Resist / Process
  - Source / Scanner
- Summary

More Moore !



Intel CPU plots, except Iyv Bridge, are shown in http://www.intel.com/jp/technology/mooreslaw/index.htm?iid=jpIntel_tl+moores_law

Trend of Downscaling



How About Is Millennial Roadmap ?

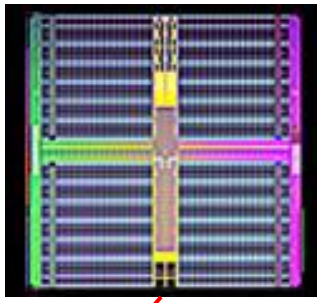
ELSEVIER

Microelectronic Engineering 41/42 (1998) 41–46

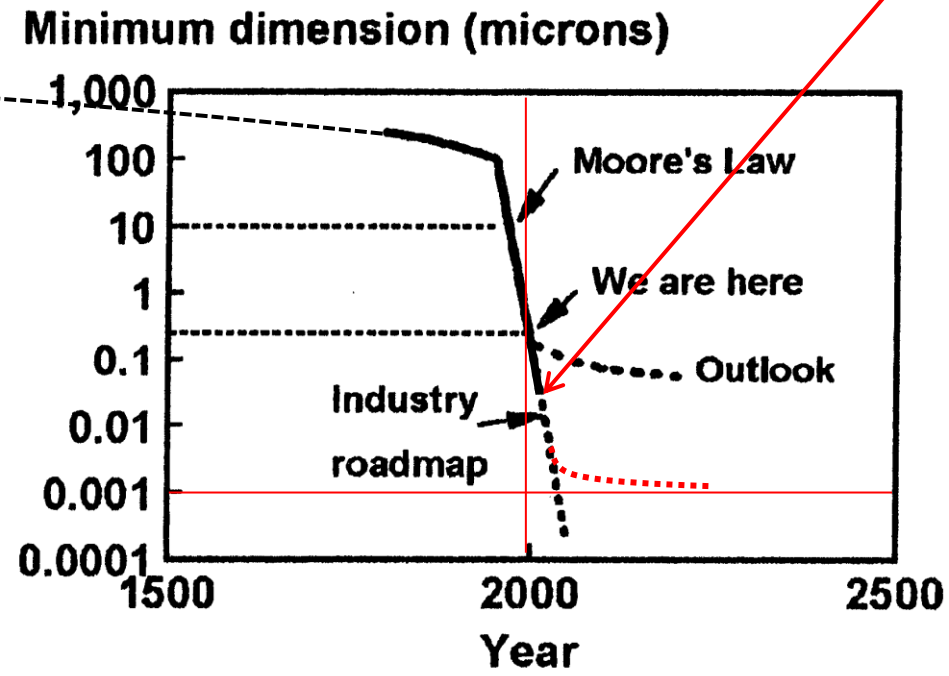
MICROELECTRONIC ENGINEERING

Microlithography in midlife crisis

Christopher P. Ausschnitt
IBM Advanced Semiconductor Technology Center
Hopewell Junction, New York



Gold Stamp (AD100)
Dimension ~ 1mm



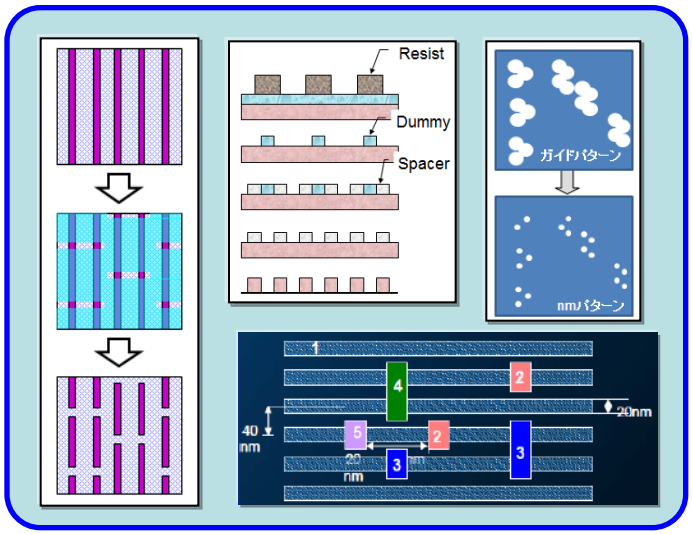
Lithography Prospect

hp70nm hp56nm hp43nm hp3xnm hp2xnm Next (=hp1xnm)

ArF (DRY)

ArF (Water Immersion)

EUVL



ArF Immersion Extendibility

Double Patterning Technology

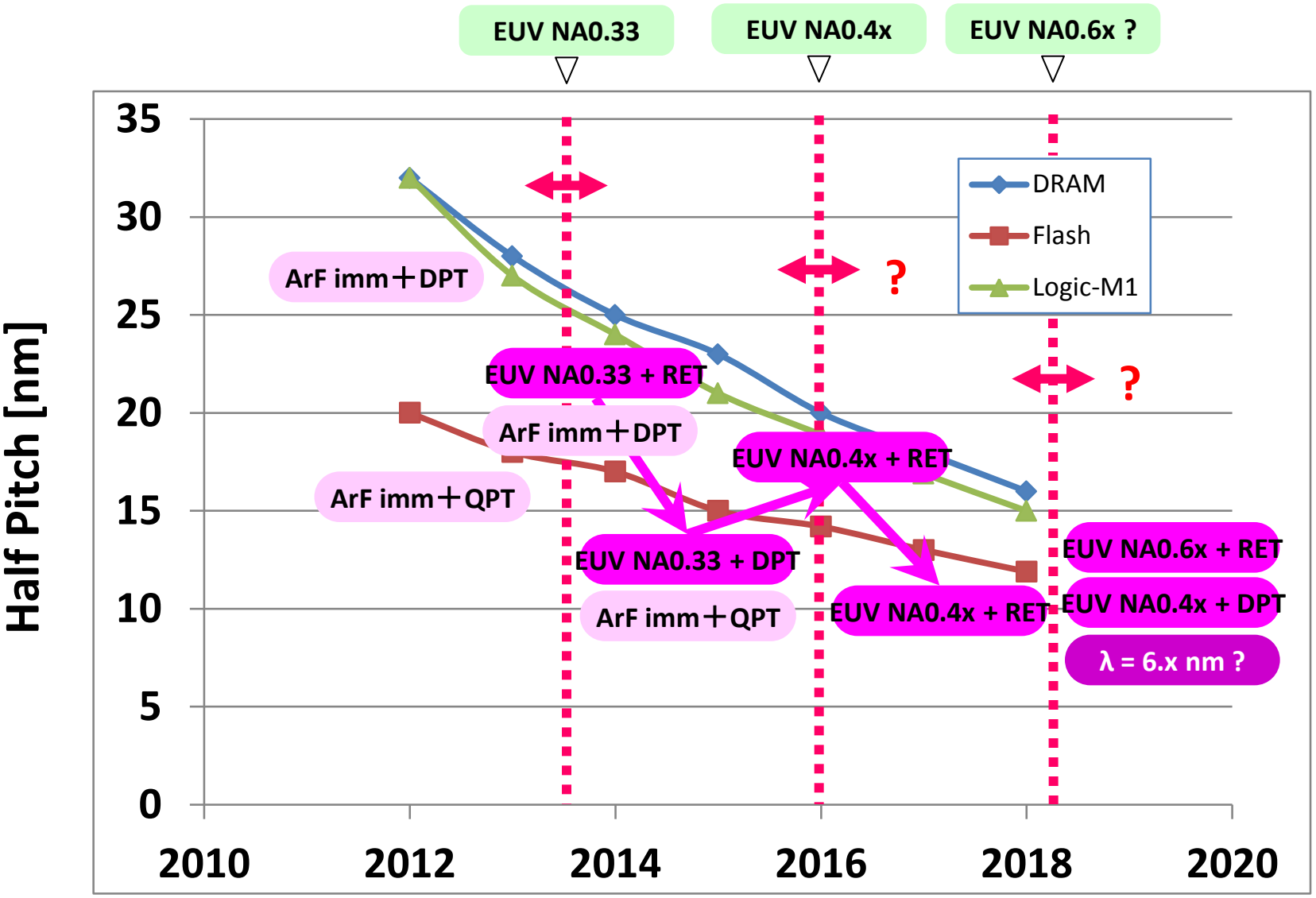
Nanoimprint

DSA

ML2

- ✓ **Technology direction will be decided by development schedule, performance and economics.**
- ✓ **EUV lithography will be the main stream technology from cost and extendibility viewpoint.**

Scenario of EUV Insertion



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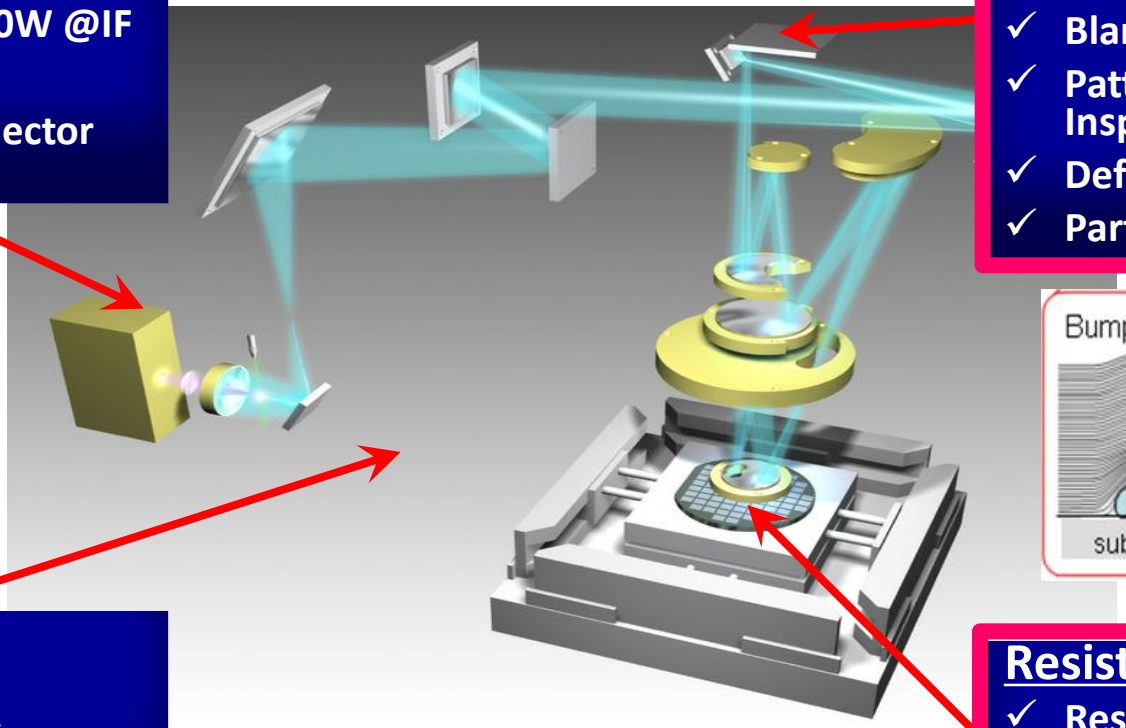
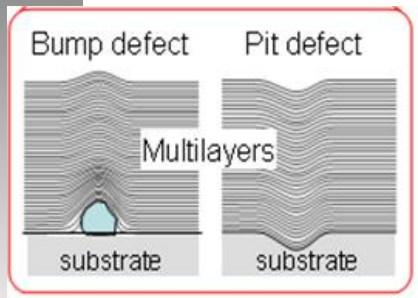
Technical Challenge for EUVL

Source
- ✓ High power: 250W @IF
- ✓ Stability
- ✓ Long Life of Collector Mirror

Mask
- ✓ Blank Inspection
- ✓ Patterned Mask Inspection
- ✓ Defect Review System
- ✓ Particle Free Handling





Courtesy by EUVA

Scanner
- ✓ Field data
- ✓ Higher quality / Long lifetime of optical components

Resist
- ✓ Resolution < 20nmHP
- ✓ Sensitivity < 10mJ/cm^2
- ✓ LER < 2nm
- ✓ Lower outgassing

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EIDEC Outlook

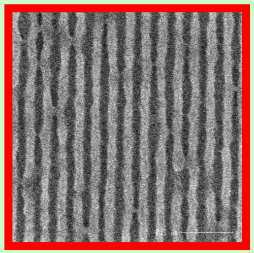
◆Project Start : 2011-4-1

2011	2012	2013	2014	2015
Phase-1 hp 16nm			Phase-2 hp 11nm	

◆ Focus Area

Blank/Mask defect inspection

Resist development



*AIST Super Clean Room @ Tsukuba

◆ Programs （EIDEC Project is supported by METI and NEDO)

1. Blank Inspection
2. Patterned Mask Inspection
3. Resist Materials
4. Resist Outgassing Control

◆Member Companies (16)

(Mask/Blank)
- AGC
- DNP
- HOYA
- TOPPAN

(Resist/Material)
- FUJIFILM
- JSR
- Nissan Chemical
- Shin-Etsu Chemical
- TOK

(Device)
- Intel (USA)
- Renesas Electronics
- Samsung (Korea)
- SanDisk (USA)
- SK Hynix (Korea)
- TOSHIBA
- TSMC (Taiwan)

◆ JD Companies (2)
- EBARA
- Lasertec

◆ JD Research Institutes (3)
- AIST
- Osaka University
- University of Hyogo

*AIST: National Institute of Advanced Industrial Science and Technology

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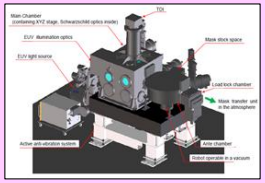
Status of Mask Infrastructure

Blank Inspector

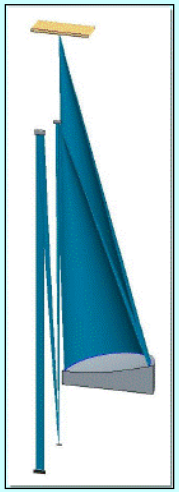
193 nm



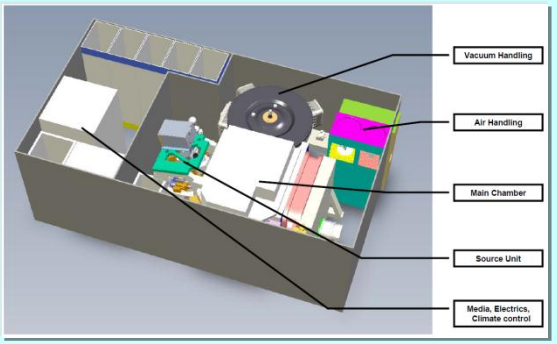
EUV (Dark Field)

EUV (Bright Field)

Defect Reviewer



EUV-AIMS (13.5nm)



Patterned Mask Inspector

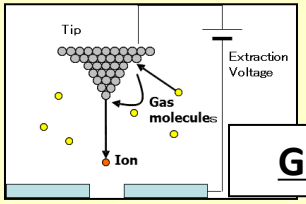
199 nm

193 nm

e-Beam (SEM, Projection)

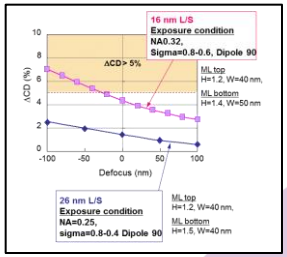
EUV (13.5 nm)

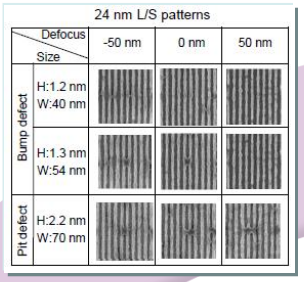
Defect Repair Tool

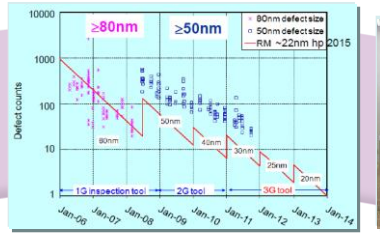


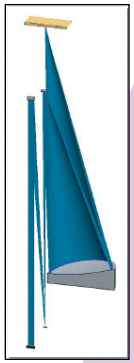
GFIS

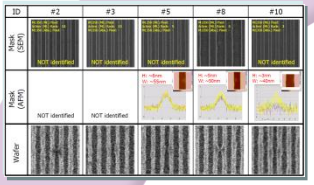
Challenges for "Effective" Phase Defect-free Blank

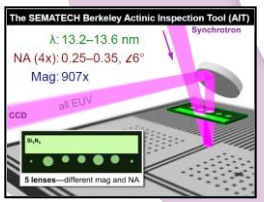


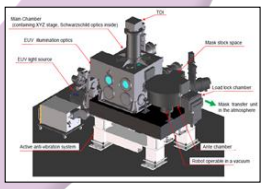


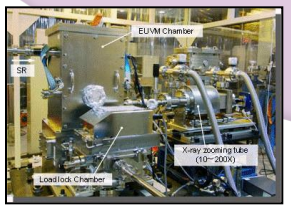


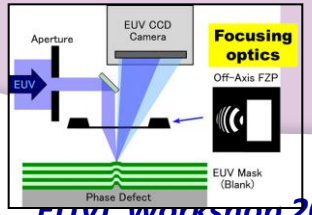


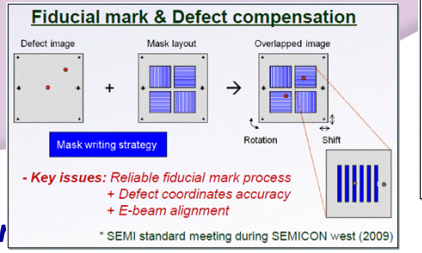


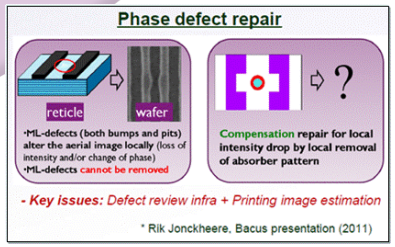






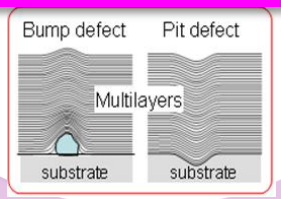






Defect Reduction

Phase Defect



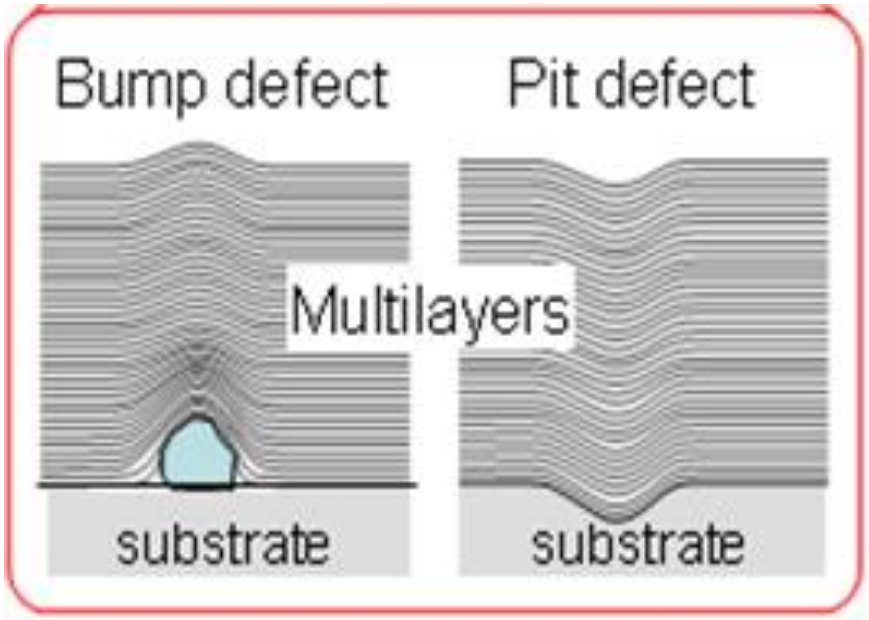
CD Impact (Real Defect Traceability)

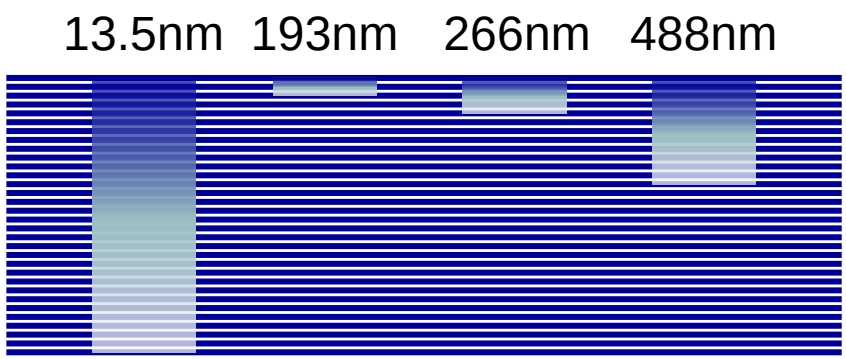
Defect Inspection

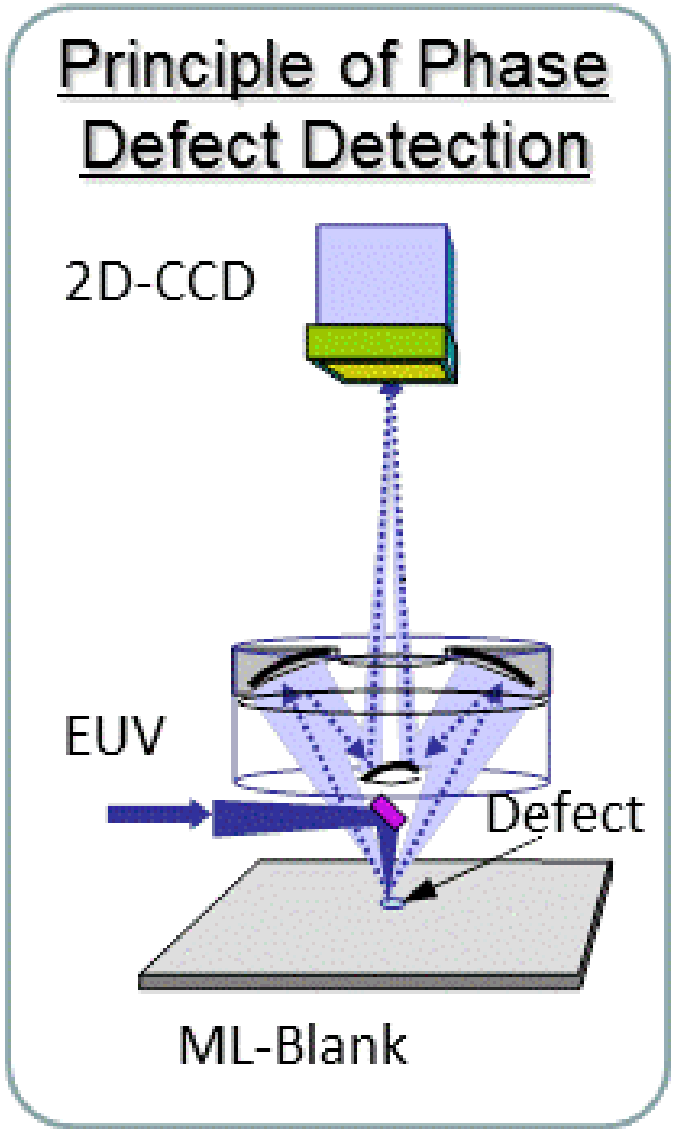
Defect Review & Characterization

Defect Mitigation

Dark Field Actinic Blank Inspector (ABI)

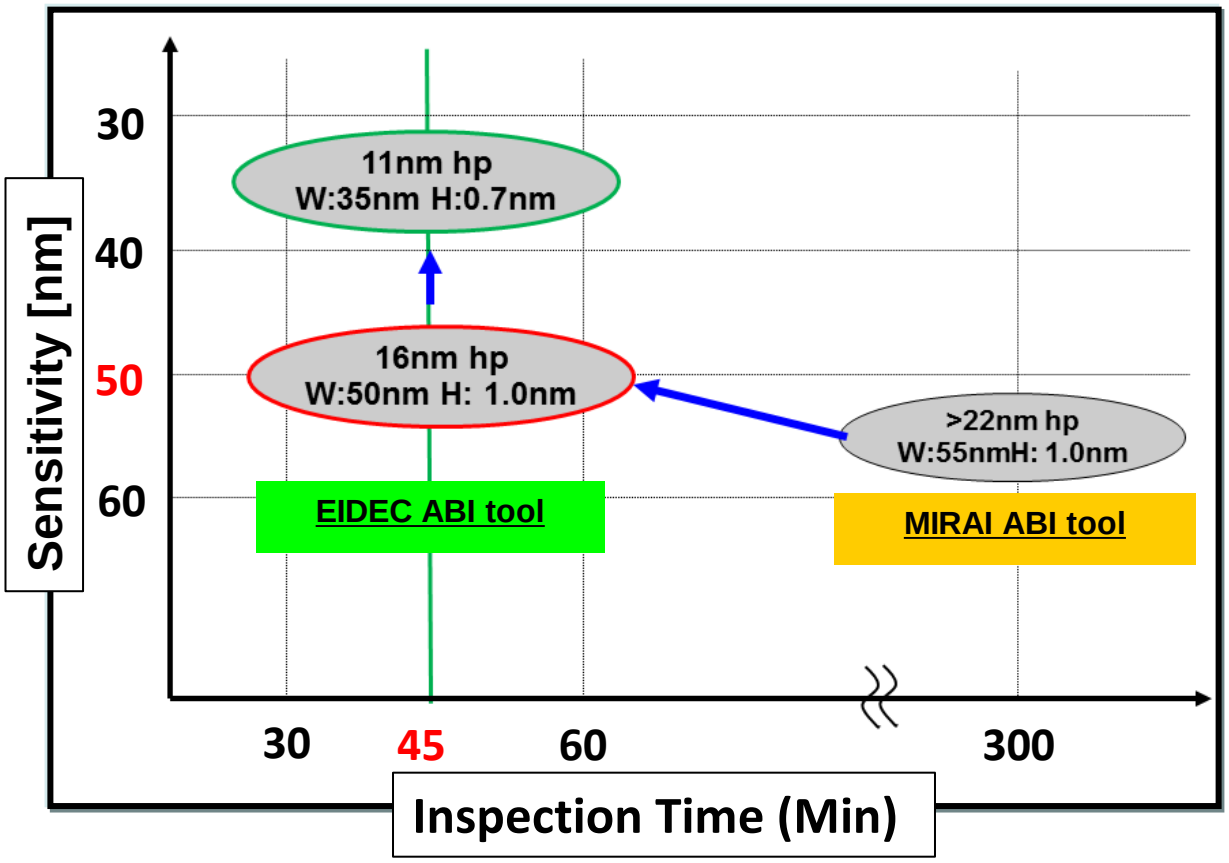






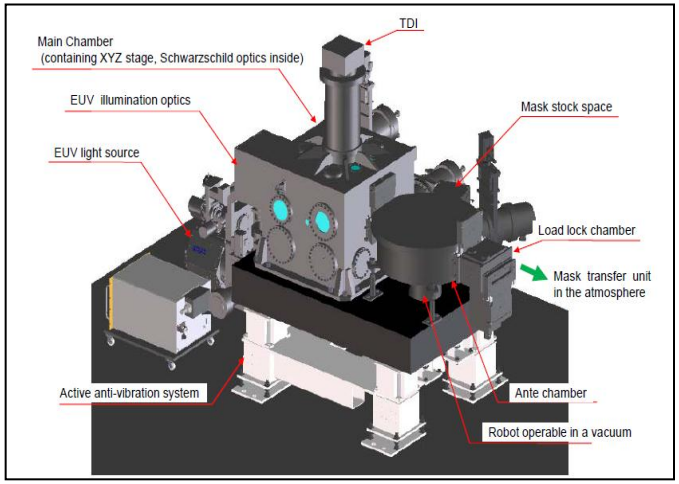
Progress of Actinic Blank Inspector (ABI)

Higher sensitivity and throughput (16 and 11nm hp)



MIRAI ABI tool

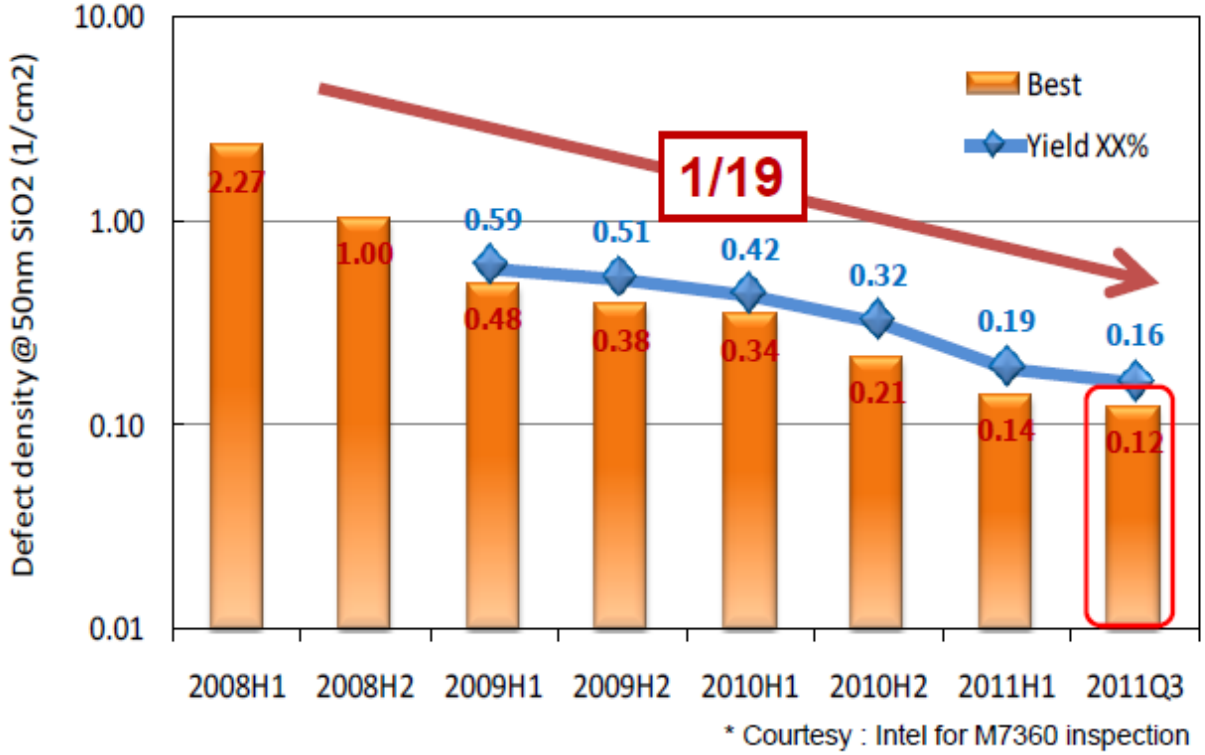
EIDEC ABI tool



Current Status of Phase Defect

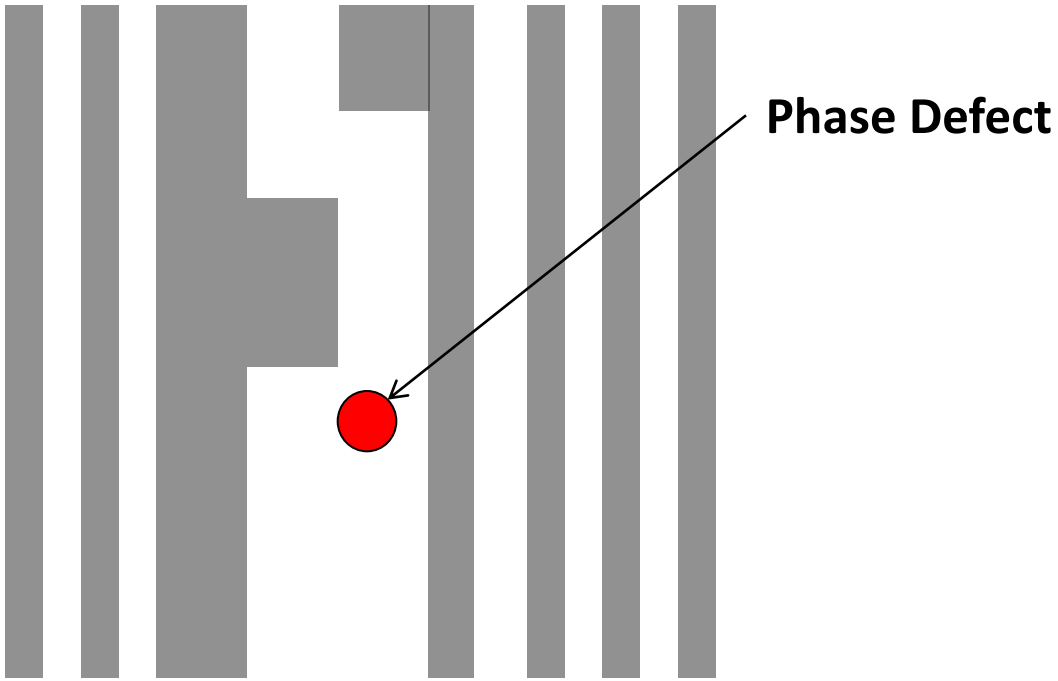
2-2. LTEM-ML blank defect trend @50nm SiO2

- This is the updated defect trend of the LTEM-ML blank (LTEM substrate flatness <150nm). "NEW CHAMPION" defect density is 0.12/cm2 (21defects/plate) at 50nm SiO2 w/M7360. The defect density at yield XX% has also been continuously decreased.



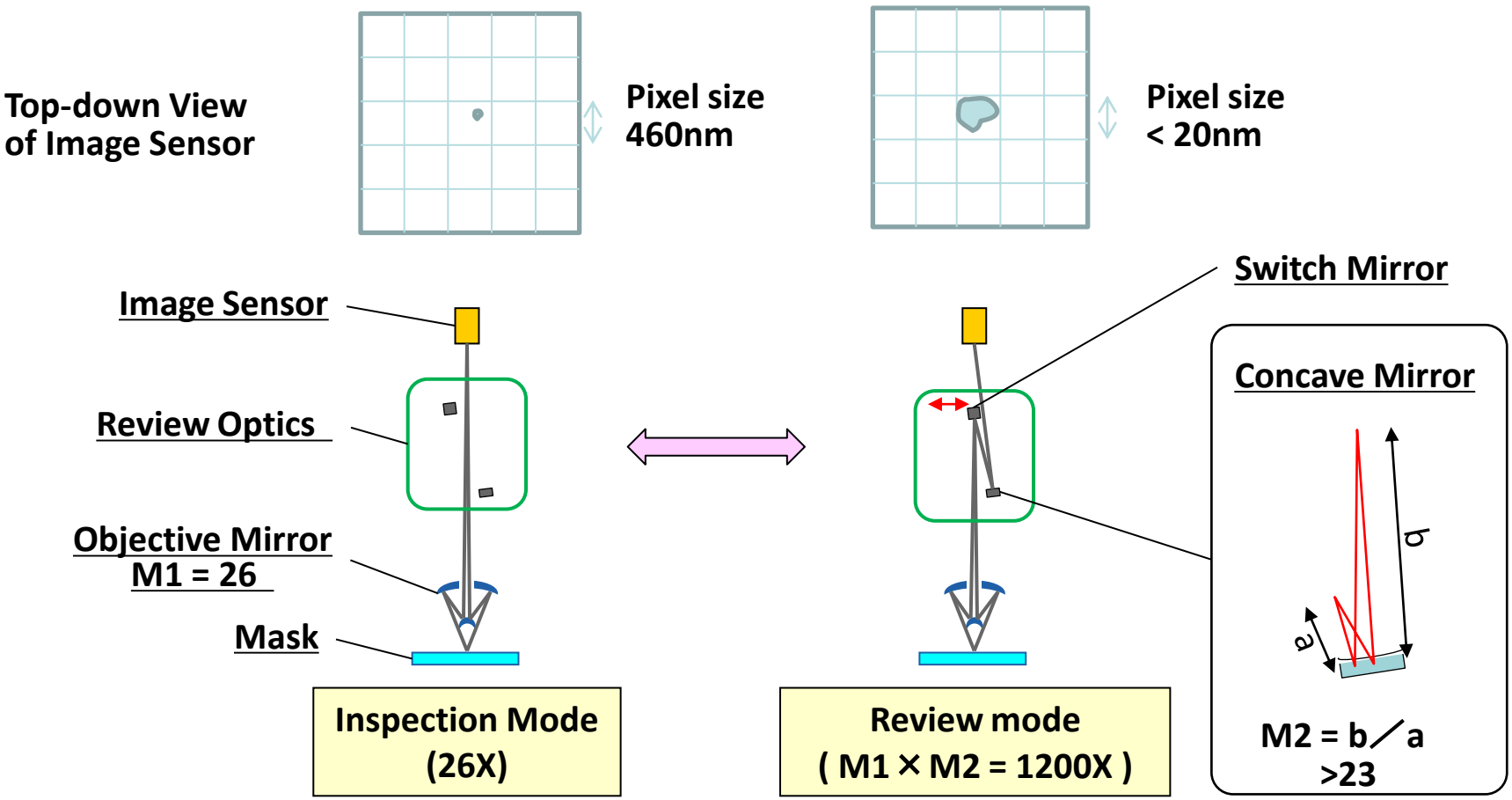
* Courtesy : Intel for M7360 inspection

Requirement: Defect Hiding Process



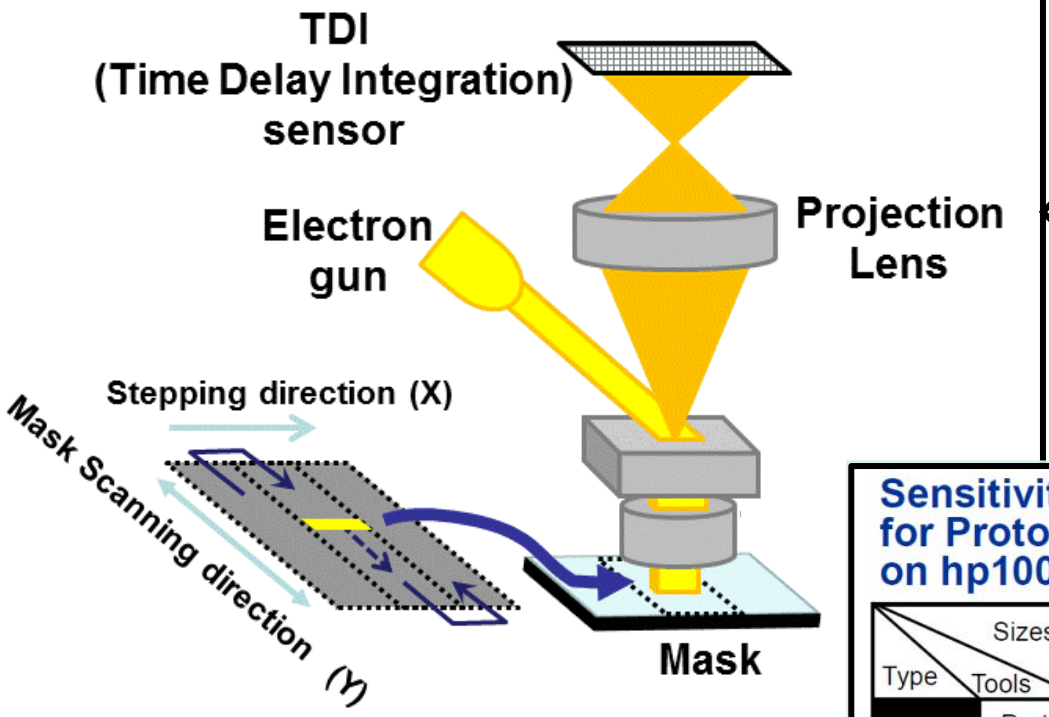
- ✓ It takes a long time to achieve perfect blanks (no phase defect) with high yield.
- ✓ Industry requires to identify precise location of phase defects to mitigate them by shifting patterns and hiding them.

New Feature: Defect Review Mode



✓ Review optics enables to demagnify the corresponding pixel size of image sensor on wafer and to identify the position of phase defect with higher accuracy.

Patterned Mask Inspector (PMI) with EB Projection Optics



Basic Concept

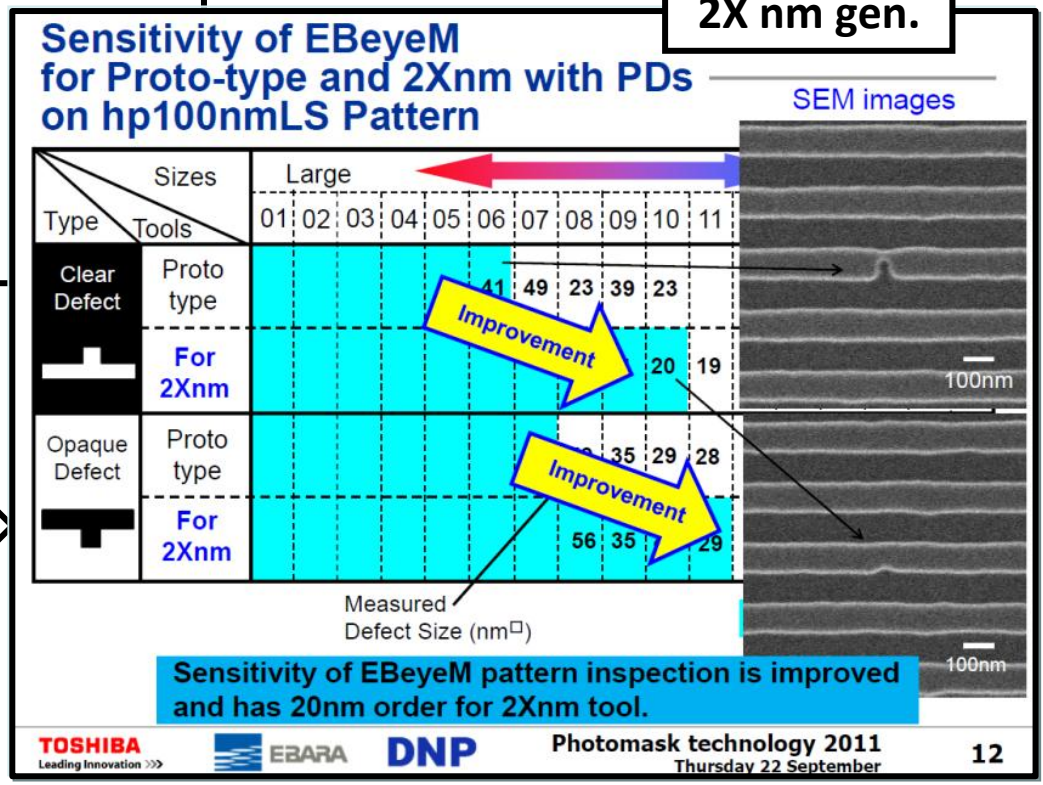
- EB Projection Optics
- High Resolution
- High Throughput

Previous Generation

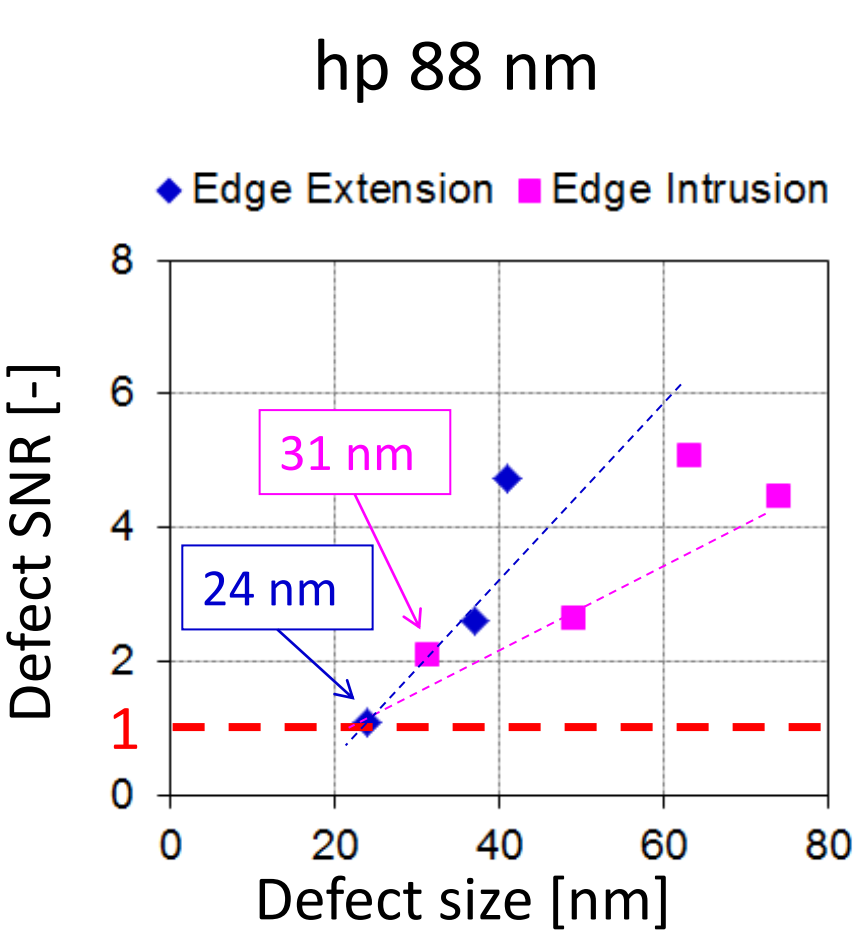
- Program Defect Mask
- Sensitivity: < 30nm

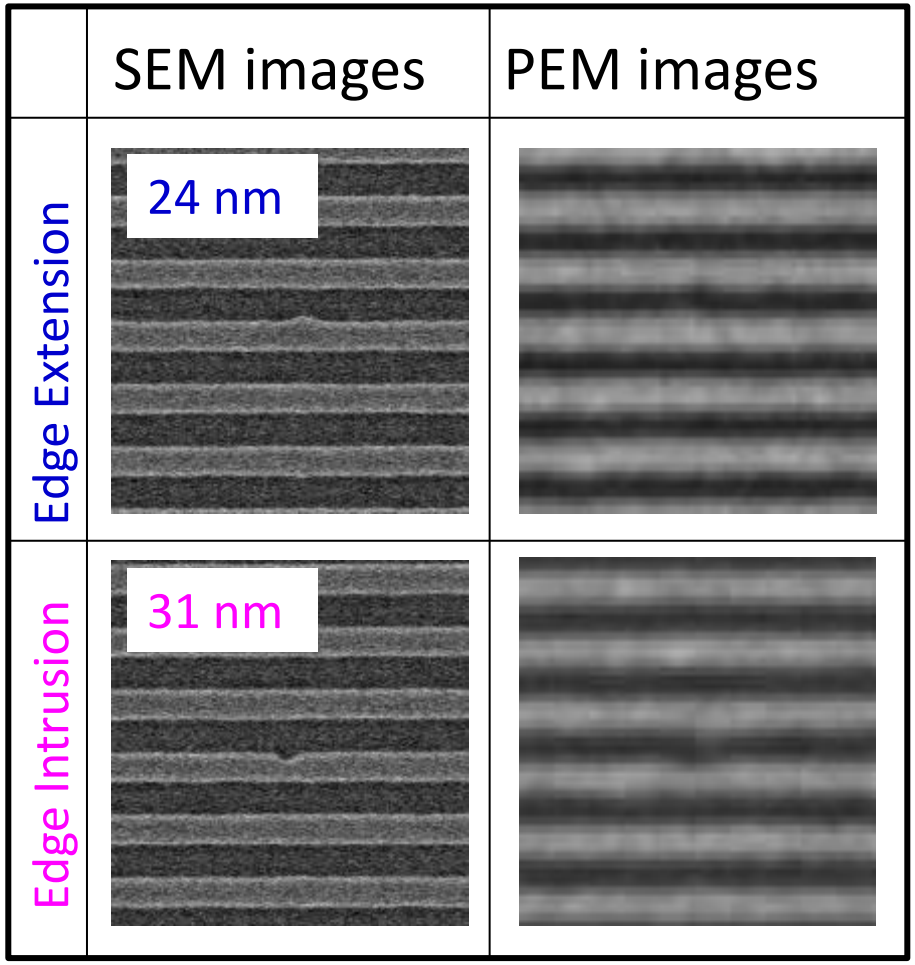
S. Yamaguchi, et al., Proc. of SPIE
Vol. 8166 81662F-1 (2011)

2X nm gen.



Signal-to-Noise Ratio of Defect





The 24 nm-sized edge extension defect was successfully identified

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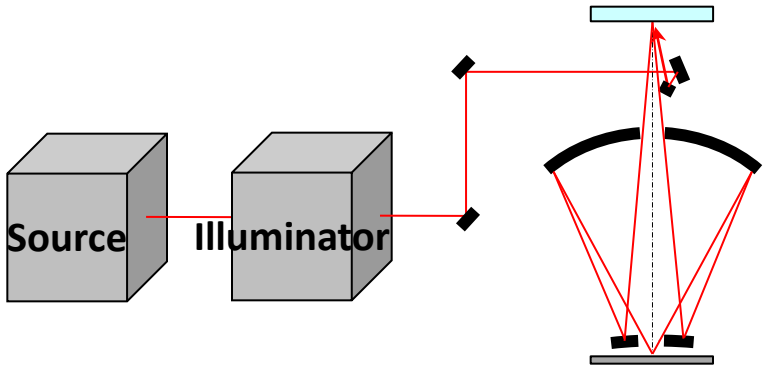
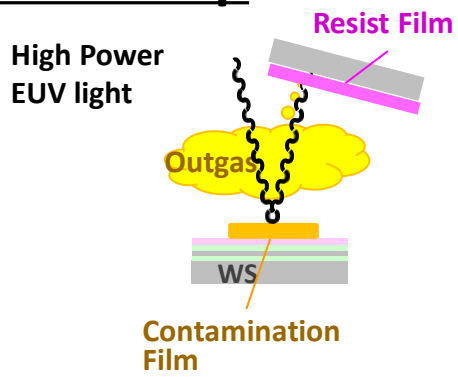
Metric & Infrastructure for Resist Development

Infrastructure

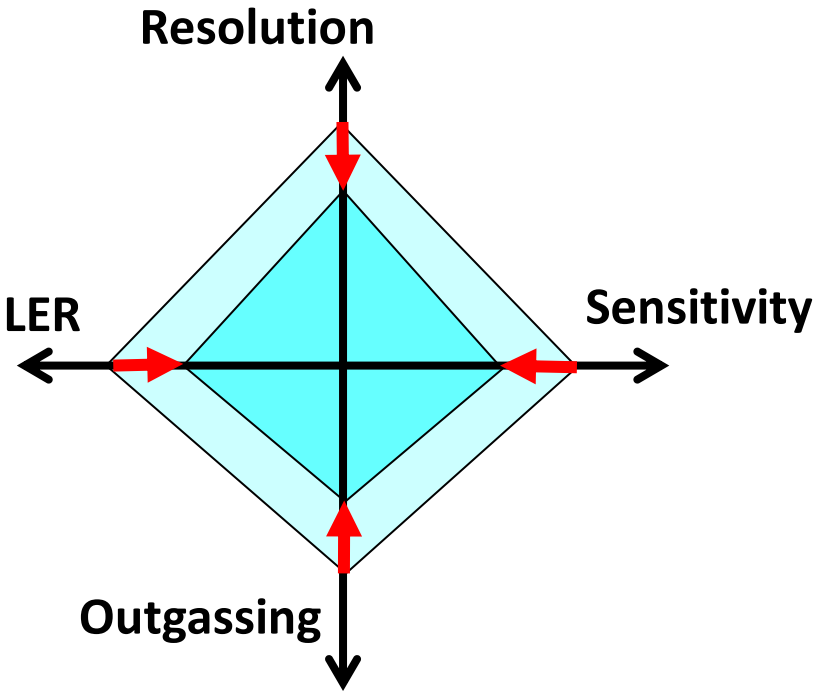
SFET



Outgas Test Setup

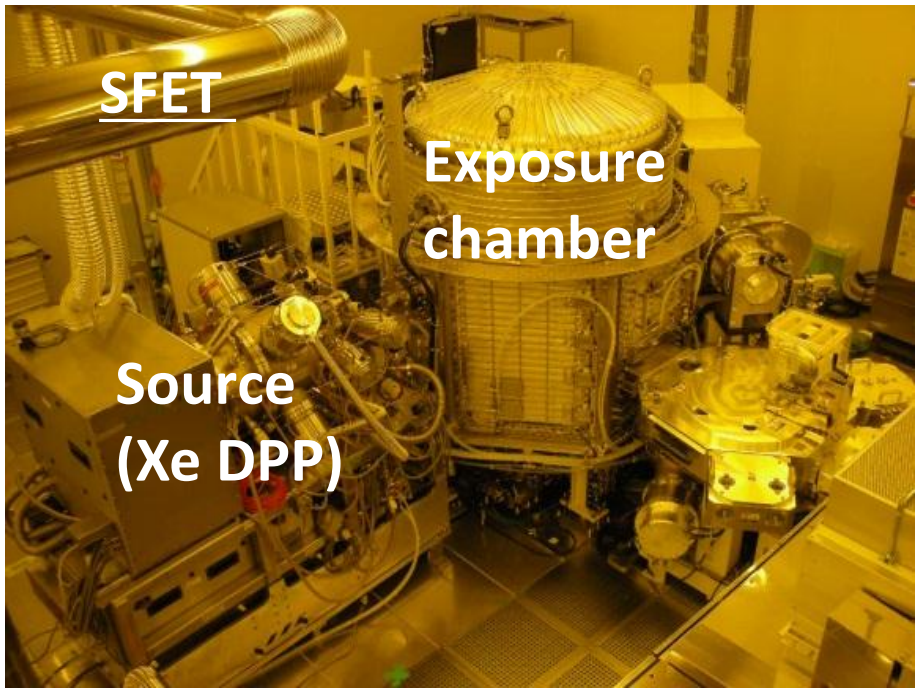


Resist Development

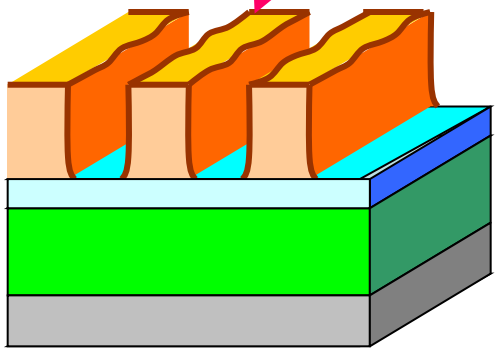


All performance improvement are necessary

Small Field Exposure Tool: SFET



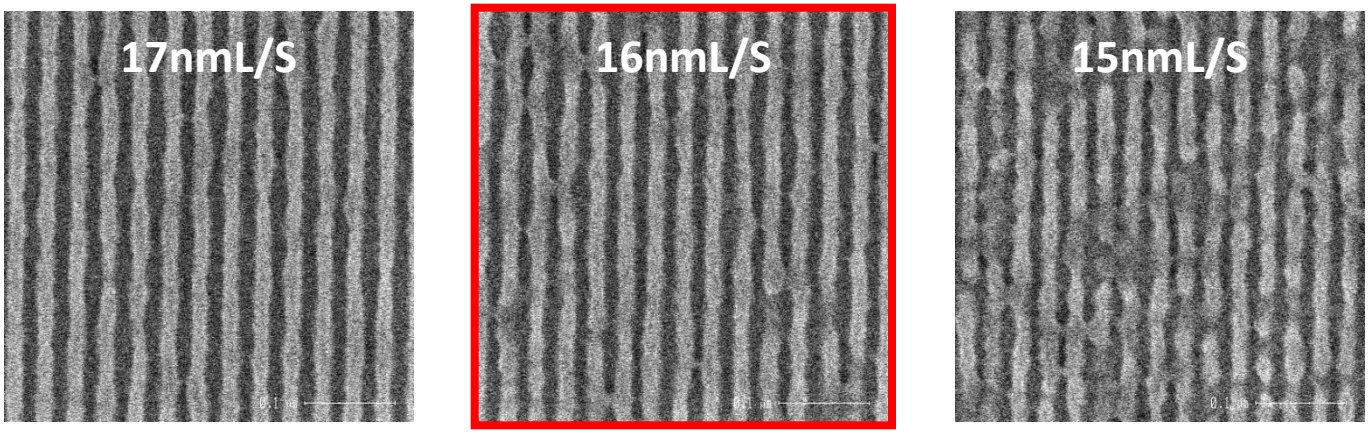
- Resolution ＜ 20nmHP
- Sensitivity < 10mJ/cm^2
- LER < 2nm
- Low Outgassing



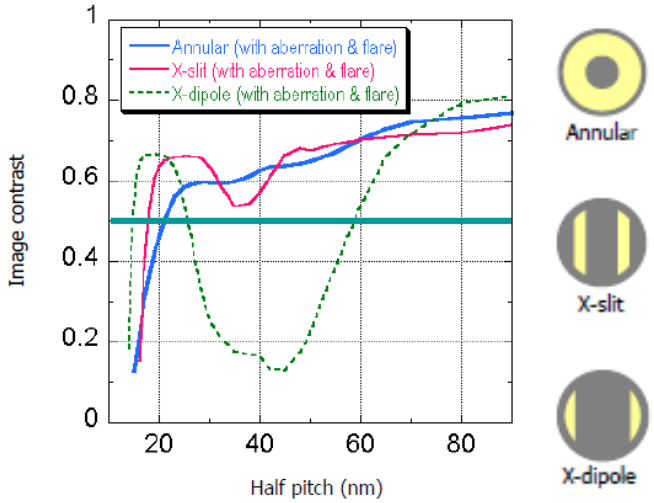
Items	Spec
NA	0.3
Field size: mm	0.2 x 0.6
Magnification	1/5
Source power	0.5W @IF

Ultimate Resolution (Aggressive Dipole Illum.)

16nm L/S was resolved.



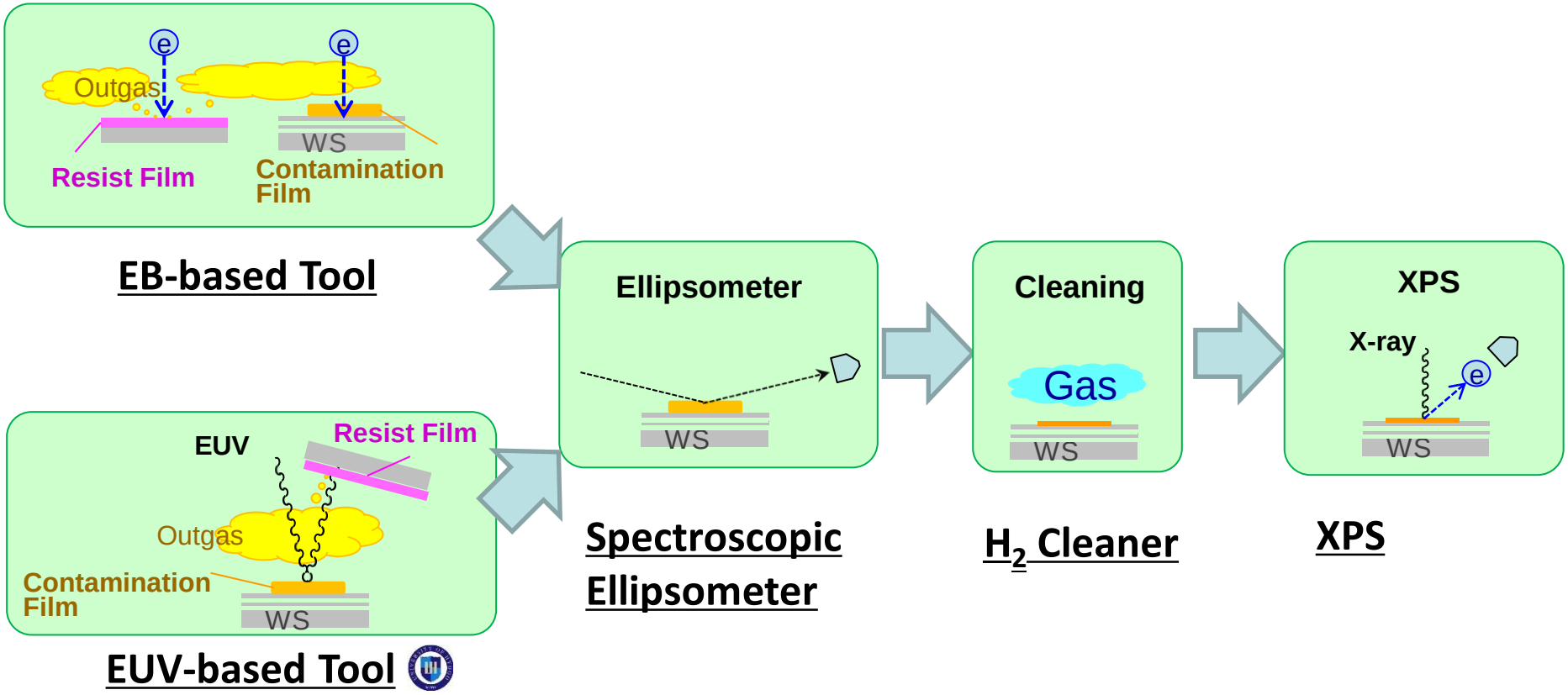
Exposure		
Tool	:	**Canon SFET**
NA	:	**0.3**
Illumination	:	**X-dipole**
Track	:	**TEL ACT12**
Evaluation		
SEM	:	**Hitachi CG4000**
Resist	:	**35nm Thickness**



Proc. of SPIE Vol. 7696 79690Q-6

N. Sugie, et al., presented at The 21st Research Group on Polymers for Microelectronics and Photonics, No.1 (2012).

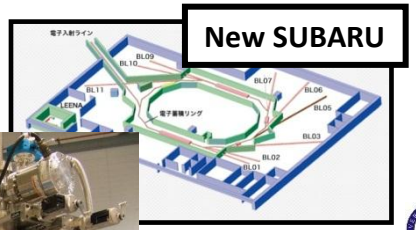
Outgas Evaluation Procedure

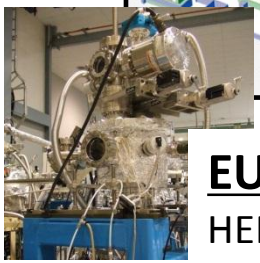


- ✓ Outgassing from resist material generates contamination film on WS.
- ✓ The outgas amount for cleanable (carbon) components is quantified by measuring the thickness of the contamination film.
- ✓ Non-cleanable components can be characterized by XPS after cleaning the carbon contaminant by H_2 radical.

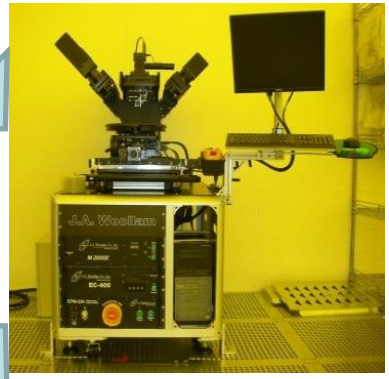
Outgas Evaluation Infrastructure in EIDEC

EB-based Tool
EUVOM-9000 (LTJ)

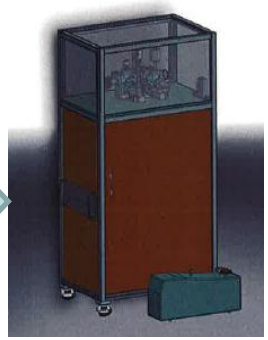




EUV-based Tool
HERC (Univ. of Hyogo)



Spectroscopic Ellipsometer
M-2000X
(J.A.Woollam)

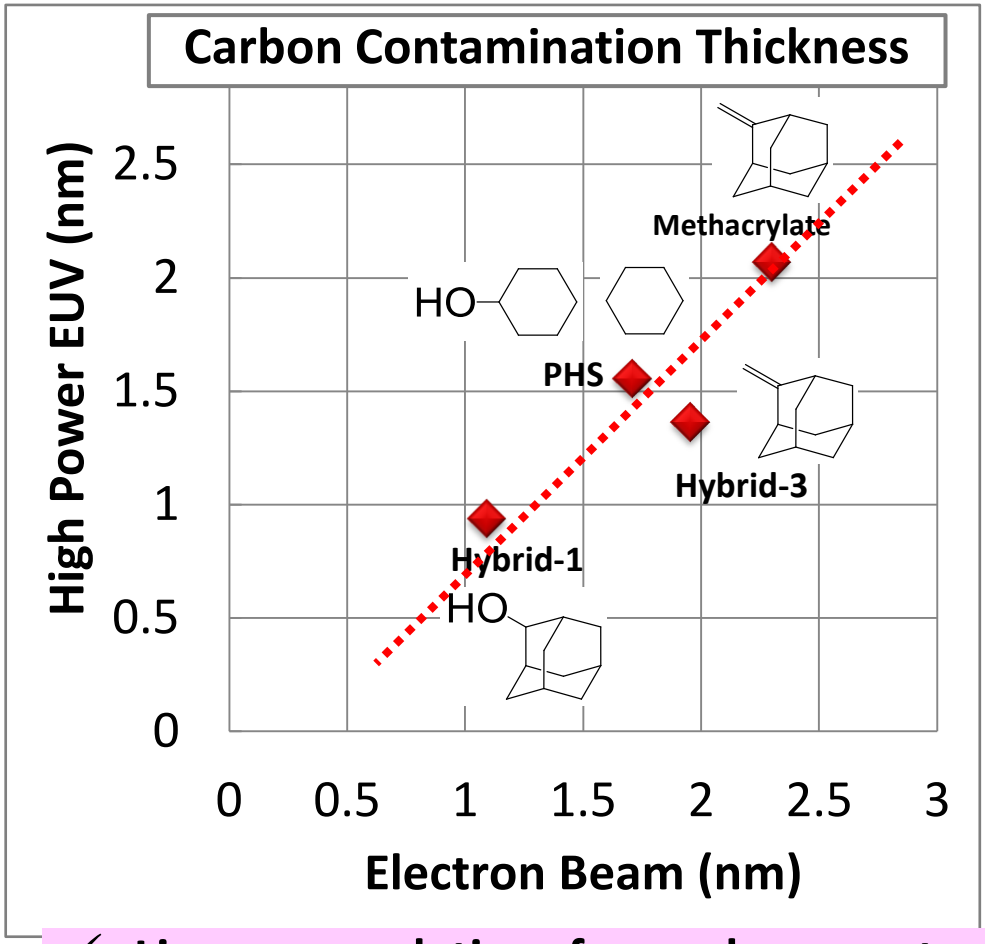


H_2 Cleaner
(EUVT)

XPS
Versa Probe Ⅱ
(ULVAC PHI)

- ✓ **EB-based Outgas Evaluation Tool has been installed in Mar. 2012.**
- ✓ **EUV-based Tool also has been installed as a reference of EB-based tool.**
- ✓ **The metrology tools, i.e. Spectroscopic Ellipsometer (SE) and XPS, was certificated by exposure tool supplier.**

Carbon Contamination



Platform	De-protected Group
Methacrylate	
Hybrid-3	
PHS	
Hybrid-1	

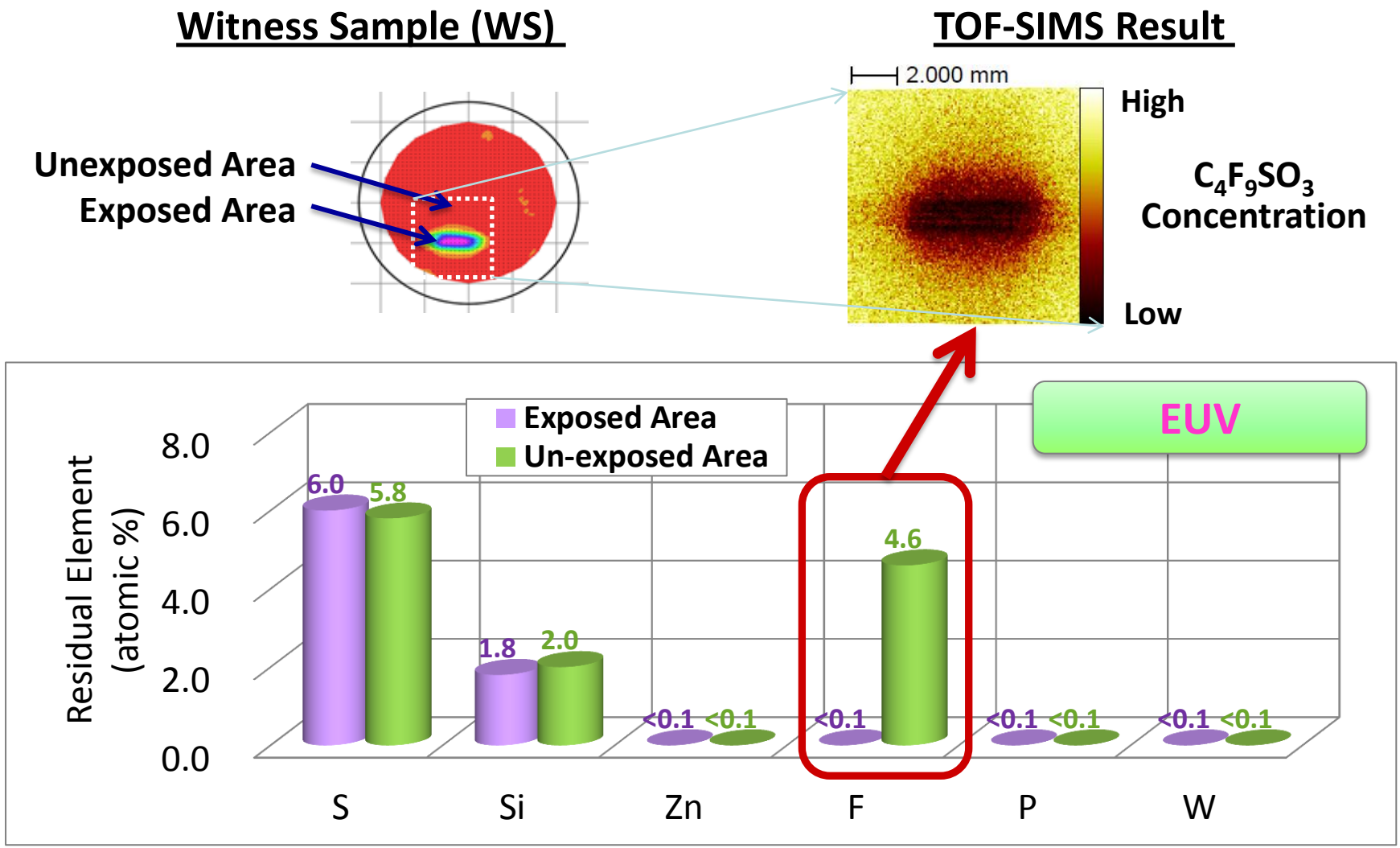
Weak

Polarity

Strong

- ✓ Linear correlation for carbon contamination between EUV and EB was clearly observed.
- ✓ The carbon contamination was decreasing with increase in degree of polarity of the de-protected groups and polymer platforms. <u>Polarity control</u> is one of the key design parameters to reduce outgassing.

Contamination at Unexposed Area after Cleaning



- ✓ Fluorine was detected by XPS only at unexposed area of EUV sample.
- ✓ TOF-SIMS indicated it was PAG anion compounds outgassed from resist.

Agenda

- Trend of LSI Downscaling
- Lithography Prospect
- Technical Challenge for EUVL
- Role of EIDEC
- Persistent Efforts for Each Technology Development
  - Mask
  - Resist / Process
  - Source / Scanner
- Summary

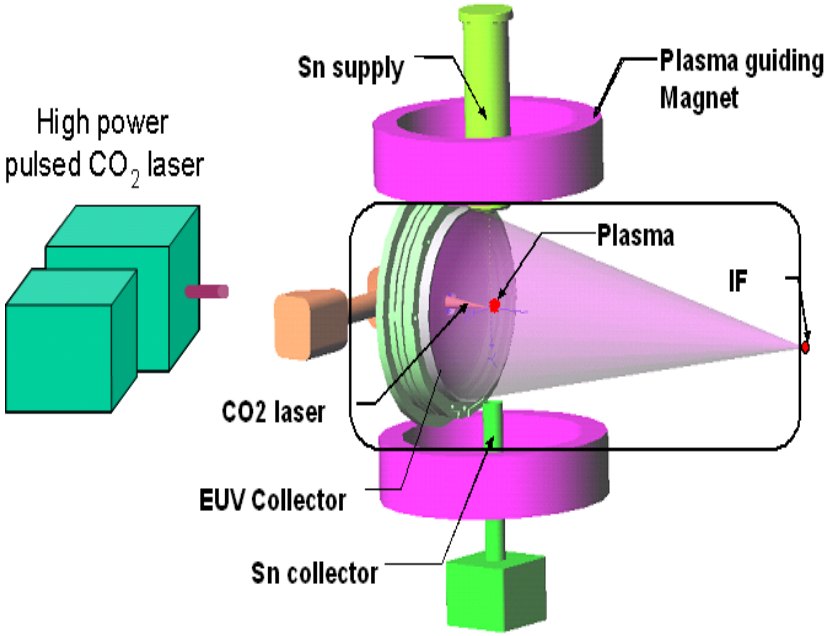
EUV Focus Areas 2006-2010: 22 nm half-pitch insertion target

2007 / 22hp	2008 / 22hp	2009 / 22hp	2010 / 22hp	2011 / 22hp
1. Reliable high power source & collector module	1. Long-term source operation with 100 W at IF and 5MJ/day	1. Mask yield & defect inspection/review infrastructure	1. Mask yield & defect inspection/review infrastructure	1. Long-term reliable source operation with 200 W at IF*
2. Resist resolution, sensitivity & LER met simultaneously	2. Defect free masks through lifecycle & inspection/review infrastructure	2. Long-term reliable source operation with 200 W at IF	1. Long-term reliable source operation with 200 W at IF	2. Mask yield & defect inspection/review infrastructure
3. Availability of defect free mask	3. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously
4. Reticle protection during storage, handling and use	• Reticle protection during storage, handling and use	• EUVL manufacturing integration	• EUVL manufacturing integration	• EUVL manufacturing integration
5. Projection and illuminator optics quality & lifetime	• Projection / illuminator optics and mask lifetime			

*) *This requires a 20 X improvement from current source power status*

HVM introduction in late 2013 if productivity challenge can be met

EUV Light Source

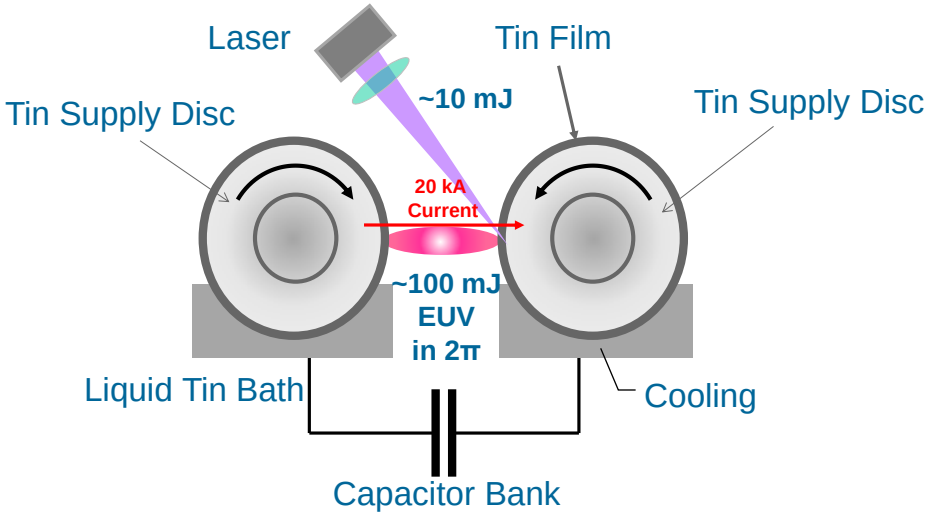


EUVA/Komatsu/GIGAPHOTON

LDP: Discharge Produced Plasma

Laser Assisted Trigger

Rotating Electrodes for Heat Dissipation



EUVA/USHIO/XTREME

LPP: Laser Produced Plasma

CO_2 Laser with Pre-Pulse

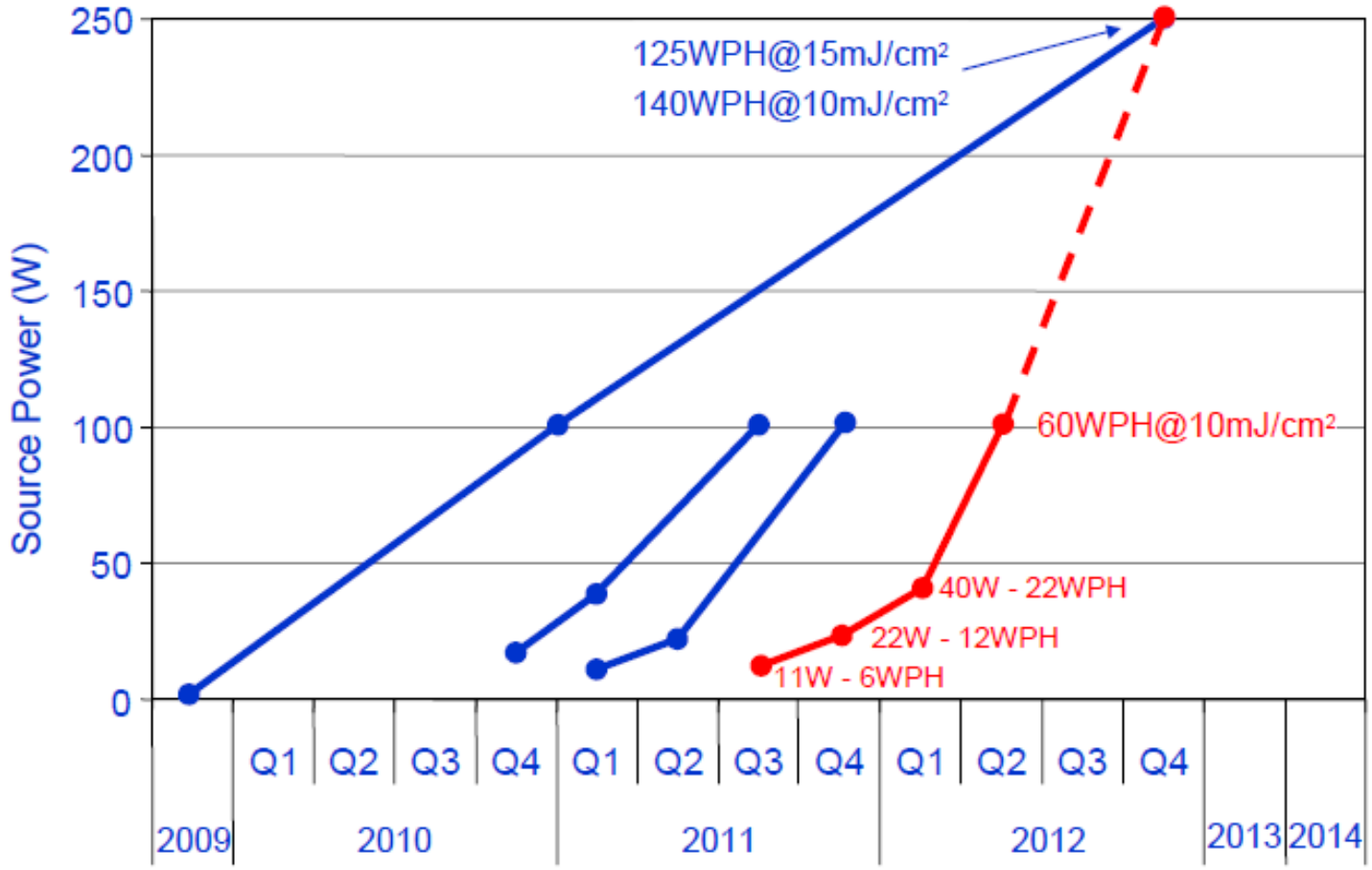
Debris Mitigation

Magnetic Field (Gigaphoton)

Gas curtain (Cymer)

Courtesy of Dr. Shinji Okazaki

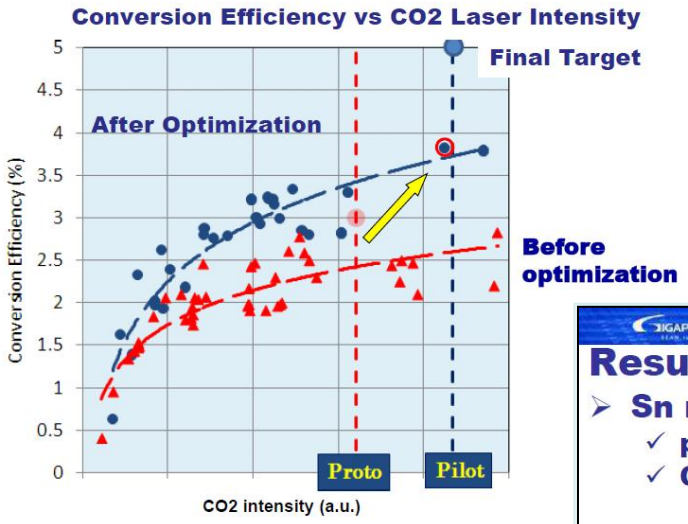
Challenges in Delivering Source Power

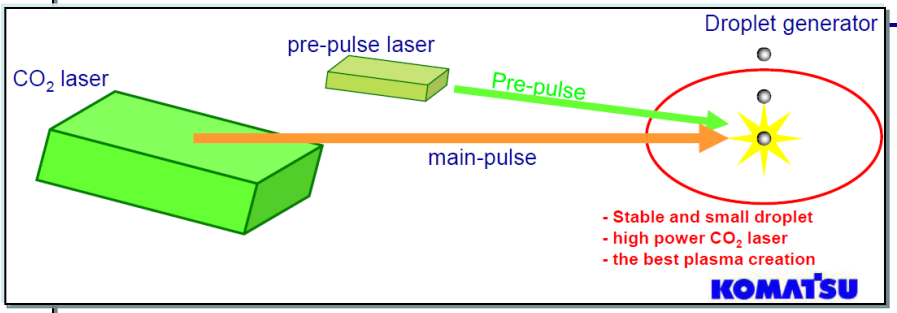


Tony Yen, "EUV Lithography for High-Volume Manufacturing Progress and Challenges," EUVL Symposium Oct. 2011

New champion data of CE = 3.8% (Aug.2011)

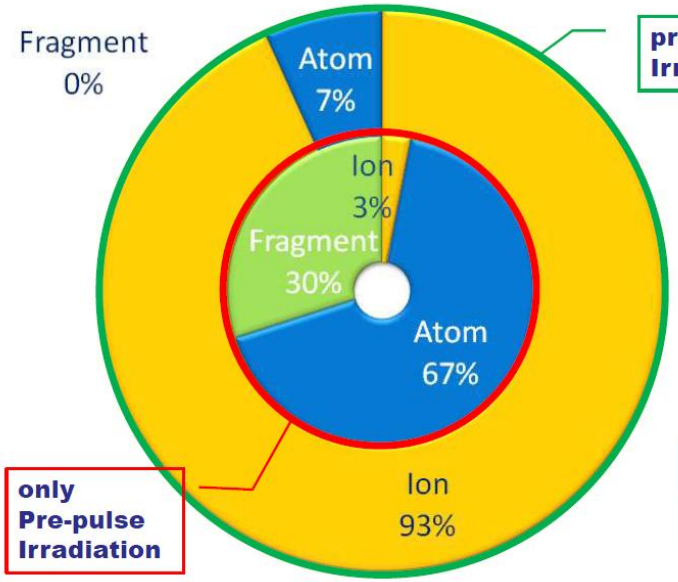
- After CE optimization
  - ✓ 3.3% → 3.8% (@ pilot condition)





Results Summary

- Sn molecule measurement results
  - ✓ pre-pulse laser + CO2 laser irradiation : ionized 93% of Sn
  - ✓ Only pre-pulse laser irradiation : ionized 3% of Sn



Experimental Condition: Same as proto machine

		This time	Proto Condition
Repetition rate	Hz	10	100k

KOMATSU

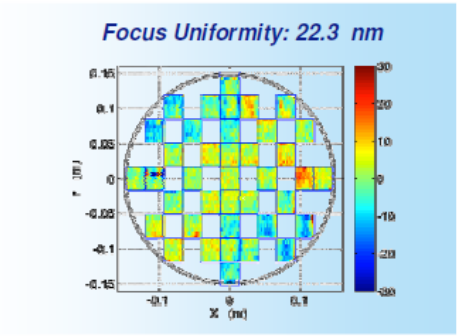
GR11-241 2011 EUVL symposium P17

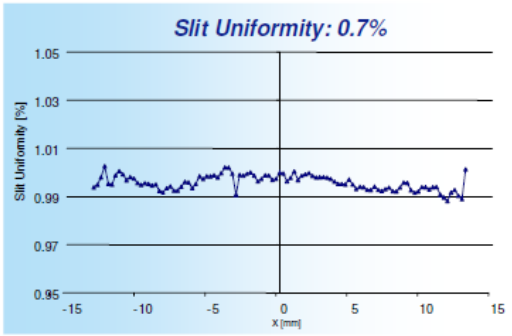
Effect of Pre-pulse laser

→ CE improvement
→ Effective debris mitigation

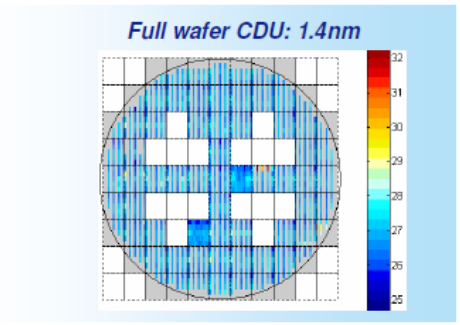
Junichi Fujimoto et.al, "Development of LPP-EUV source for HVM EUVL," EUVL Symposium Oct. 2011

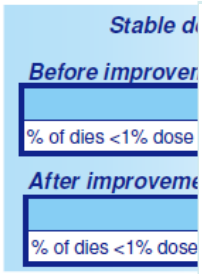
NXE:3100 sub-system performance meets design targets and supports sub-27 nm imaging





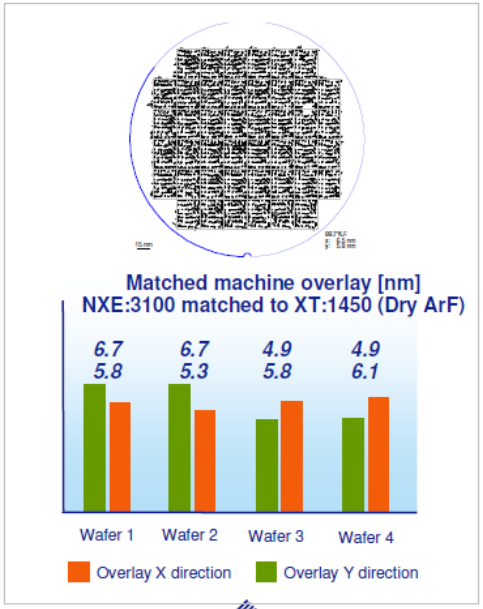
- ✓ The scanner supplier has already shipped 6 tools.
- ✓ Basic performance, i.e. CD, OL has been validated.





Slide 11 | Public

NXE:3100 overlay ready to support process development



Slide 17 | Public

ASML

Rudy Peeters, "EUV lithography: NXE:3100 is in use at customer sites and building of NXE:3300B has started," EUVL Symposium Oct. 2011

Status, Target & Persistent Effort

Core Element 0 Score 10	Current Status	Target	Persistent Effort
Source	~10W @IF	250W @IF	- Laser stability - Droplet generator stability - Debris mitigation - OoB reduction
Scanner	- NXE3100 / CDU: 1.4nm, DCOL: <1nm	Place NA0.33 to market in 2013	- Productivity
Mask	- ϕ-defect : 20-30/plate (>50nm) - Particle:	Ideally : 0	- ϕ-defect mitigation - To establish ABI - Handling/cleaning/pellicle
Resist/Process	- Resolution:16nm - Sensitivity : 30~mJ/cm^2 - LWR : ~ 5 nm	- 11nm - 10mJ/cm^2 - ~ 1.1 nm	- Thinner resist thickness - Hardmask process, bias control - LWR: build up consensus
Litho Integration	Small experience	Ready for HVM	Learn more - Defectivity - Total CD control - Total OL control

Summary

- ✓ **Downscaling of LSI still makes sense for the cost reduction, performance improvement and power consumption.**
- ✓ **EUV lithography will be the main stream technology from cost and extendibility viewpoint.**
- ✓ **However, some key technologies still have fundamental issues. Persistent efforts are necessary to overcome the challenge for realizing EUVL.**
- ✓ **The source no doubt needs to increase in power dramatically and reach the set targets (main & pre-pulse laser, debris mitigation, droplet generation, IR reduction) with sufficient stability.**
- ✓ **The development of EUVL infrastructure, i.e. mask inspection, resist, etc. in consortia is a reasonable approach for reducing cost of pre-competitive technology development.**
- ✓ **The persistent efforts including the EUVL infrastructure development will definitely ensure the realization of EUV lithography.**

Acknowledgement

The part of this work was supported by New Energy and Industrial Technology Development Organization (NEDO).

Thank you for your attention !!