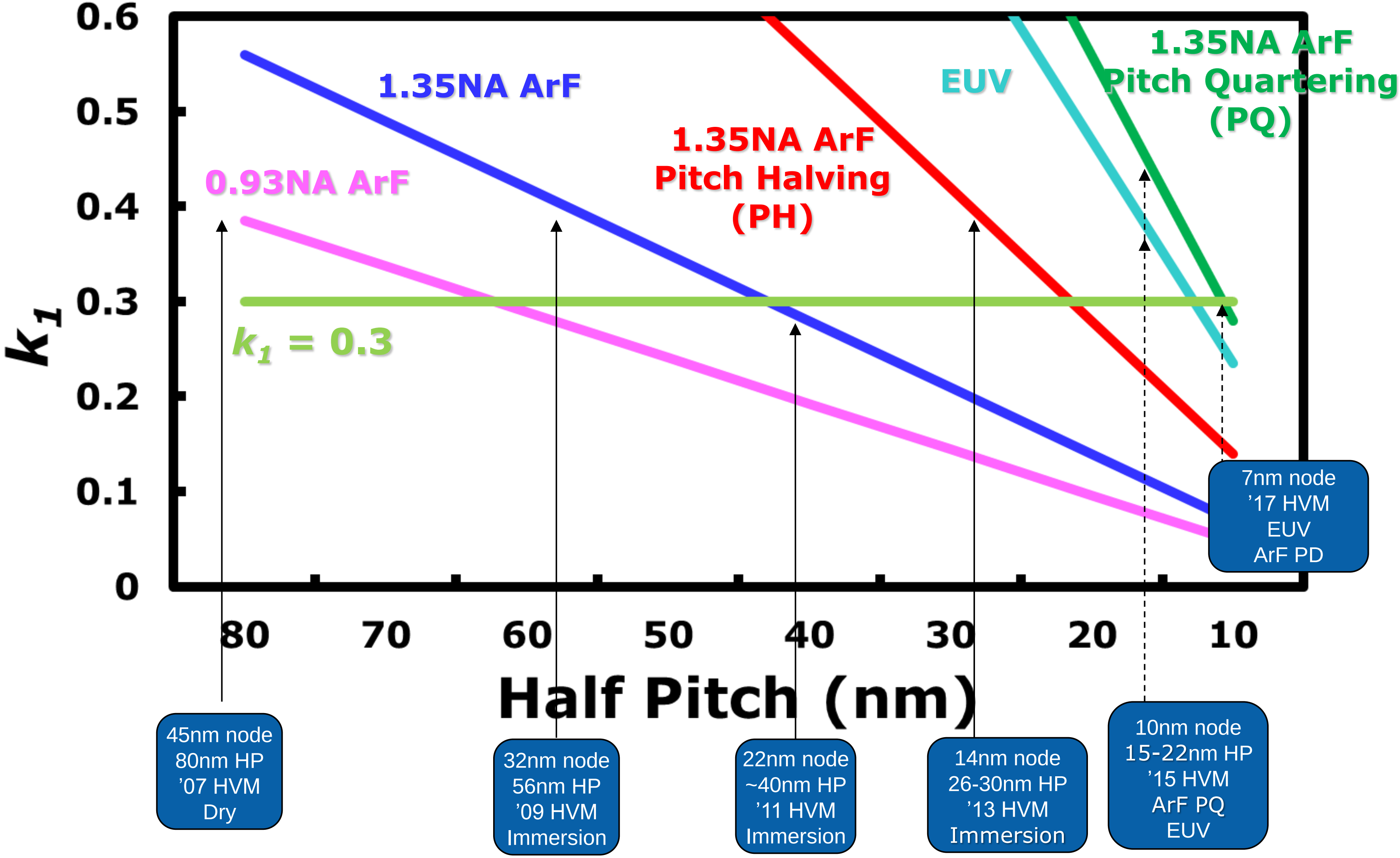
EUV: From Development to HVM

Sam Sivakumar

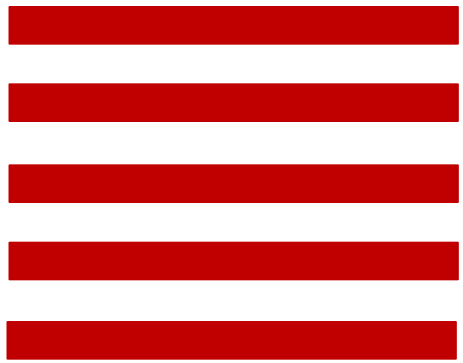
Intel Corporation

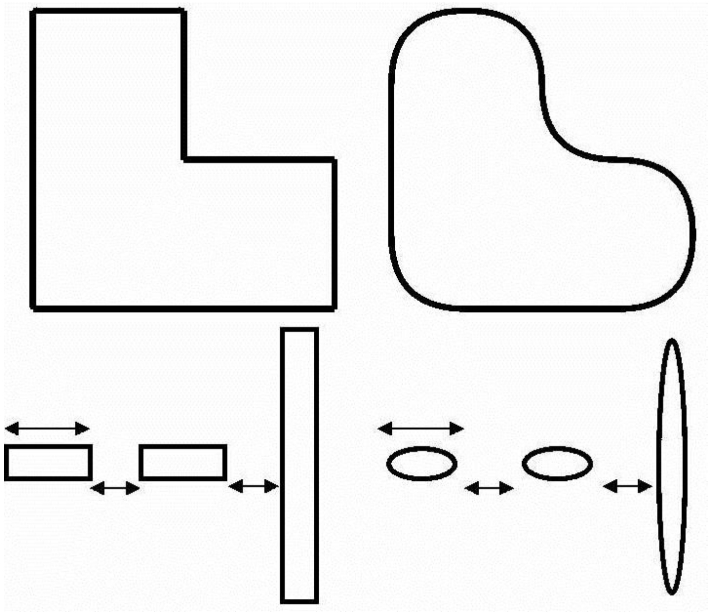
The Litho Landscape



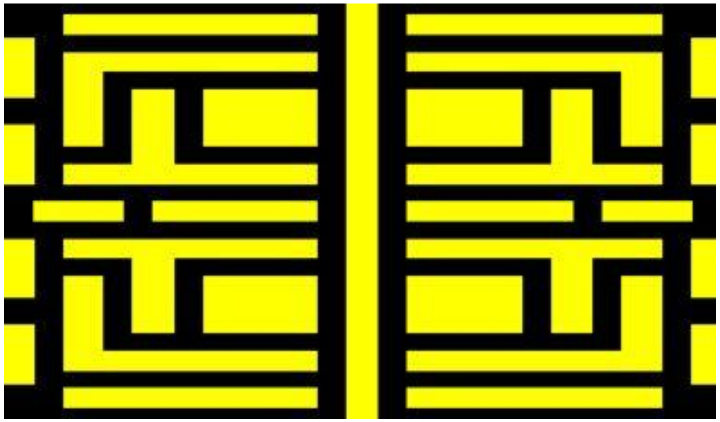
The Real Scaling Challenge

Ideal Layout



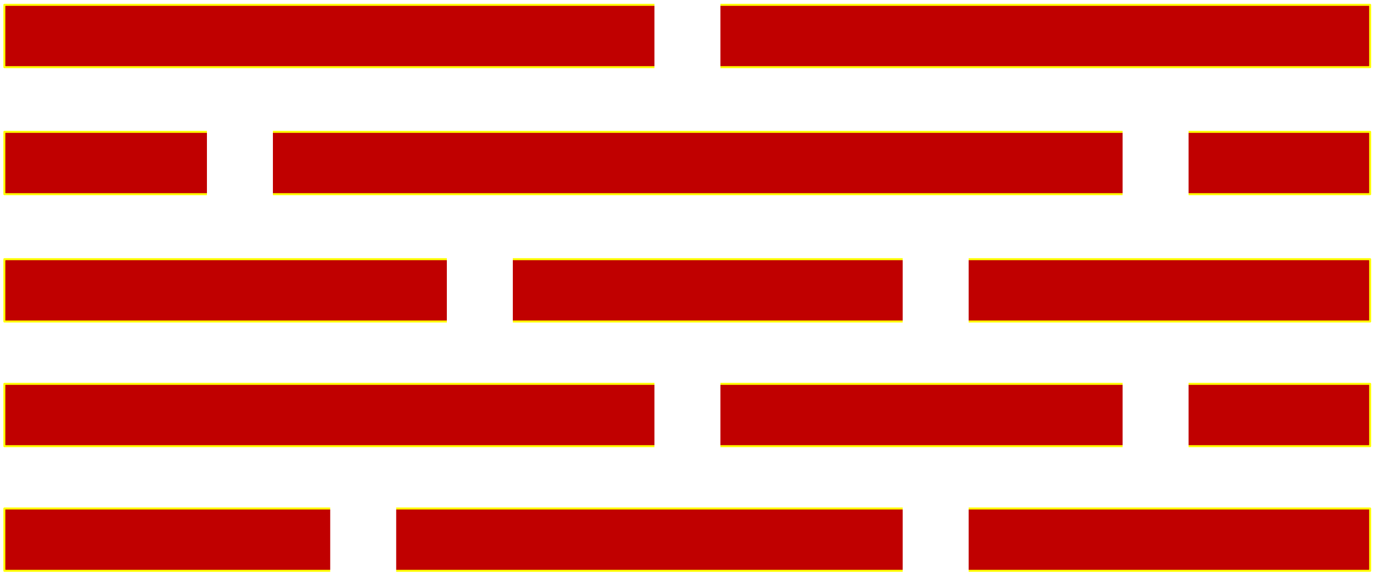


Real Layout



1D Structures Scale Well…. 2D Structures Don't

Grating and Cut

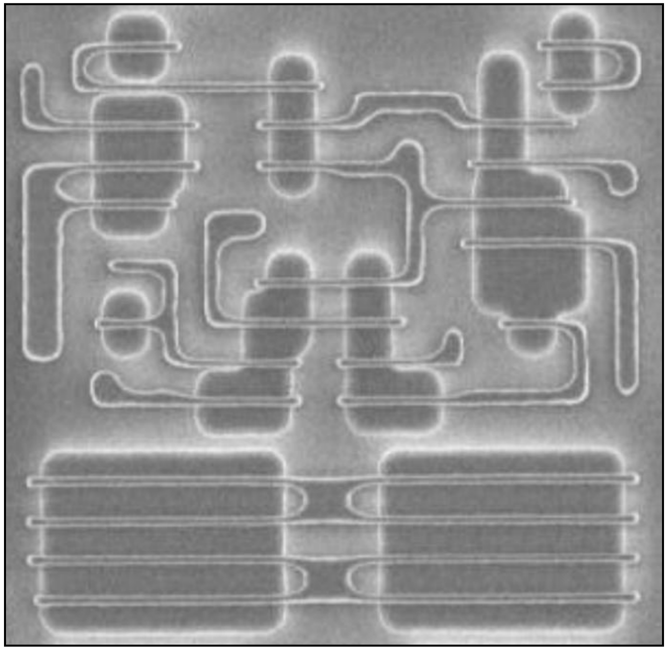


1.Print Grating
2.Cut Grating

Two fundamentally different patterning challenges

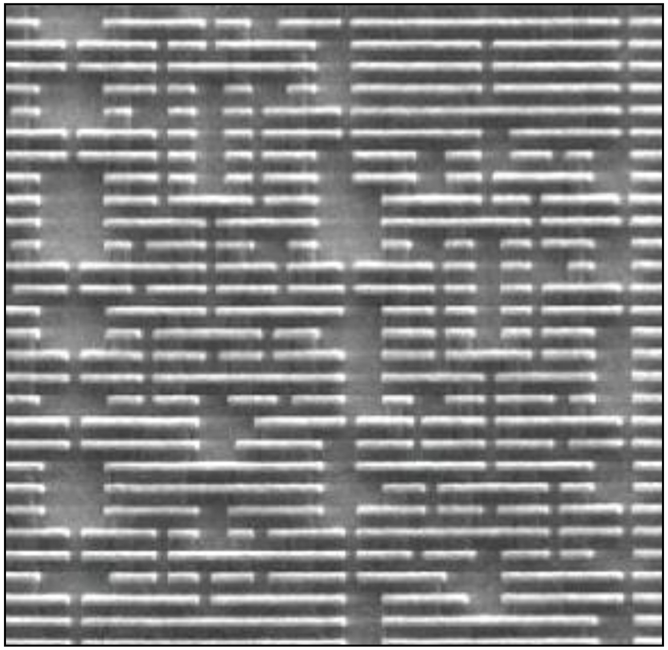
Gridded Unidirectional Layouts

65 nm Layout Style



- Bi-directional features
- Varied gate dimensions
- Varied pitches

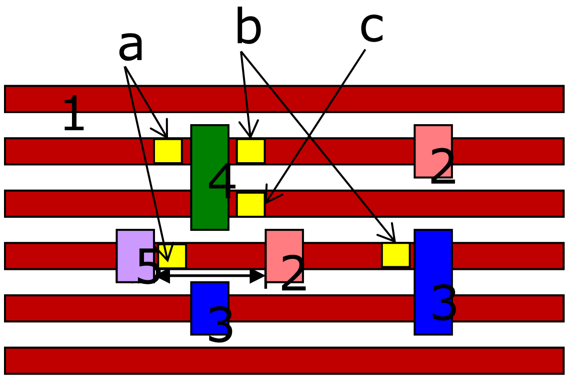
45 nm Layout Style



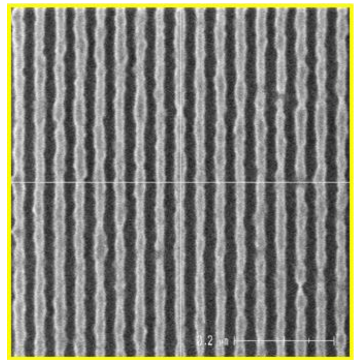
- Uni-directional features
- Uniform gate dimension
- Gridded layout

Standard now, density neutral or better

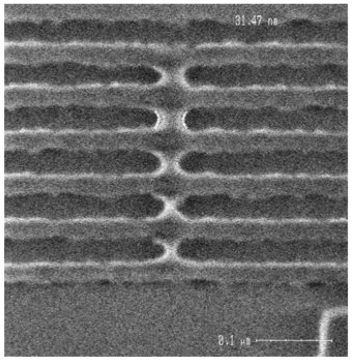
Likely EUV Use Scenario



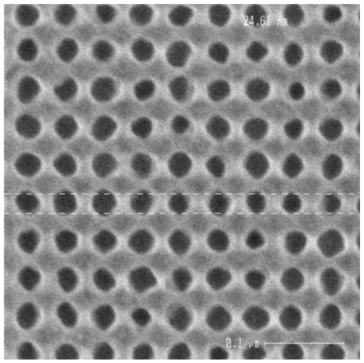
ArF MP



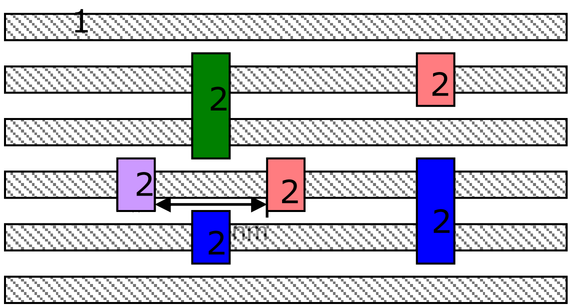
L/S



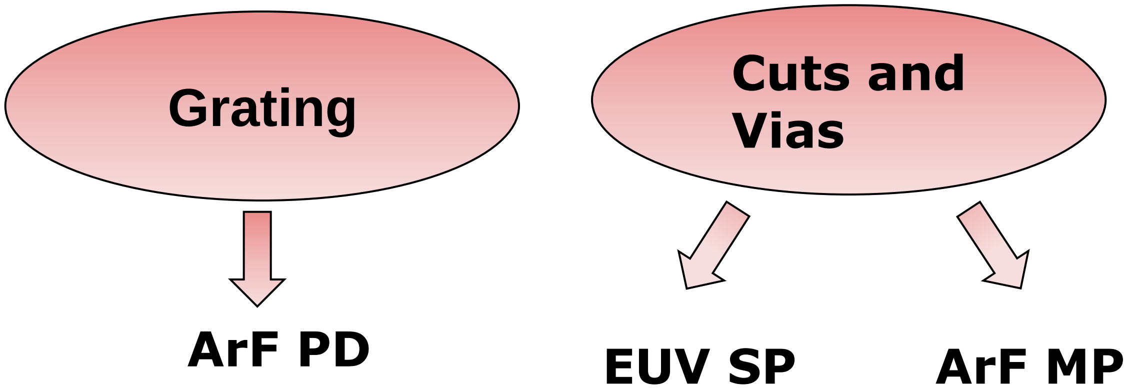
ETE



C/H



EUV



EUV offers the best value as a replacement of ArF multi-pass cut/via layers

The Challenges of EUV

Resists

- Patterning requirements...
  - Resolution
  - LWR/Dose
- Outgassing
  - IDM TPT requirements
  - Scanner outgassing requirements

Tool

- Source
  - Availability
  - Power
- Scanner
- Hardware

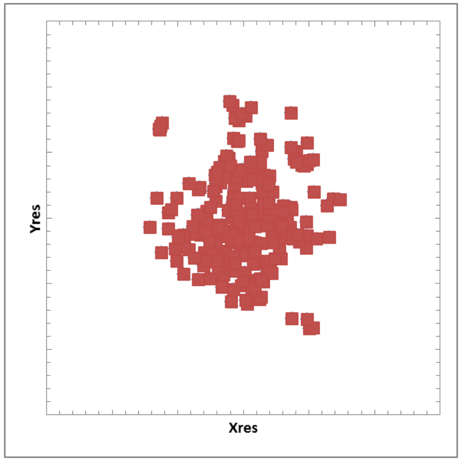
Reticle

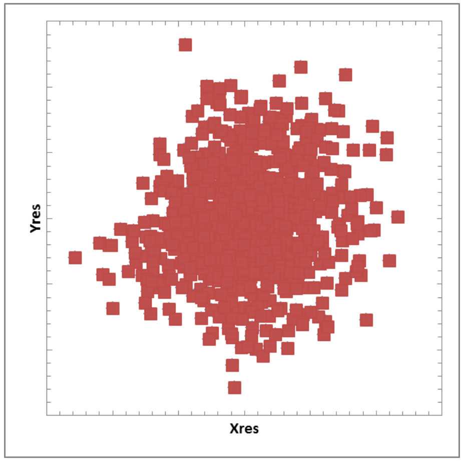
- Defectivity
  - Killer defect impact >> wafer process defect impact
  - Mitigation strategies
    - Reticle inspection
    - Patterned wafer inspection
    - Alternative strategies

EUV HVM implementation depends on satisfactory progress on all these fronts!

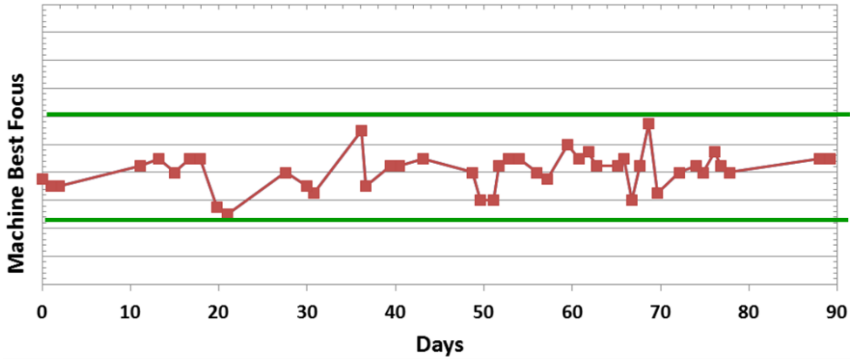
Scanner/Track Performance

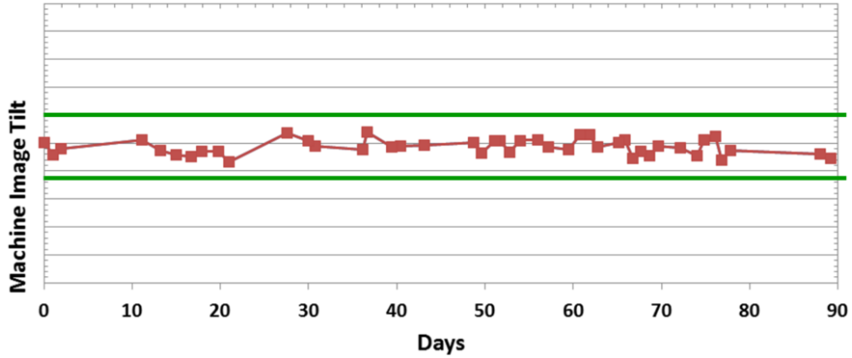
NXE Overlay Residuals





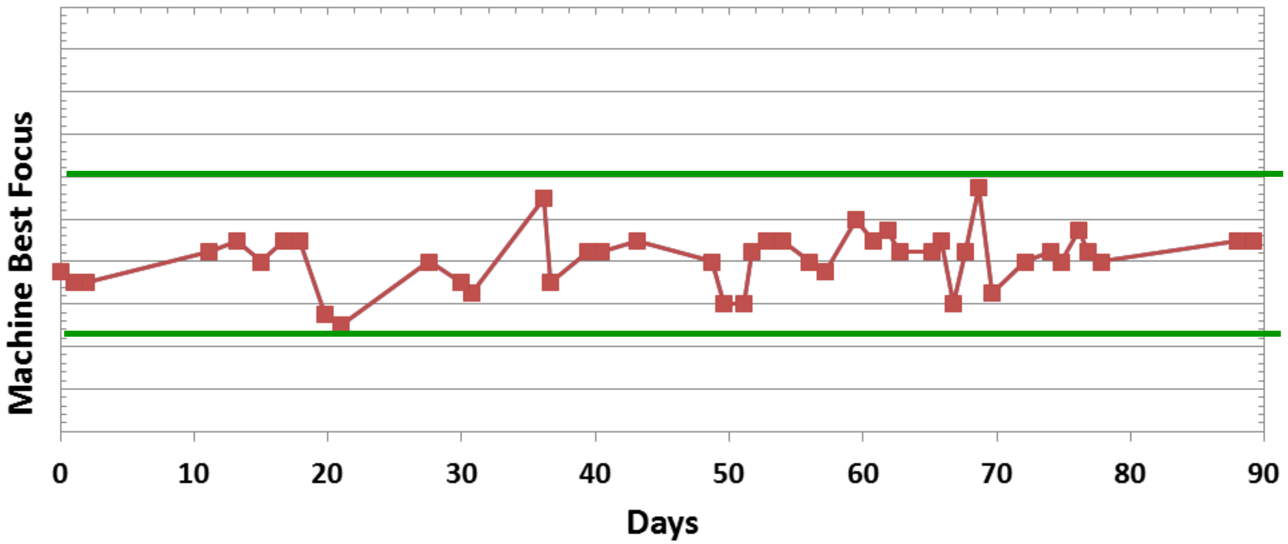
NXT:NXE MMO **NXT:NXT MMO**

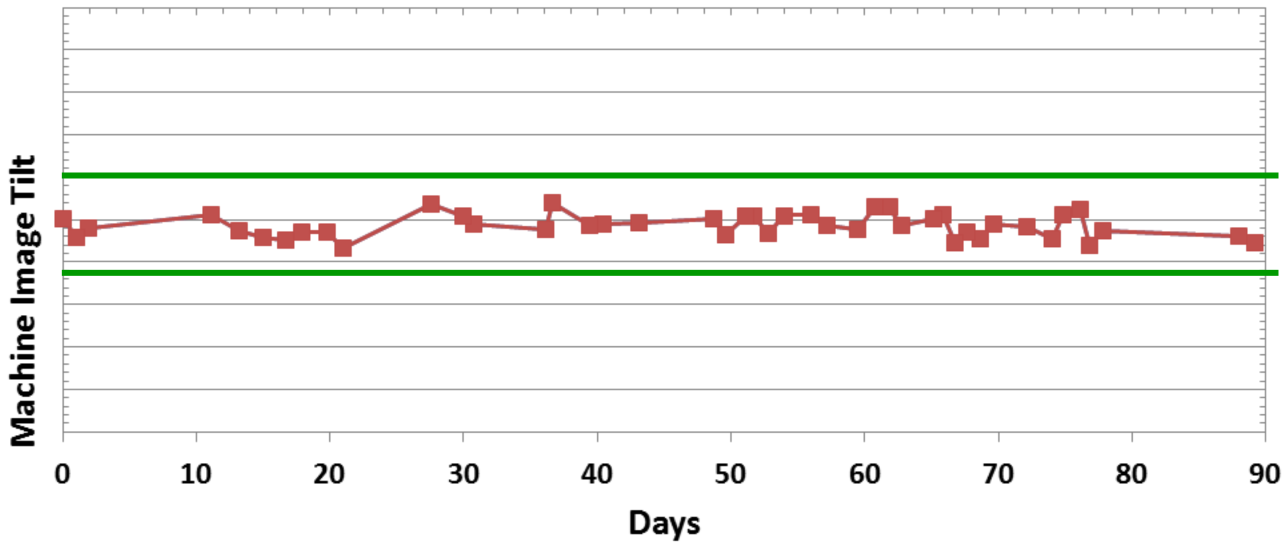




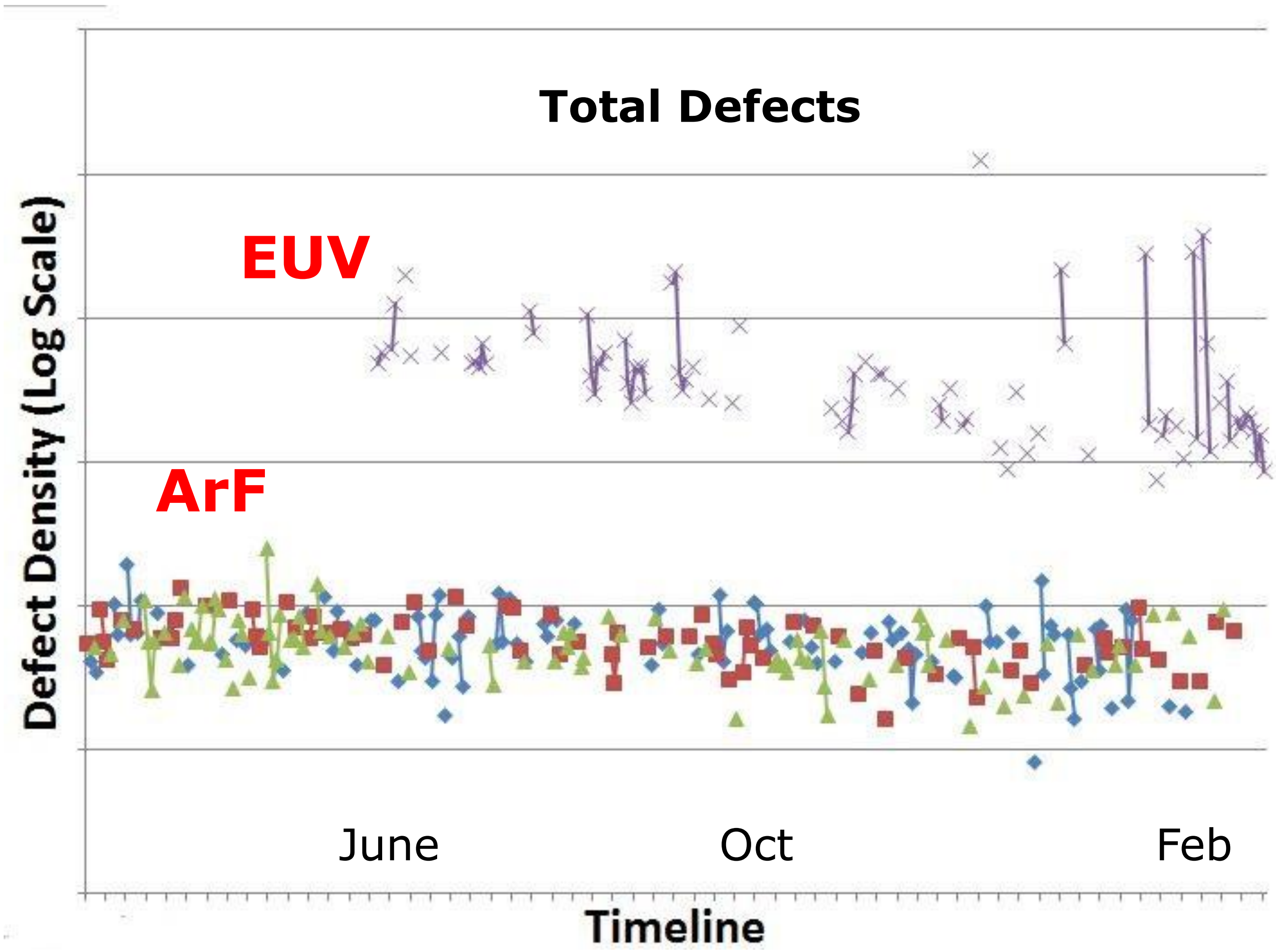
NXT aligned to NXE overlay and NXE focus and tilt performance are well within ArF baseline distribution

Focus and Tilt Performance

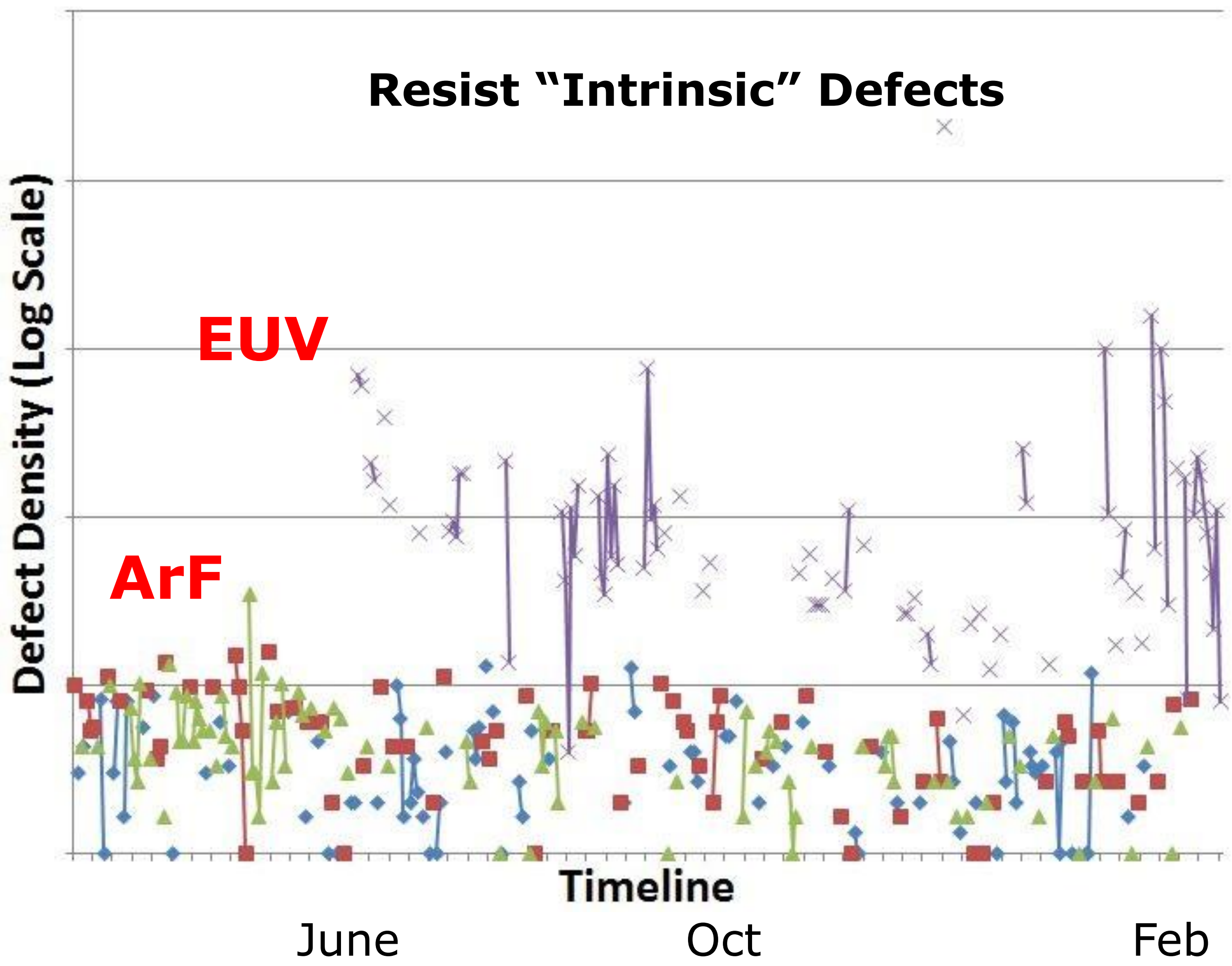




Scanner/Track Defectivity



Scanner/Track Defectivity



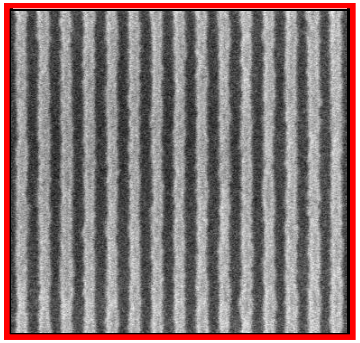
Scanner/Track Hardware Summary

- Basic tool hardware performance appears to be more or less in line with ArF baseline
  - Overlay and focus performance appear to be as expected
- Overlay performance of EUV systems appear to be roughly in line with ArF mix-match baseline
  - Further improvements likely with better characterization of reticle components and other EUV-specific effects
- Significant improvement made in linked defect performance
  - Current performance still lags ArF but within striking range
  - Residual defects appear to be largely resist related

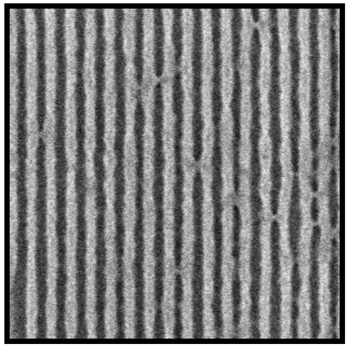
Resist Performance

Resist Resolution

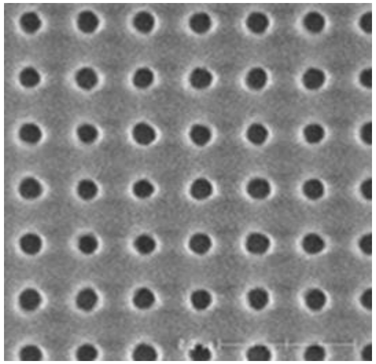
CA Resist

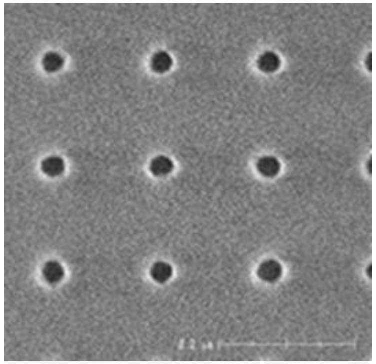


L18P36



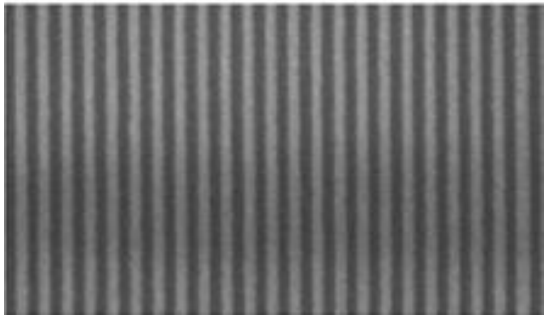
L16P32 Modulation



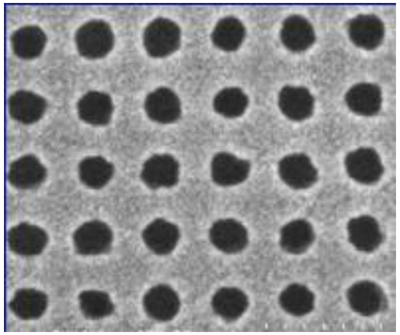


C32P84

Non-CA Resist



L16P32

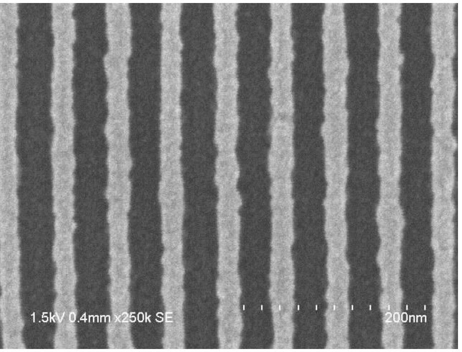


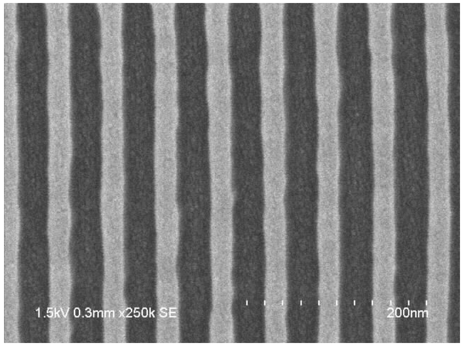
C32P70

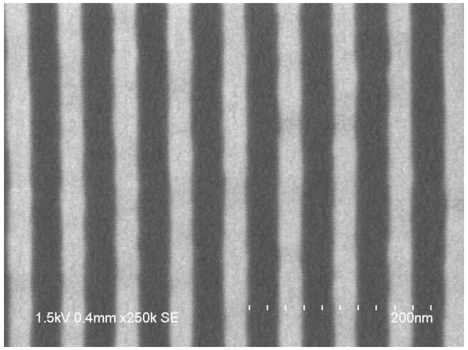
LWR Mitigation

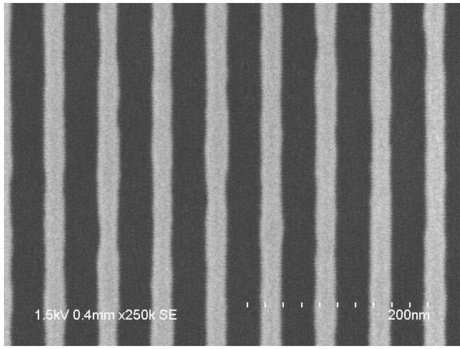
NXE3100, 50 nm FT, 30 HP

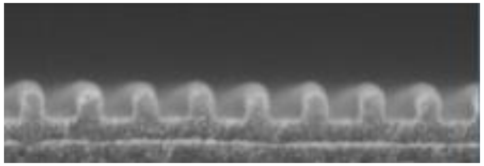
Litho ← LWR Mitigation →

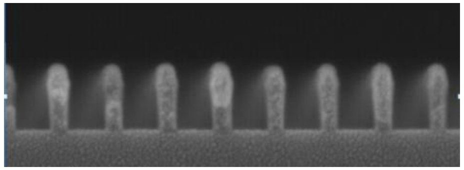




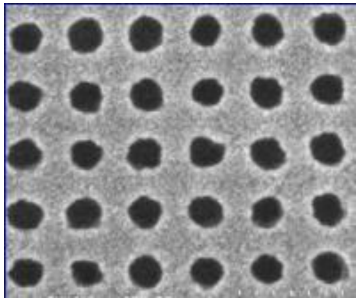


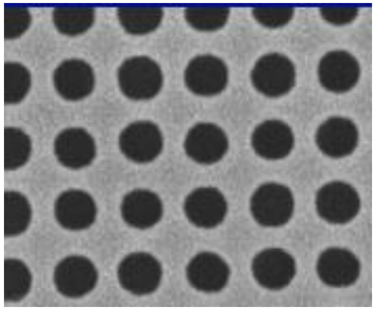


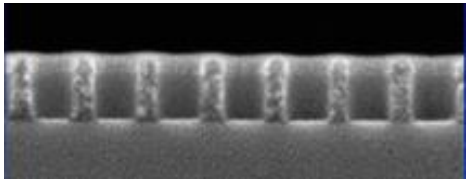




NXE3100
70P







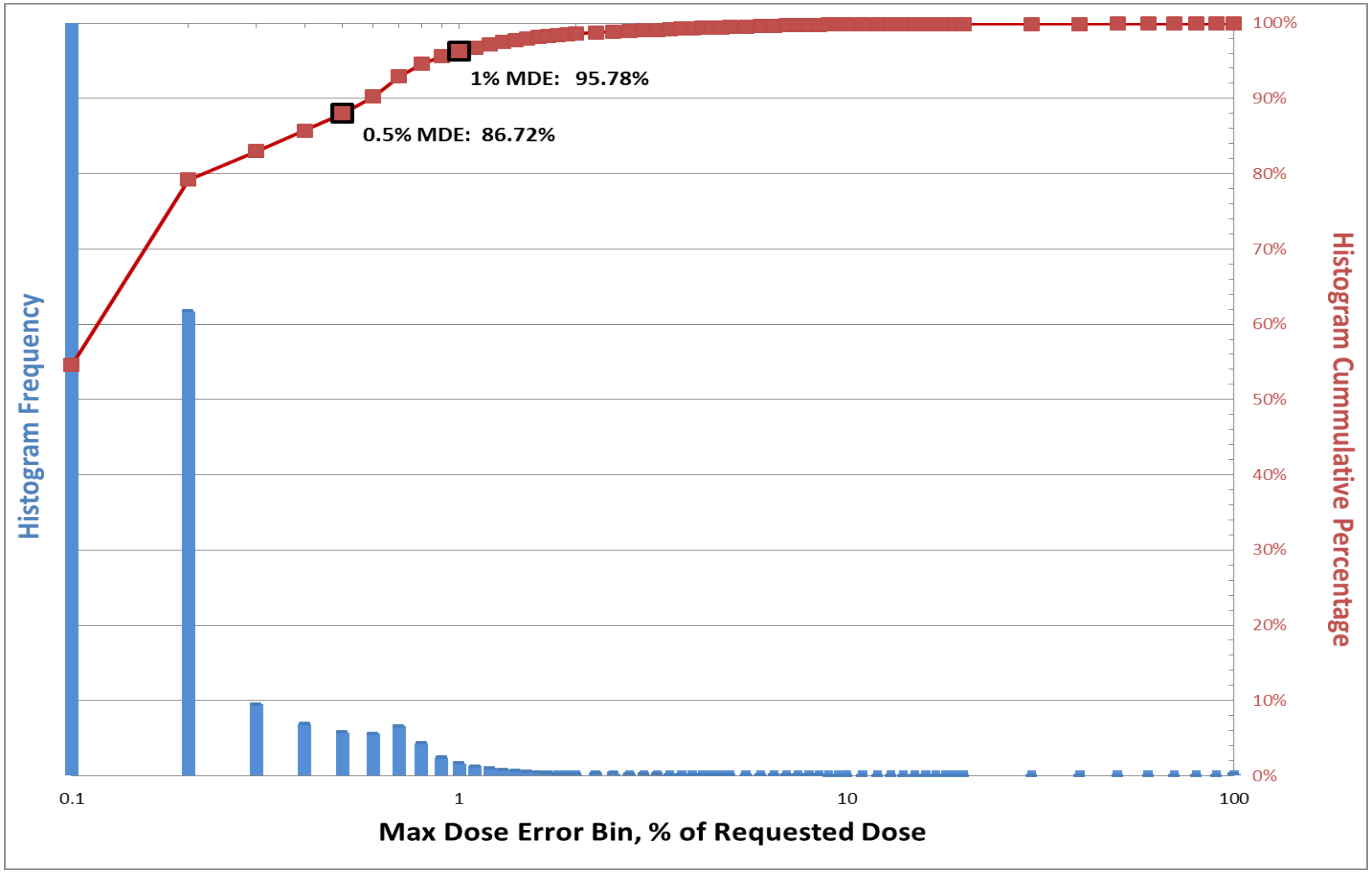
Resist Performance – Key Takeaways

- Resist resolution performance looks reasonable for 18-20 nm HP, will need further improvement beyond this target
- LWR performance is a challenge but promising results seen for post-litho treatments
  - Non-CA resist LWR looks good but photospeed is key issue
- Good results seen for hole patterning, but pattern shrink techniques would be needed to achieve CD targets
- Preliminary double pass approaches (LFLE, LELE, etc.) look reasonable for EUV

Current resists when pushed for pitch on NXE 3300 will require significant improvement

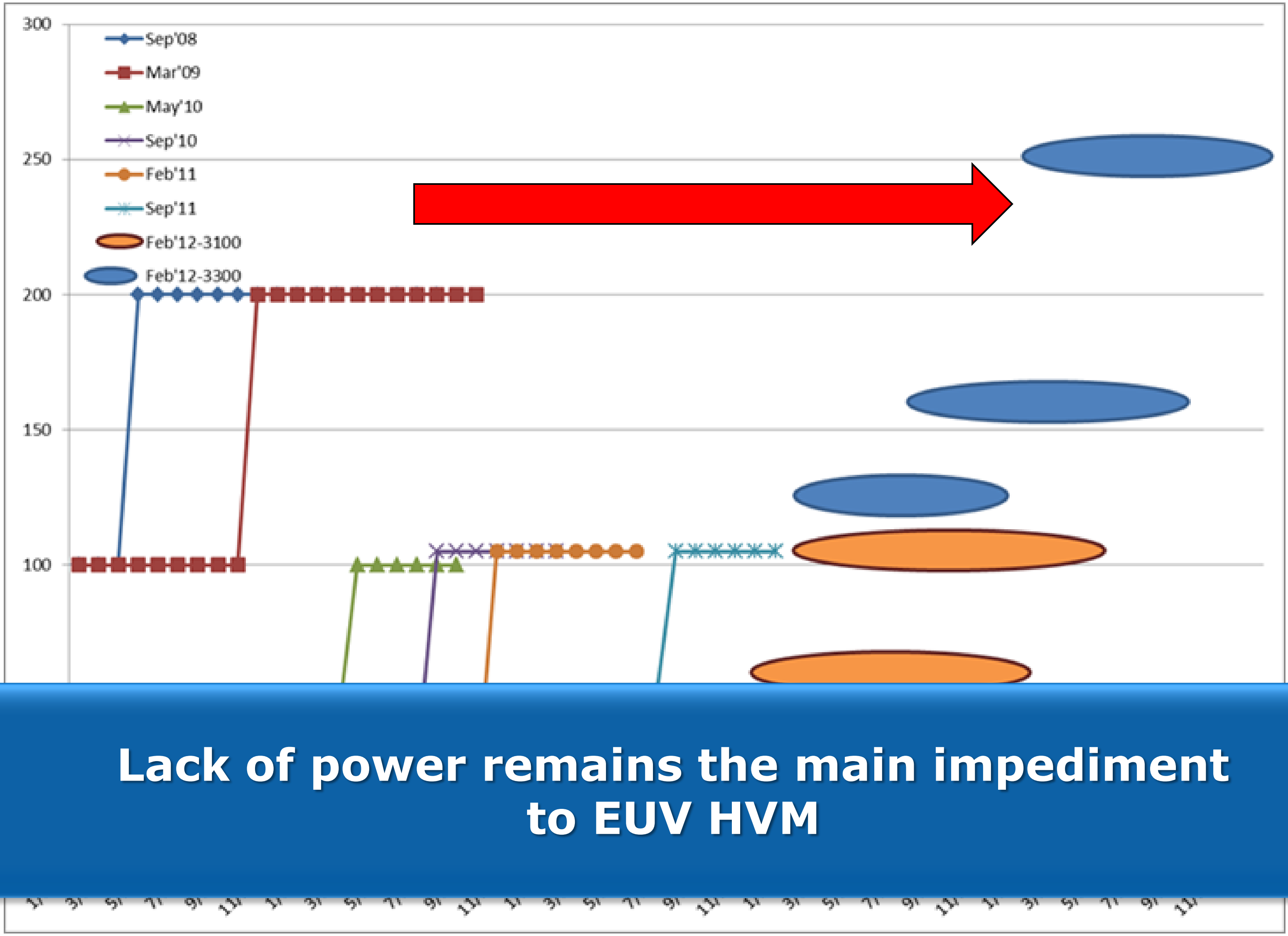
Source Performance

Max Dose Error Per Field



Power delivery reasonable, getting better

Laser Power Roadmap



Lack of power remains the main impediment to EUV HVM

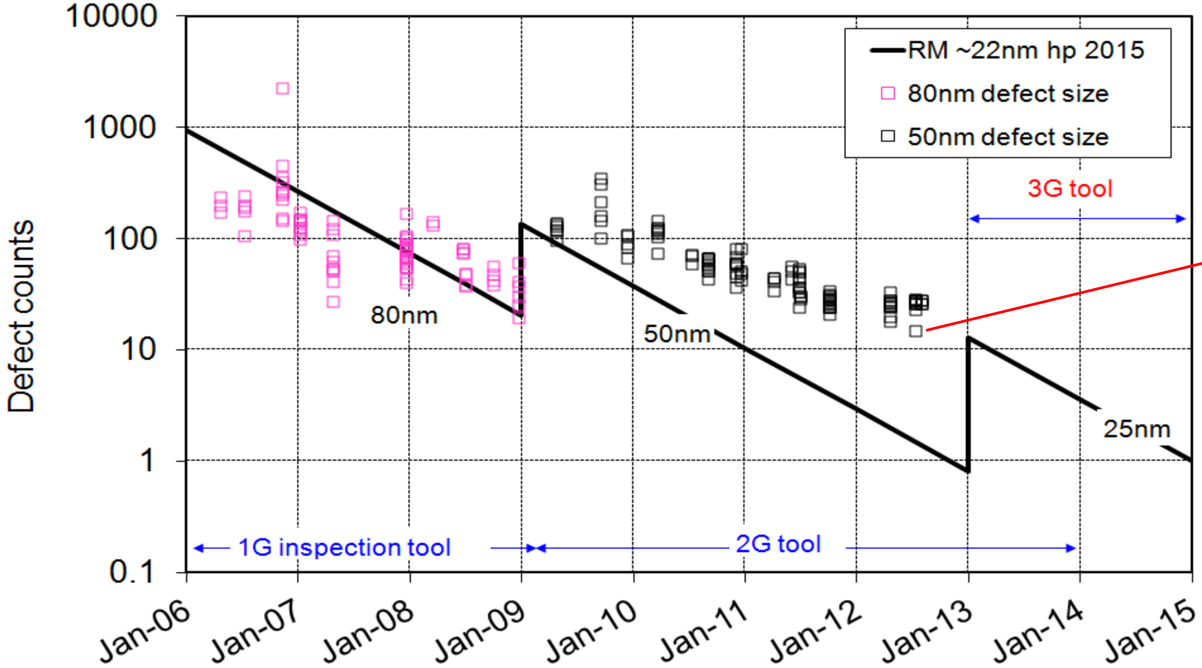
Source Performance – Key Takeaways

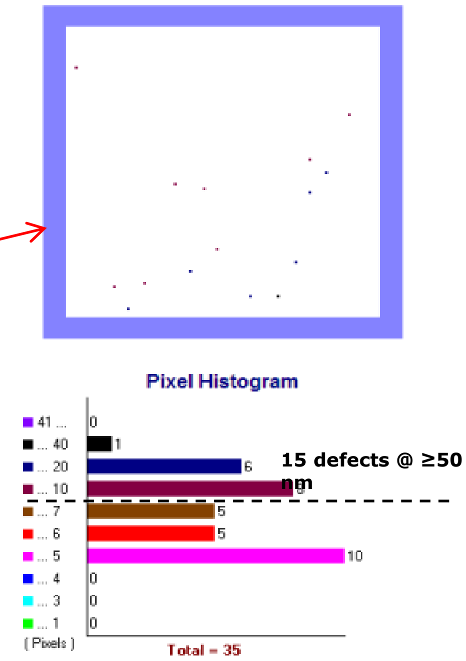
- Intrinsic source performance showing good improvement over time
  - Significantly higher availability seen week to week with better predictability in maintenance/consumable changes
  - Good dose error performance seen with scope defined for further improvements
- While higher HW reliability is needed, key remaining technical hurdle is source power
  - Delays to roadmap threaten to impact EUV insertion
  - SPIE Cymer data of >50W power is welcome news!
  - Need to build on the momentum and focus attention on power roadmap and any collateral impact to lifetime of other ancillary hardware

Achieving high, reliable power is key!

Reticles

Blank Defects





- <40defects @50nm being produced (low yield)
  - Process capable of generating blanks with <20 defects @ 50nm has been demonstrated
- Inspection capability @ 30nm needs to be set up at blank vendor for further improvement

Reticle Integrated Performance

Mask: 22 nm node test chip

Blank: LTEM, Full ML, 84nm Ta based absorber

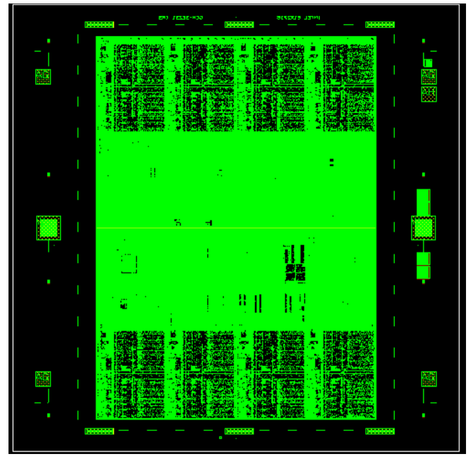
Pattern Reg: X/Y=-3.59nm/4.89nm

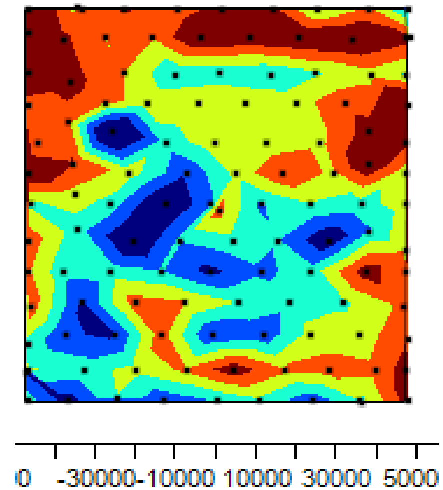
Flatness: FS=439nm, BS=493nm

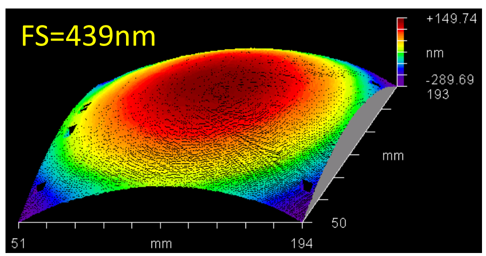
EUV Reflectivity: Ref.=62.1%, CW(λ)=13.524nm

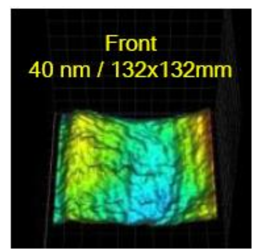
Absorber EUV leakage: 0.75%

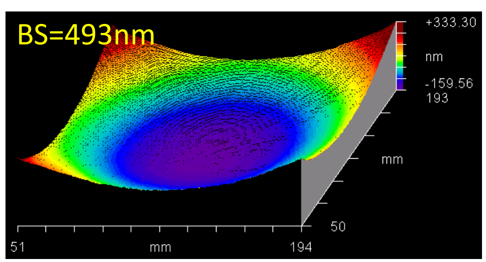
Defectivity: single digit before repair

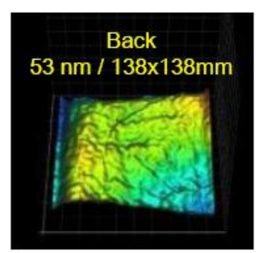


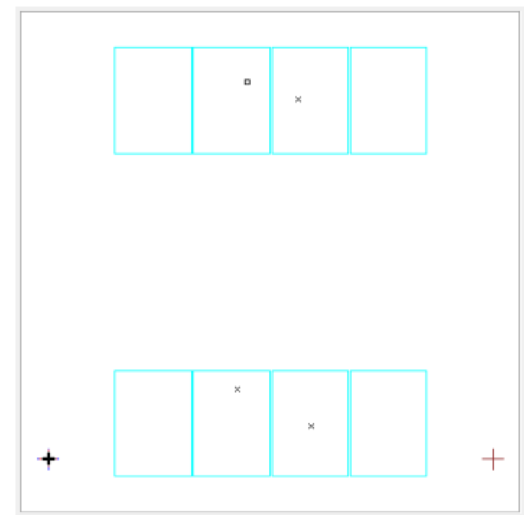




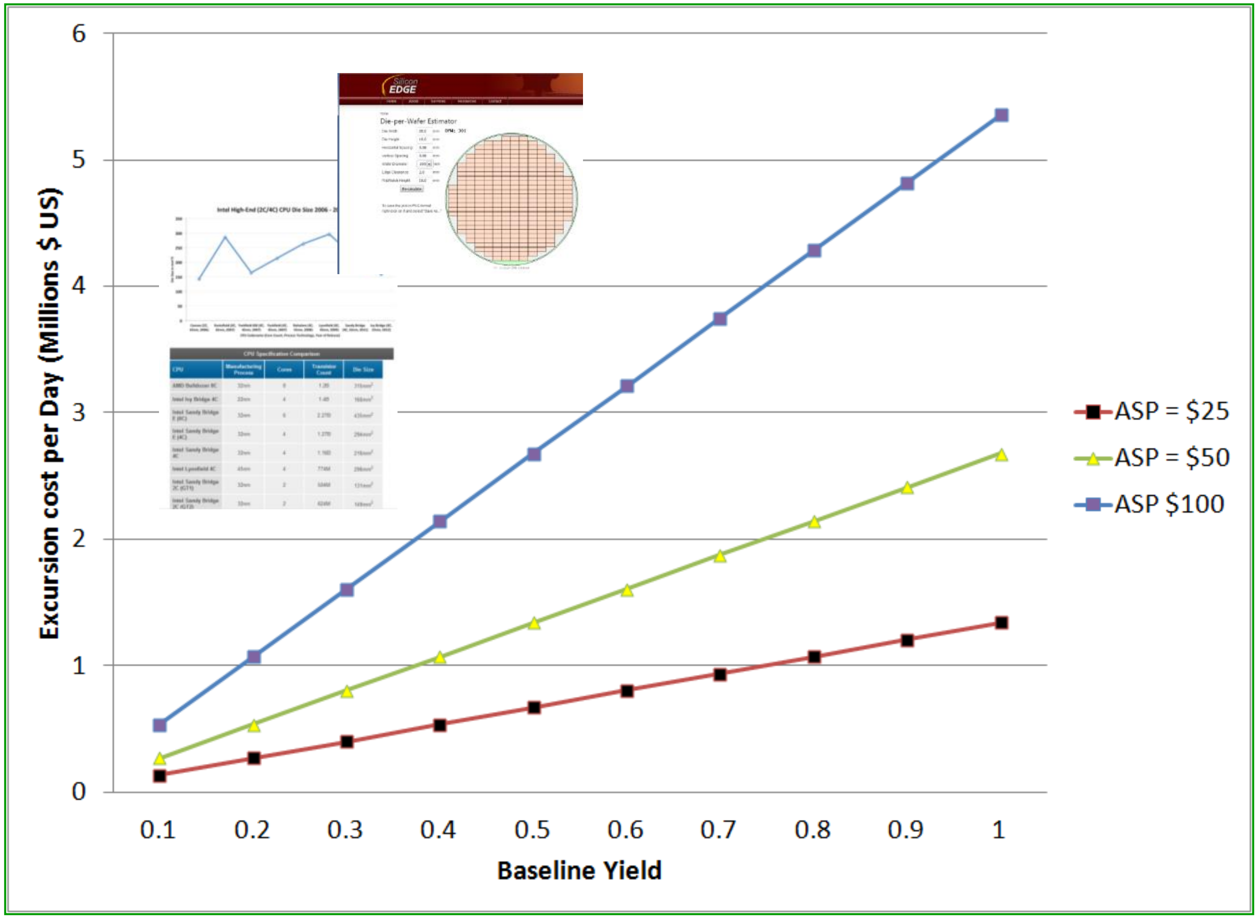








Daily Cost of a Reticle Fall-on Defect Excursion



Tim Crimmins,
Litho Workshop 2012

Model assumptions:

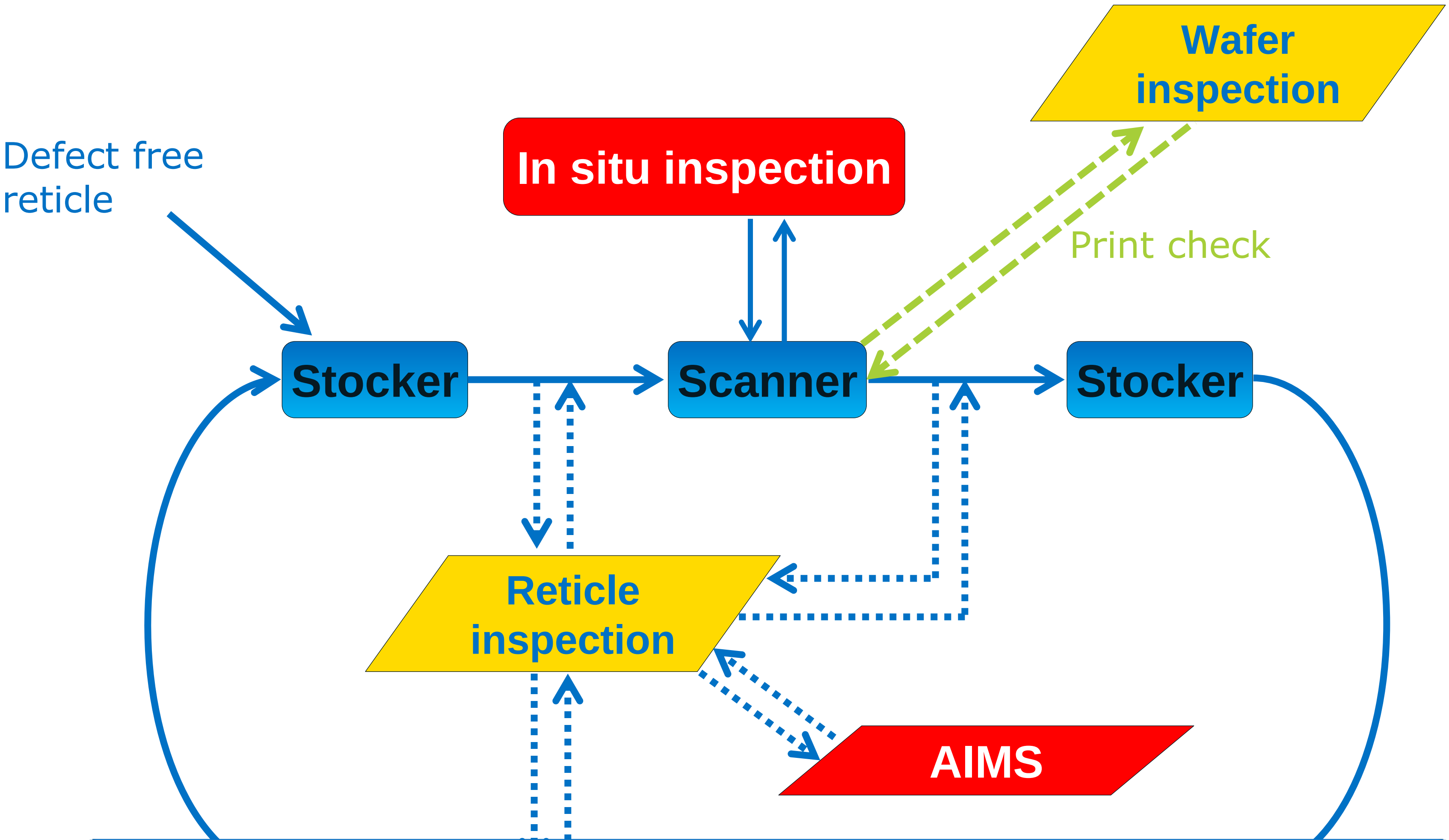
- Critical area = die area
- 200 mm² die
- 300 die per wafer
- Fab capacity = 5000 wafer starts per week

Representative data from the semiconductor industry

Reticle defects are tremendously expensive

EUV In-Fab Reticle Flow

Tim Crimmins,
Litho Workshop 2012



Reticle, mask and wafer inspection metrology need to be ready to support the EUV launch

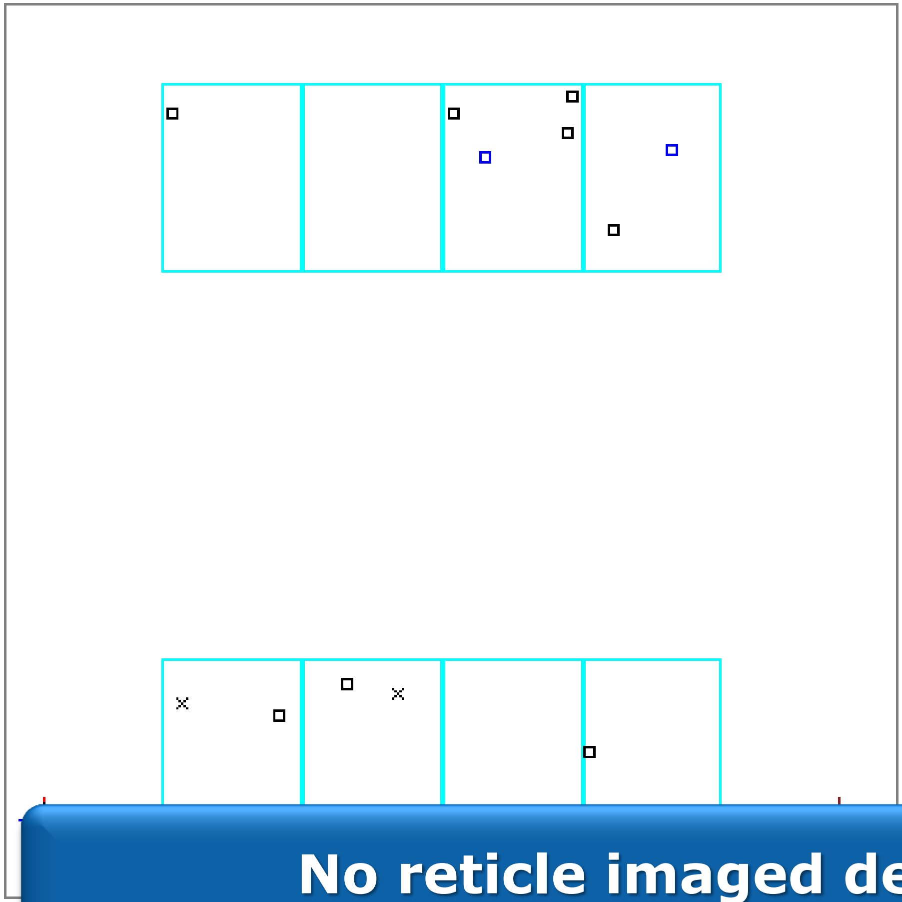
Inspection for EUV HVM – Key Takeaways

- Yield cost of random reticle adders is very high
  - Wafer inspection to catch reticle adders is an extremely costly and unworkable strategy
    - Higher wafer TPT and greater capital inspection capital investment
    - High need for EUV AIMS
- Need to ensure that adders are not patterned
  - Need to make them too small to resolve
  - How to ensure 10-5 adders per reticle pass?
  - Need to ensure reticle is in a known clean state at the point of exposure - in-situ reticle inspection?
- Keep adders away from absorber surface
  - Pellicles are essential to long-term defectivity health of reticles at previous wavelengths, and they are critical for EUV!
  - Physical requirements are available for pellicles and frames for NXE platform
  - Pellicles will reduce EUV transmission, so source must keep up

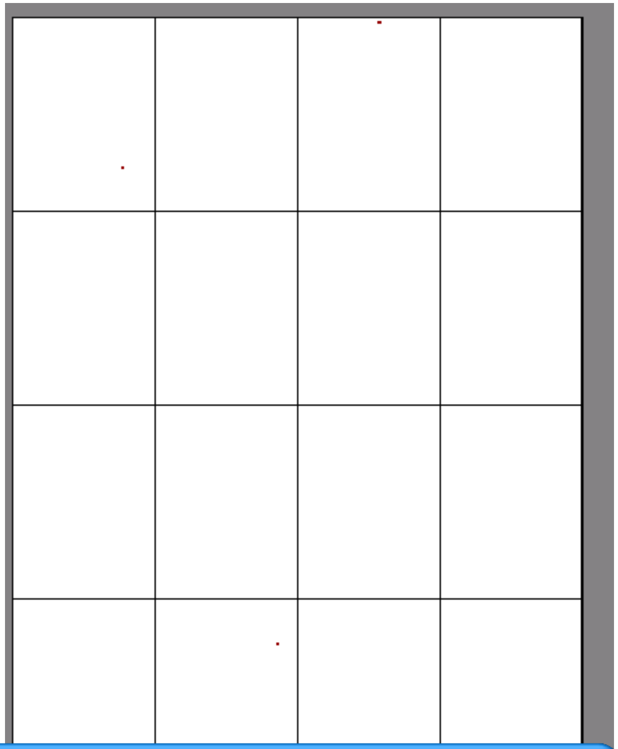
Integrated Performance

Production Reticle Printed Defectivity

Reticle Pattern Defects

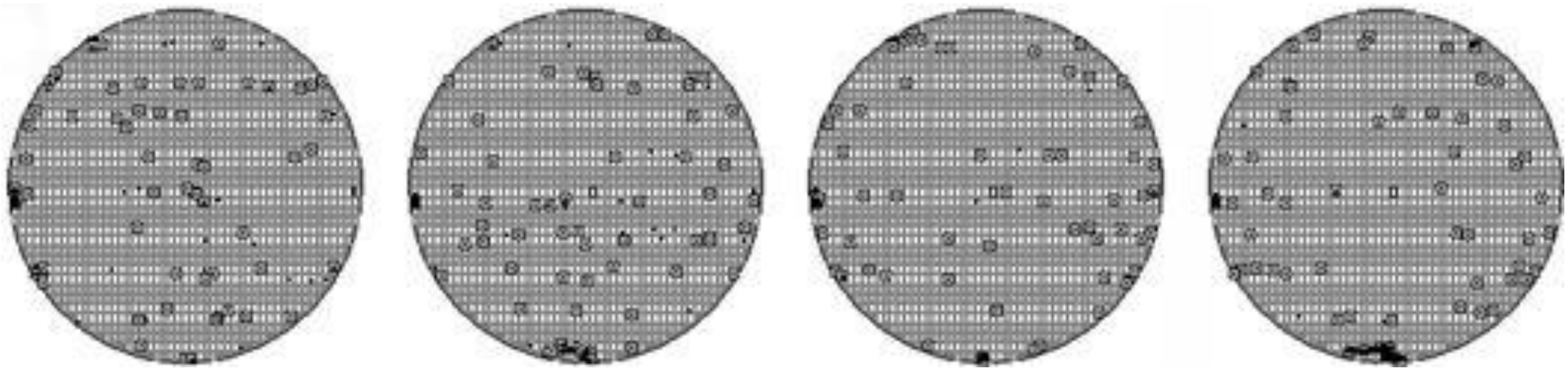


Imaged Reticle Defects



No reticle imaged defects detected

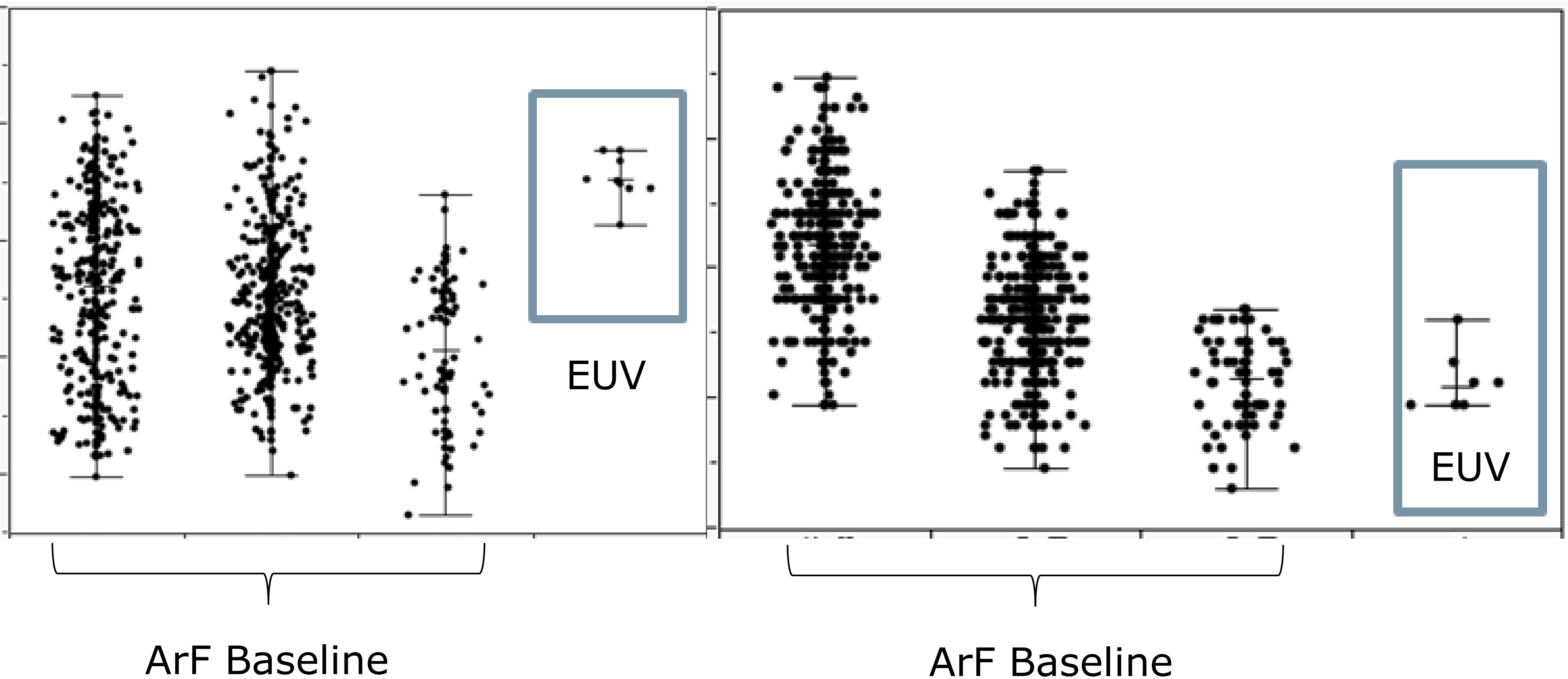
Integrated Defect Performance



ArF EUV

Integrated post-etch production wafer defectivity roughly comparable, no new EUV-specific defect modes

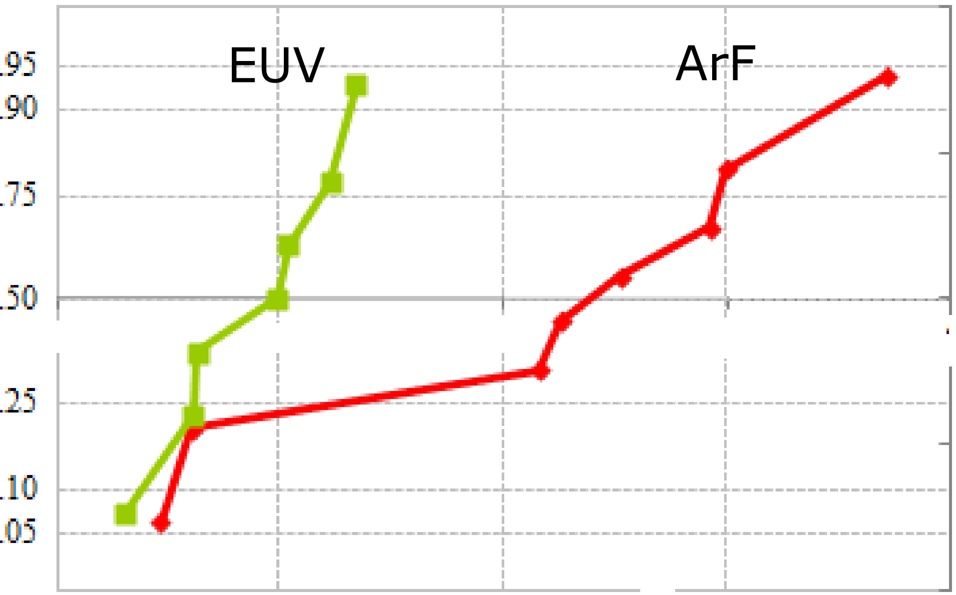
Contact/Metal Resistances



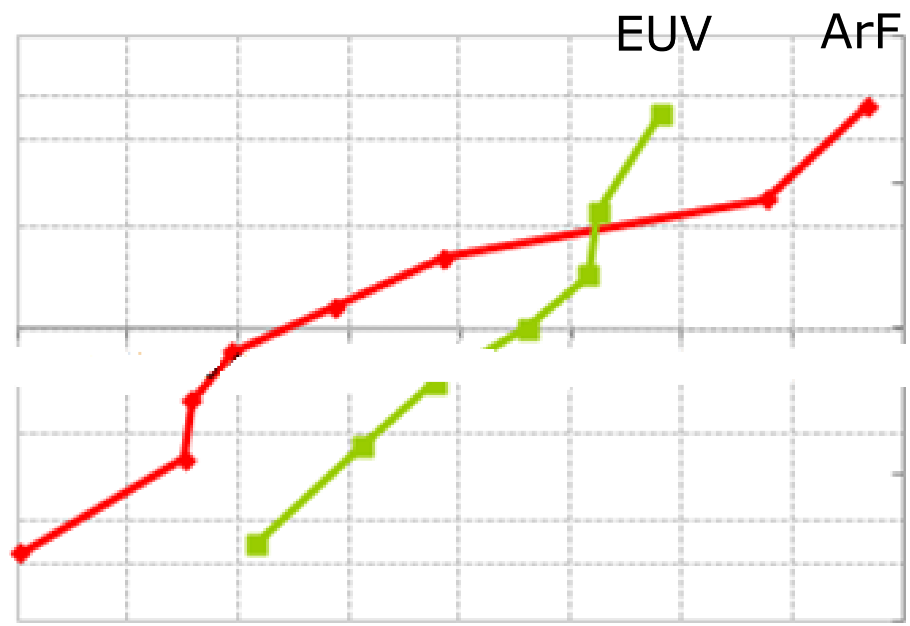
EUV Performance within ArF fab distribution

Electrical Performance - Transistor

P Channel Drive Current

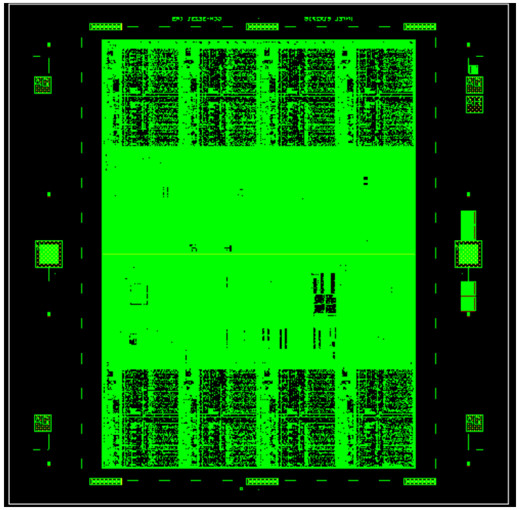


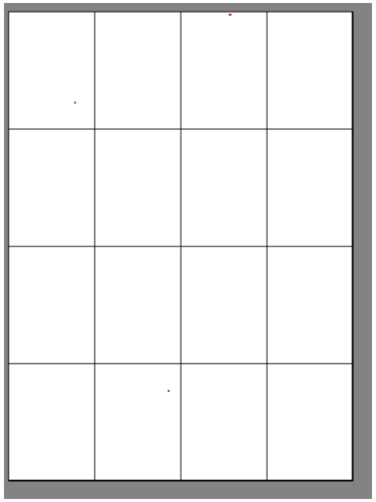
P Channel Threshold Voltage



EUV On-Wafer Electrical Performance Matched to ArF Baseline

Recent Results –Yield





- 22nm node SRAM test chip processed through entire line
- EUV yield was achieved – no EUV-unique defect modes identified
- All yield-loss mechanisms are unrelated EUV patterning process steps

There appears to be no fundamental roadblock to EUV achieving yield parity with ArF

Summary

The Good:

- EUV hardware performance roughly in line with ArF
- Resist performance looks reasonable for 18-20nm HP, needs improvement for tighter pitches
- Integrated data shows EUV performance matched to ArF baseline for defectivity and CD control. Reasonable yield achieved on 22nm
- Steady progress on mask blanks, need long term improvement
- Reticle pellicle program gaining momentum

The Not-So-Good:

- Source power is a significant concern, well behind schedule
- Reticle defectivity is a significant concern
  - Need good strategy for maintaining reticle cleanliness
  - Send-aheads are prohibitive for EUV HVM
  - Reticle inspection capability is needed in time

Demonstrable progress on these key items over next 1-1.5 years is essential!

Thank You!