Sub-10nm HP Patterning using EUV based Self-Aligned Double Patterning (P46)

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Micron (A. Niroomand)

APPLIED MATERIALS®

Planar Flash Drives 1:1 Duty Cycle HP Scaling

Effective Cell Size (nm2)

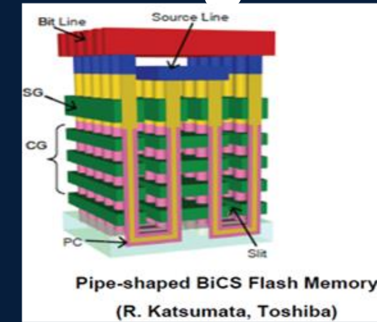
10000
1000
100

- Planar FG SLC
- 3D BICS/TCAT 16 Layers
- 3D BICS/TCAT 32 Layers

193 immersion   Multiple Patterning/EUV

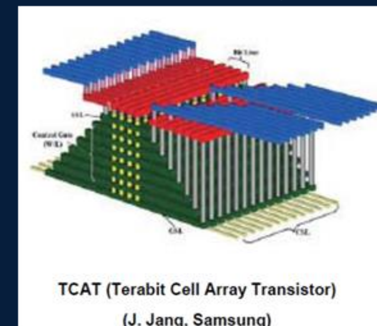
60 50 40 30 20 10

CD (nm)



Pipe-shaped BiCS Flash Memory (R. Katsumata, Toshiba)

- ➢ Planar NAND Ends Around 13-15nm
- ➢ 3D Memory Stays at >40nm Lithography and Scales Vertically


TCAT (Terabit Cell Array Transistor) (J. Jang, Samsung)

Current Choice for low 1xnm HP Patterning is 193i SAQP or EUV SADP

Acknowledgements:- Toshiba, Samsung. International Memory Workshops 2011.

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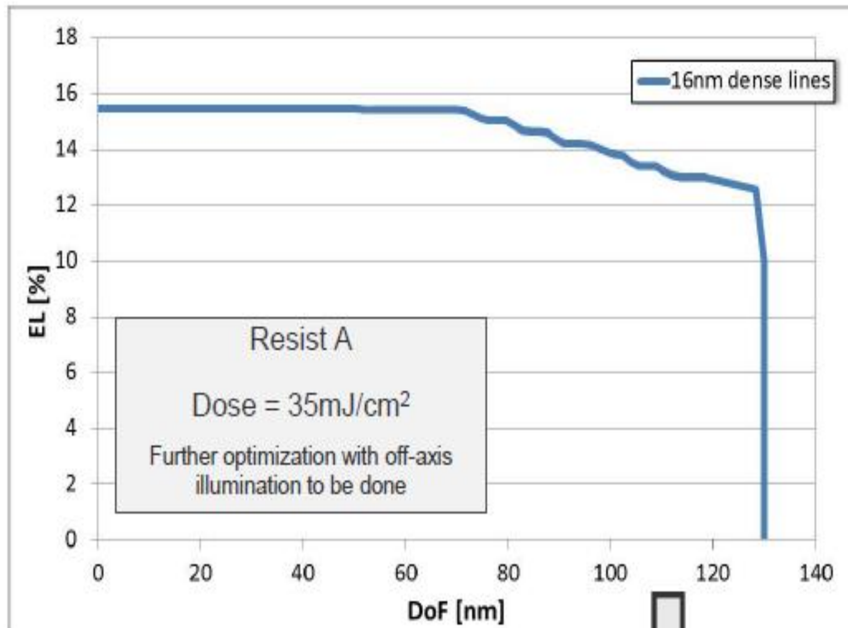
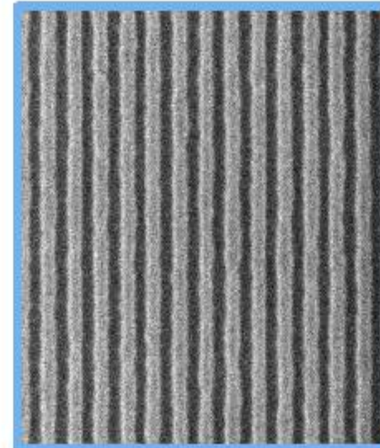
EUV SADP Could Scale ~ 8nmHP(1:1) with Resist/Source Improvements

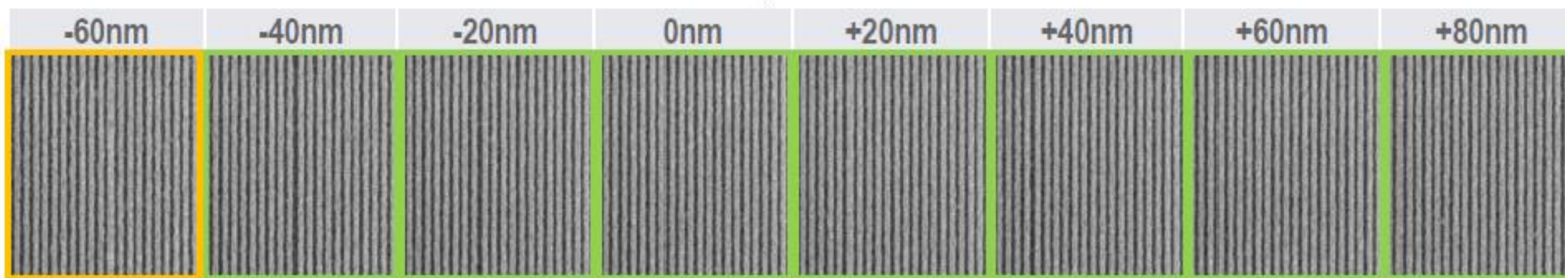
16nm dense lines with >15% exposure latitude and >120nm DoF on NXE:3300B (dipole-45 setting)

ASML





16nm L/S Dipole 45X
29.0mJ/cm2
Resist B



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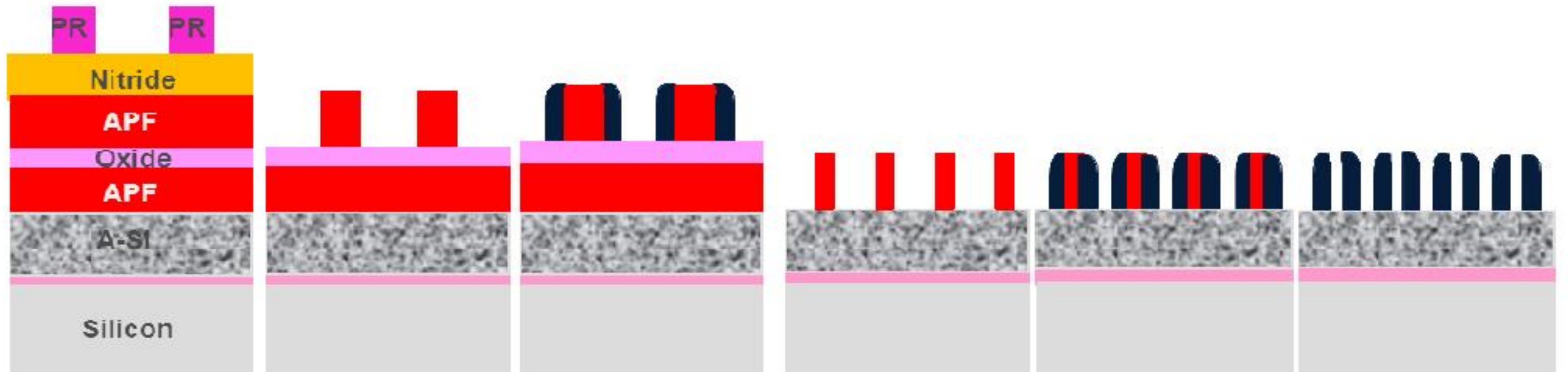
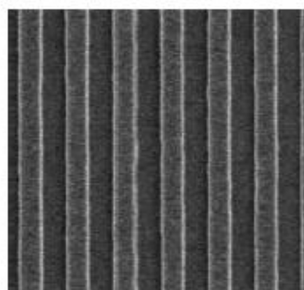
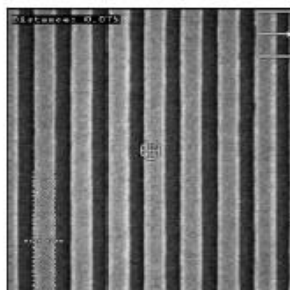
193i SAQP: The Other Alternative



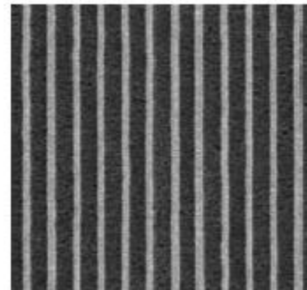
- Illustration of process flow of the SAQP scheme 1



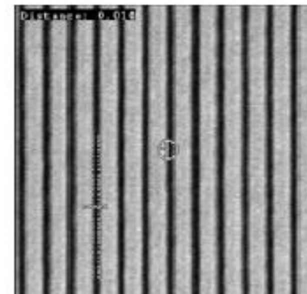
Top mandrel etch



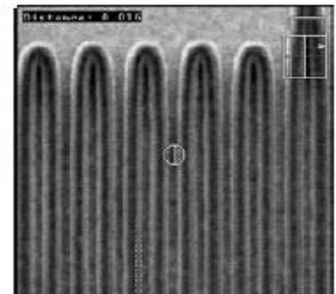
NIT Spacer1 Deposition



NIT Spacer1 etch, top mandrel strip & bottom mandrel etch



NIT Spacer2 Deposition



Bottom mandrel strip to form final pattern

2x SADP with Increased Process Costs and CDU Challenges

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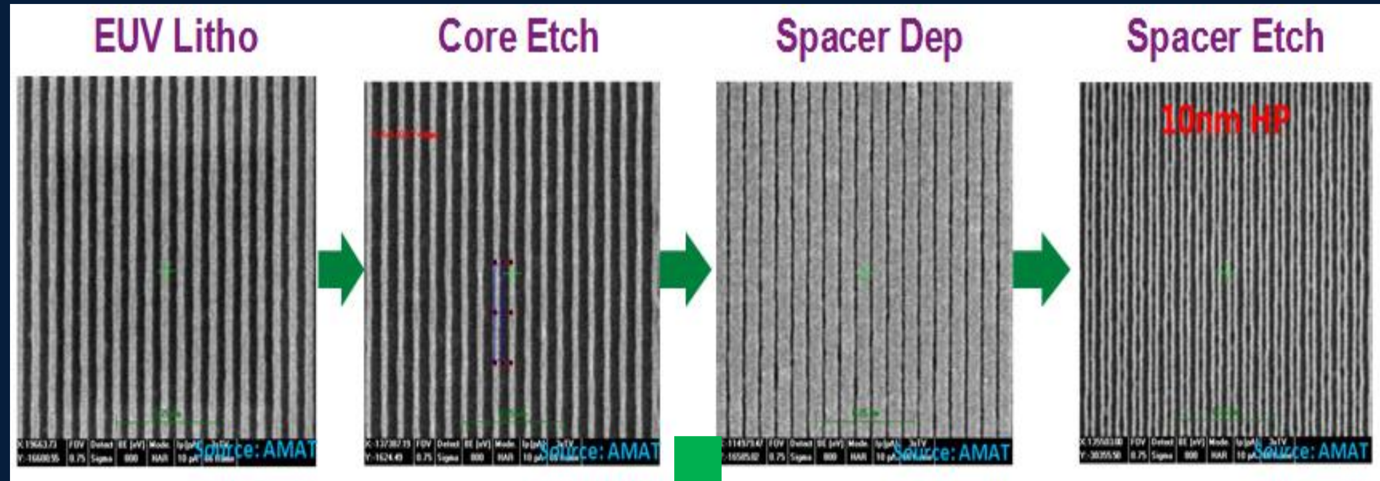
9/10nm HP EUV-SADP Demonstrations

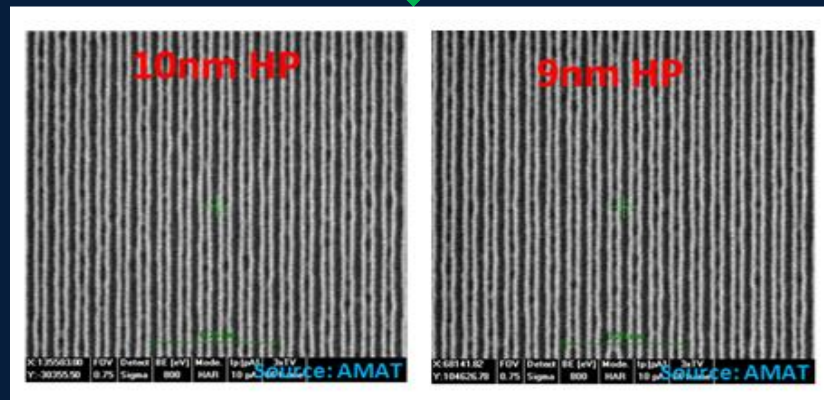
NXE 3300B
NA 0.33, Dipole
50nm Resist Thx
FIRM Rinse

Nitride
APF
Poly
Pad Oxide
Si

20nm 1:1 L/S Patterns



AMAT Producer PECVD



AMAT Mesa Etch

10nm L/S **9nm L/S**

A Potential Path for Low 1x,y,z nm Planar Flash Scaling

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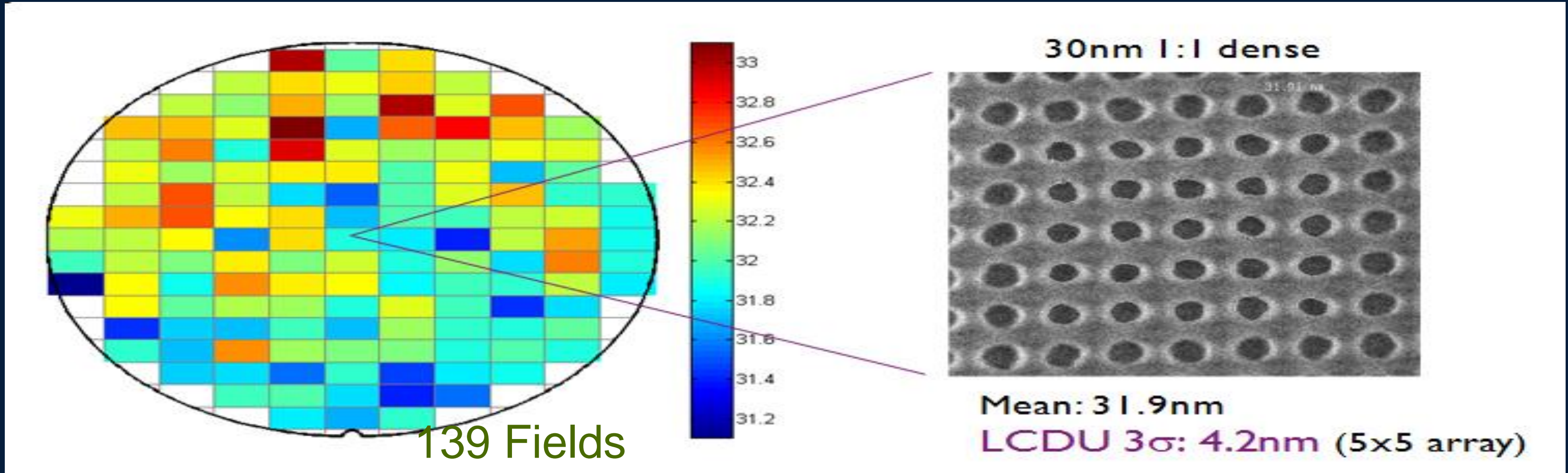
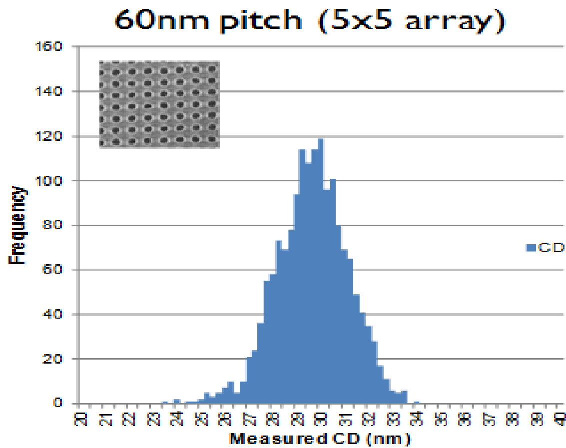
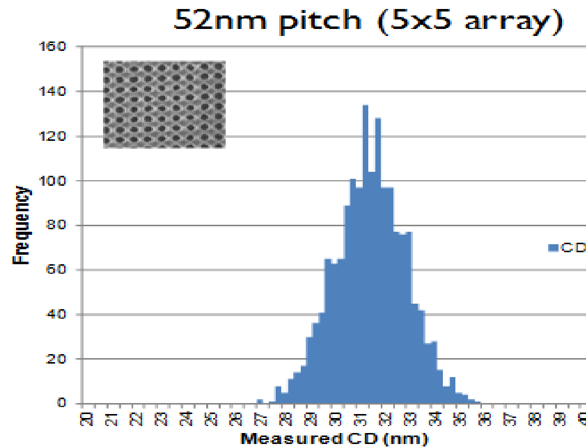
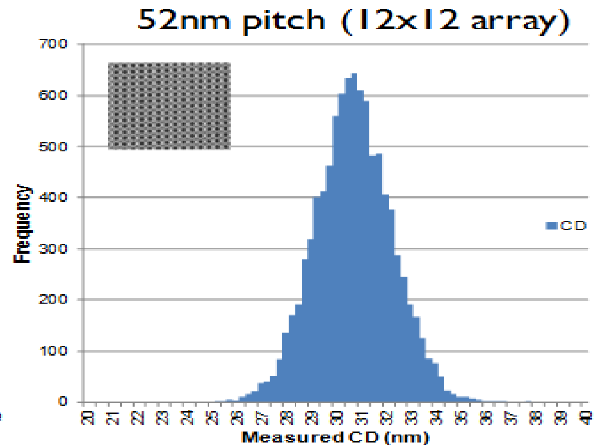
CON CDU Characterizations: Local Variations









30nm/26nm CON Data (5x5 and 12x12 arrays) Pooled Over 65 Fields

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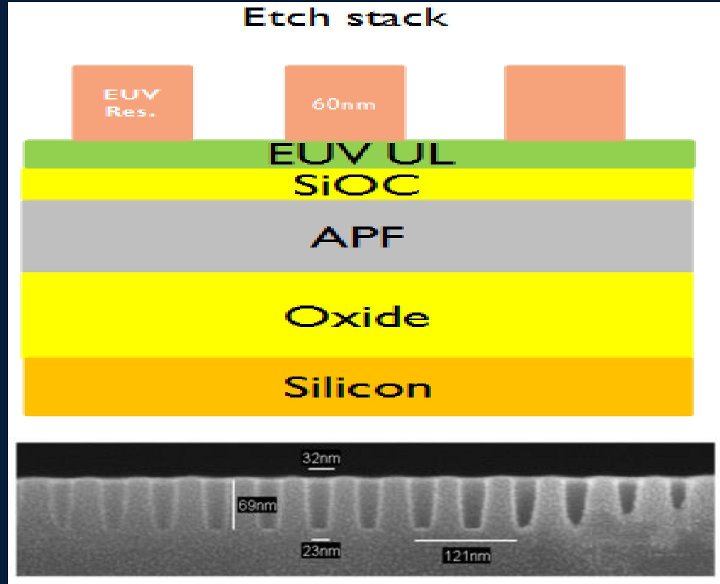
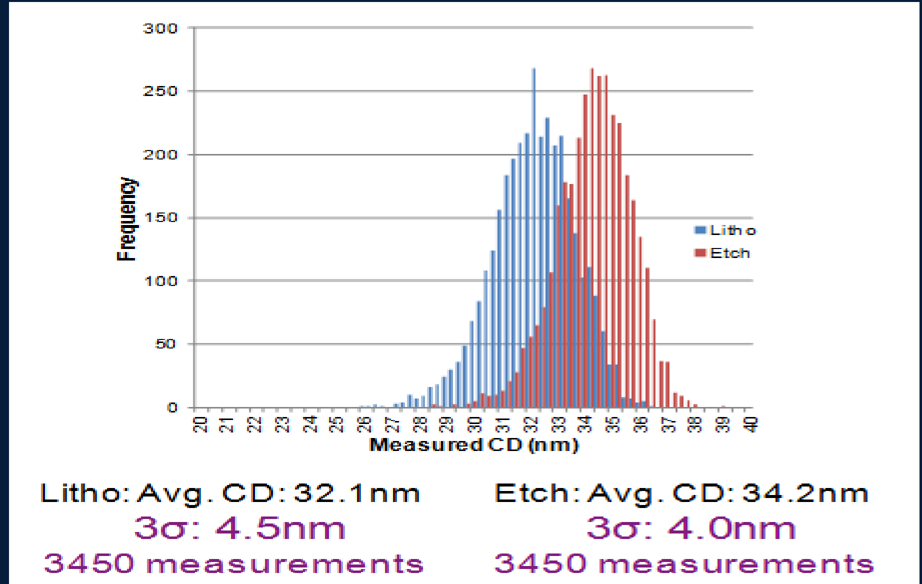
CON Etch/Shrink Development



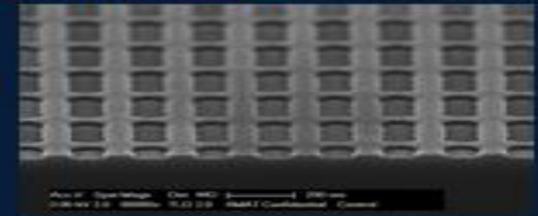


~+2nm CD Bias, Local CDU Transfers

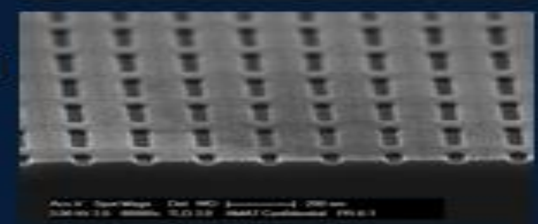
168 Fields, 5x5 Arrays Post-etch

Hardmask Etch & Ash

Etched w/o Shrink



Etched with 40nm Shrink



Low Temp C-Spacer, Minimal Micro-Loading

Provides Sizing Flexibility to OverCome Shot-Noise Induced CDU Issues.

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Next Steps

- 9nm HP EUV SADP Demonstrated Post-Etch.
- Continuing Work in Low Temp Spacer Materials and Stress Control to Understand Impact of LWR and CDU.
- 26nm/30nm CON Arrays Highlight Local CDU Variations That May Require Sizing Based Approaches.
- Low Temp CON Hole Shrink Spacers May Provide the Path to CON Scaling Needed for Sub 10nm Nodes.