Enabling EUVL for HVM Insertion

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Intel Corporation

International Symposium on EUV and Soft X-Ray Sources, 5 November 2013, Dublin, Ireland

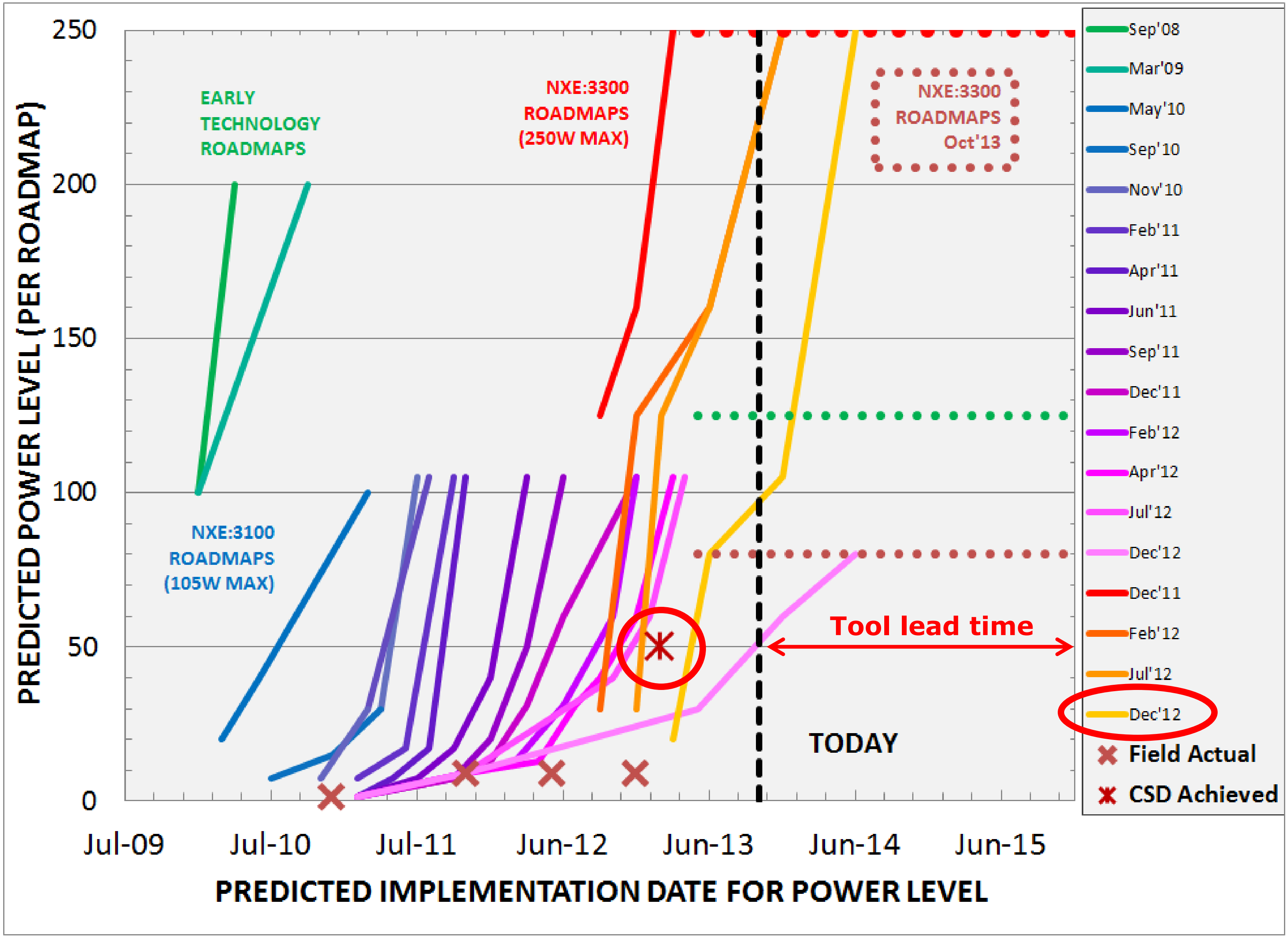
Outline

- Problem statement
- Status update on EUVL insertion in HVM
  - Resist, Reticle defects, Pellicles, Reticle Metrology
  - Challenge to Exposure Source community
  - Challenge to Metrology Source community

Problem Statement

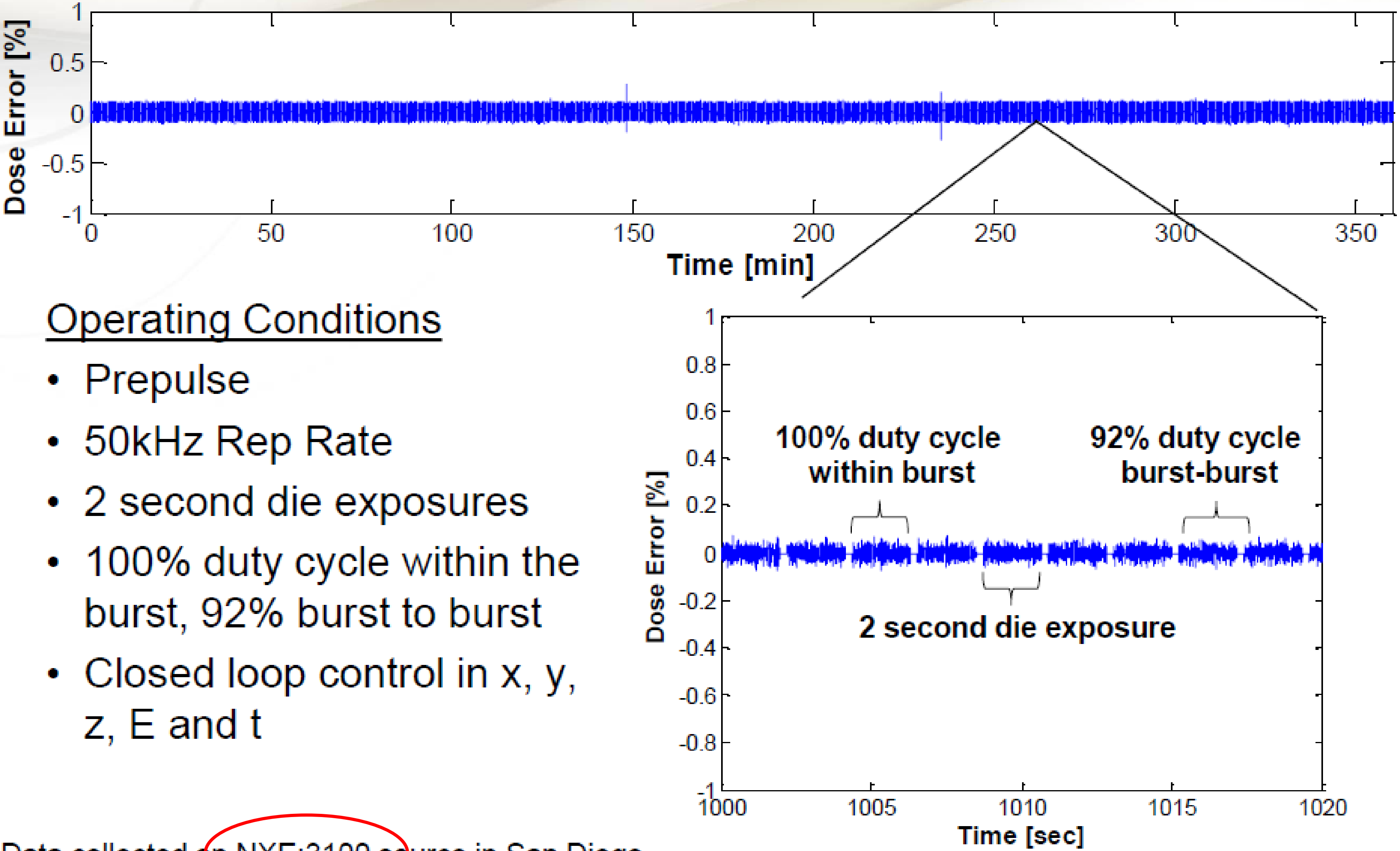
- Long delays in the exposure source power roadmap have undercut the credibility of EUVL
- Investments in other EUVL infrastructure have been reduced or delayed due to this uncertainty
- We are now at risk that practical power levels will be available before the complete infrastructure required for use of EUVL in HVM is ready.

Source power roadmap has lost credibility



MOPA Prepulse Performance at 40W

Exceptional Dose Stability <±0.5%



Operating Conditions

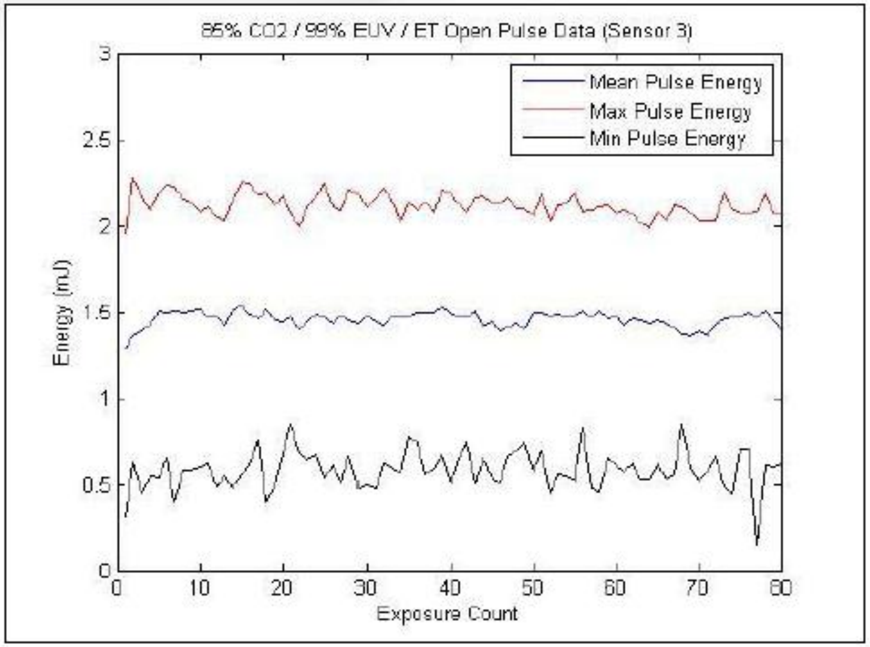
- Prepulse
- 50kHz Rep Rate
- 2 second die exposures
- 100% duty cycle within the burst, 92% burst to burst
- Closed loop control in x, y, z, E and t

Data collected on NXE:3100 source in San Diego

From D.C.Brandt *et al.*

NXE:3300B Source Qualification Progress in MOPA Prepulse: 60W Open Loop Power

60W (open loop)

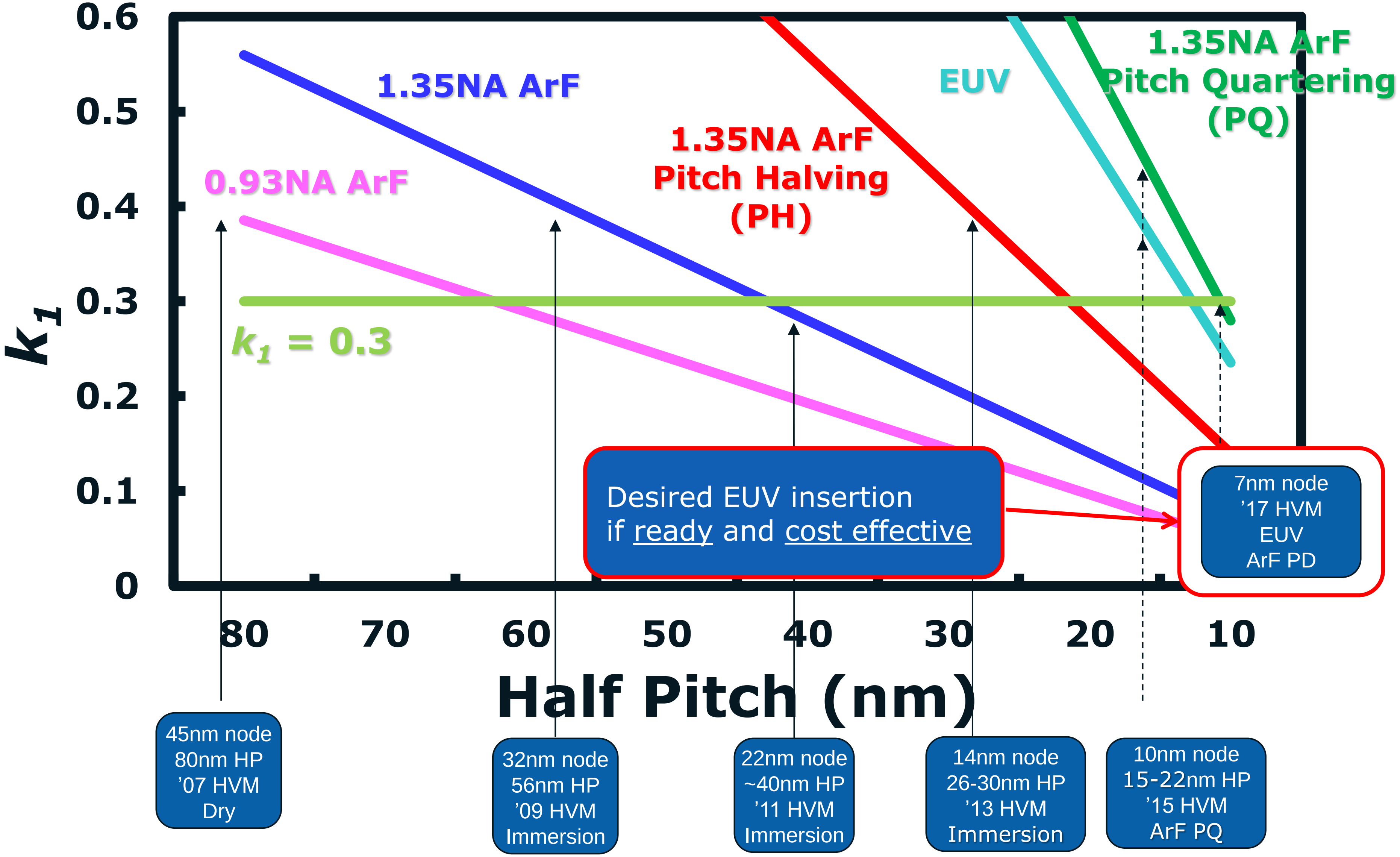


- **50kHz repetition rate**
- **Initial dose control results shown, dose margin will be improved after full controls are applied**

Short-term power outlook

- Need 40~80W stable MOPA+PP sources in the field linked to NXE:3300B scanners
- Not enough power for HVM, but enough to start TD and re-establish confidence in EUVL
- Seems achievable by Q1’14 given current status of program
- Need to look at remainder of EUV infrastructure and make sure it is on track for HVM introduction ~2017

Intel Process Nodes vs Litho Technologies



Desired EUV insertion
if ready and cost effective

7nm node
’17 HVM
EUV
ArF PD

45nm node
80nm HP
’07 HVM
Dry

32nm node
56nm HP
’09 HVM
Immersion

22nm node
~40nm HP
’11 HVM
Immersion

14nm node
26-30nm HP
’13 HVM
Immersion

10nm node
15-22nm HP
’15 HVM
ArF PQ

From Sivakumar, 2103 International Workshop on EUV Lithography

The Challenges of EUV

Resists

- Patterning requirements…
  - Resolution - *On track*
  - LWR/Dose - ?
- Outgassing
  - IDM TPT requirements
  - Scanner outgassing requirements

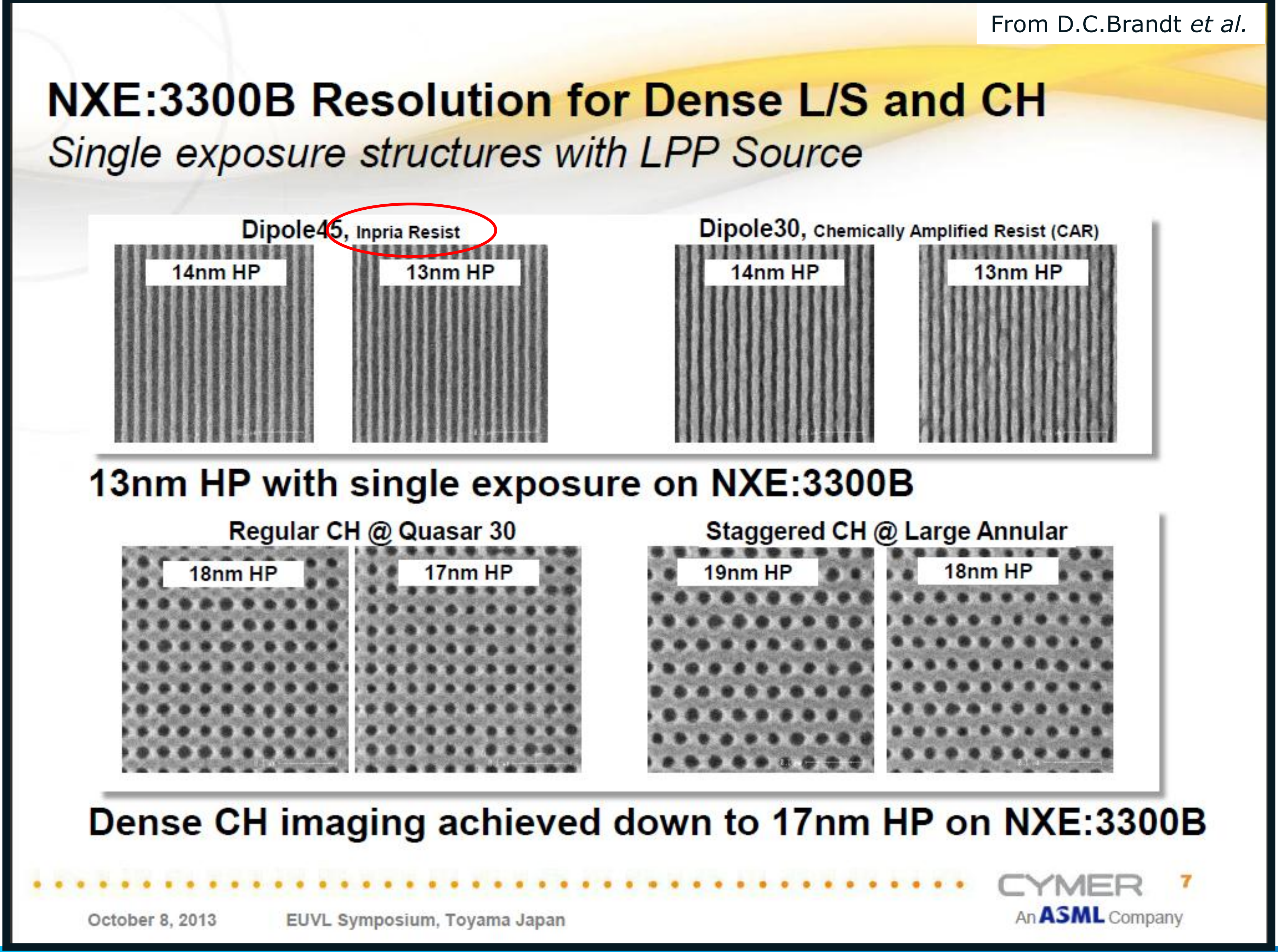
Tool

- Source
  - Availability
  - Power
- Scanner Hardware - *On track*

Reticle

- Defectivity
  - Killer defect impact >> wafer process defect impact
  - Mitigation strategies
    - Reticle inspection
    - Patterned wafer inspection
    - Alternative strategies

EUV HVM implementation depends on satisfactory progress on all these fronts!



From D.C.Brandt *et al.*

NXE:3300B Resolution for Dense L/S and CH

Single exposure structures with LPP Source

Dipole45, Inpria Resist

14nm HP

13nm HP

Dipole30, Chemically Amplified Resist (CAR)

14nm HP

13nm HP

13nm HP with single exposure on NXE:3300B

Regular CH @ Quasar 30

18nm HP

17nm HP

Staggered CH @ Large Annular

19nm HP

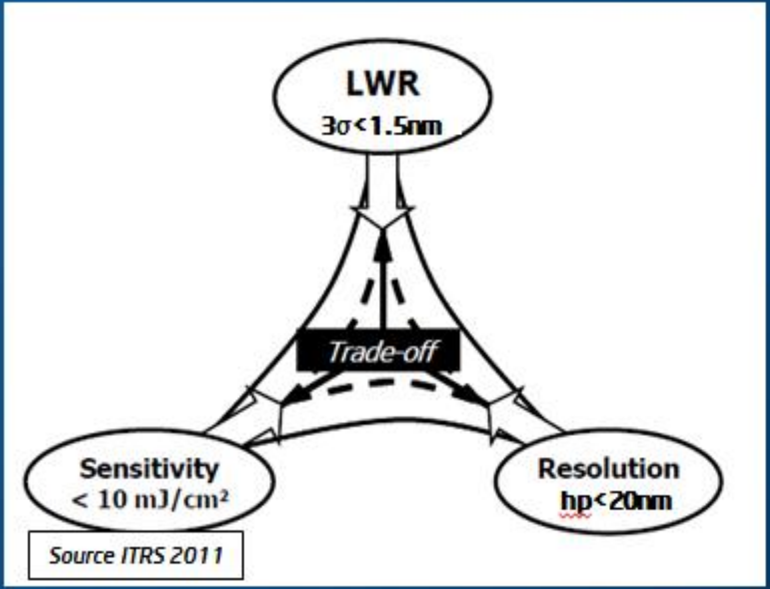
18nm HP

Dense CH imaging achieved down to 17nm HP on NXE:3300B

From Yan Borodovsky

EUV Triangles Duo

Line/Space

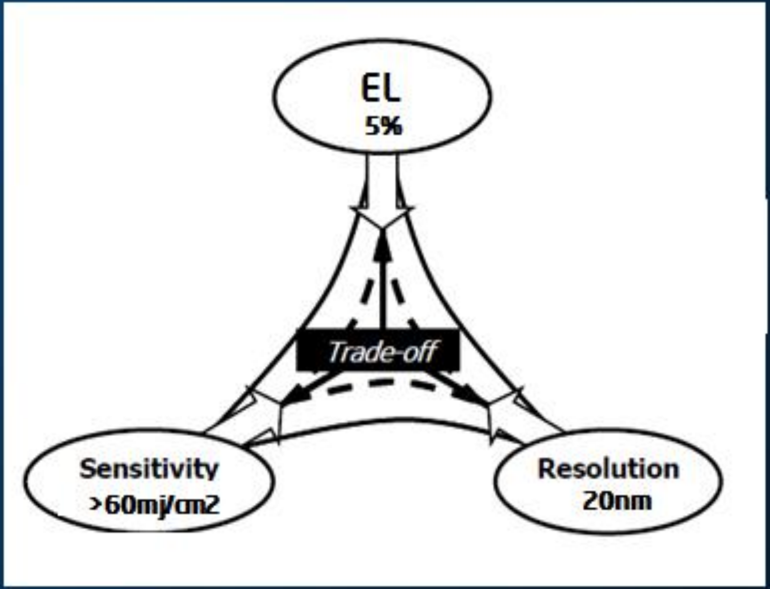


Source ITRS 2011

Blur^3*LER^2*Dose =C

Triangle of Death

Cut/Via



Size^2*EL^2*Dose=C

Triangle of Sorrow

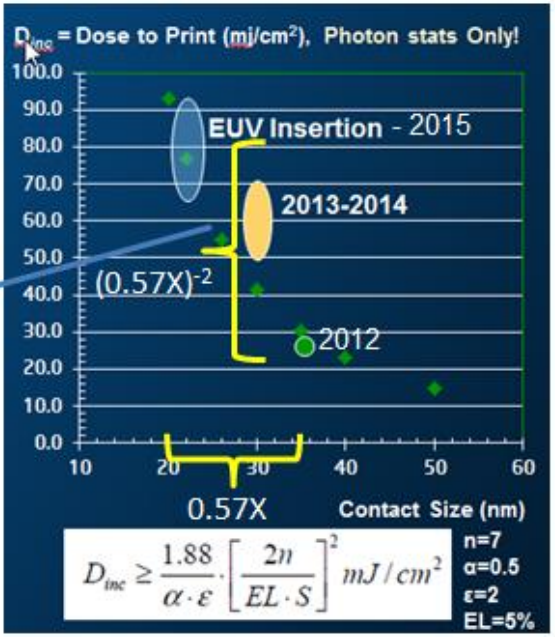
From: Yan Borodovsky, Intel, Semicon West 2012

From Yan Borodovsky

Complementary Lithography - View 2012

Gridded Layouts –
193i + Pitch Division
+ EUV Cuts
with HVM EUV

EUV Cuts –
Further EUV delays will be very expensive
Literally!
Post-EUV Shrink at Insertion?



$$D_{inc} \geq \frac{1.88}{\alpha \cdot \varepsilon} \cdot \left[\frac{2n}{EL \cdot S}\right]^2 mJ/cm^2$$

EUV Source Milestones for HVM insertion and beyond

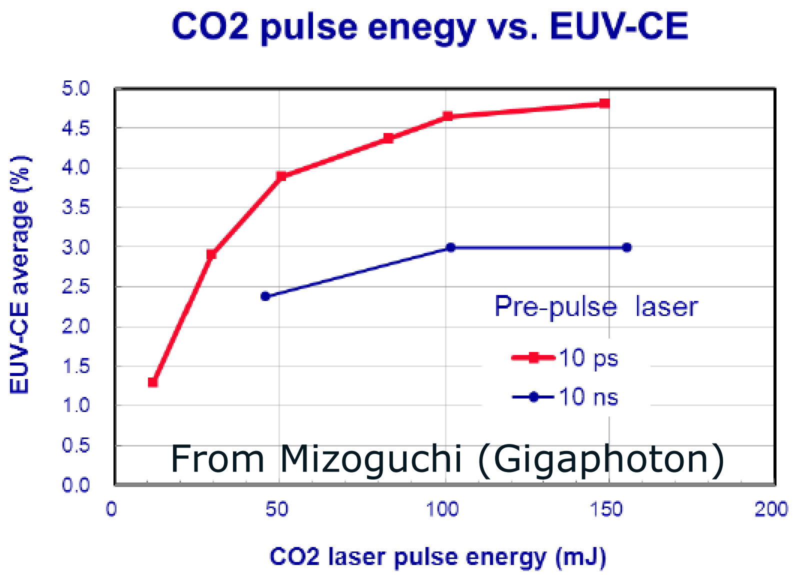
To keep HVM insertion on track:

- ~100W stable on tools in the field by Q4’14
- ~200W in CSD or VHV by Q4’14
- 250W stable on tools in field in 1H’2015
- Solid progress towards affordable source COO

For long-term viability:

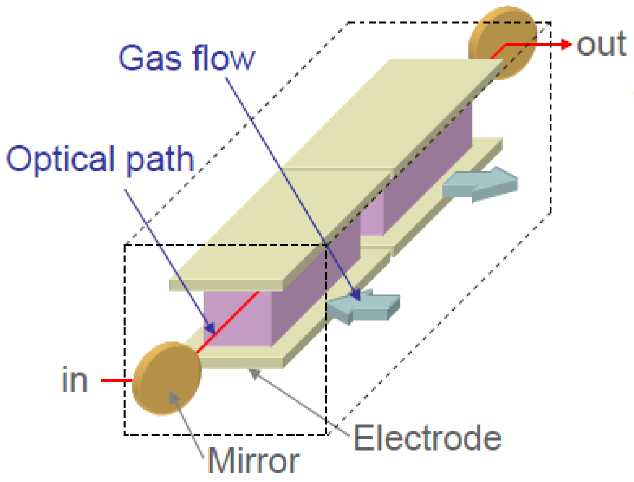
- Power scaling to ~1kW
- Dramatic improvements in COO

New work on high CE, transverse-flow drive laser, and grating collector shown in Toyama


CO2 pulse enegy vs. EUV-CE

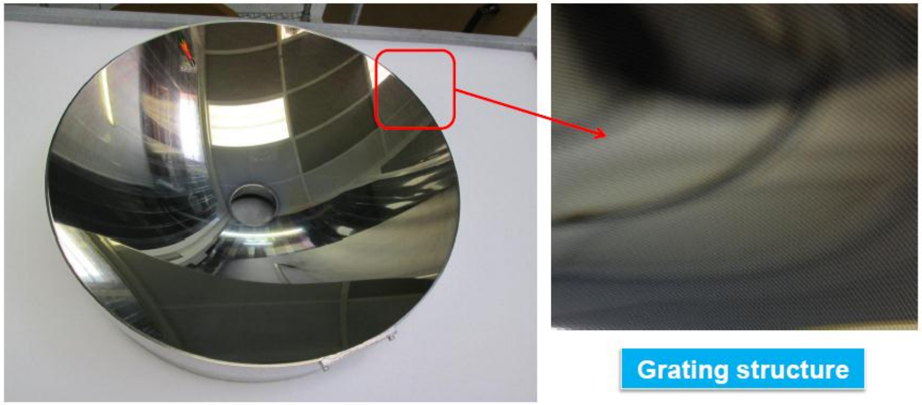
From Mizoguchi (Gigaphoton)

Transverse-flow:
Gas flow ⊥ Optical path



From Tanino *et al,* (Mitsubishi Electric)

Demonstration Collector: ~450mm dia (NA ~0.23)



Rigaku

2013 International Symposium on Extreme Ultraviolet Lithography

From Kriese *et al* (Rigaku)

Exposure Source Challenge to Source Community

- HVM insertion of EUV must be with existing LPP & drive laser technology
- In order for EUV to scale for future generations, we need dramatic power and COO improvements
- Are there alternate technologies for drive lasers or the EUV source that are better suited in the long term (say, HVM in ~2019)?

From Sivakumar, 2103 International Workshop on EUV Lithography

The Challenges of EUV

Resists

Patterning requirements…

- Resolution – On track
- LWR/Dose – Need high power

Outgassing - *Testing issues slow development*

- IDM TPT requirements
- Scanner outgassing requirements

Tool

Source

- Availability - *Critical*
- Power - *Critical*

Scanner Hardware
- On track

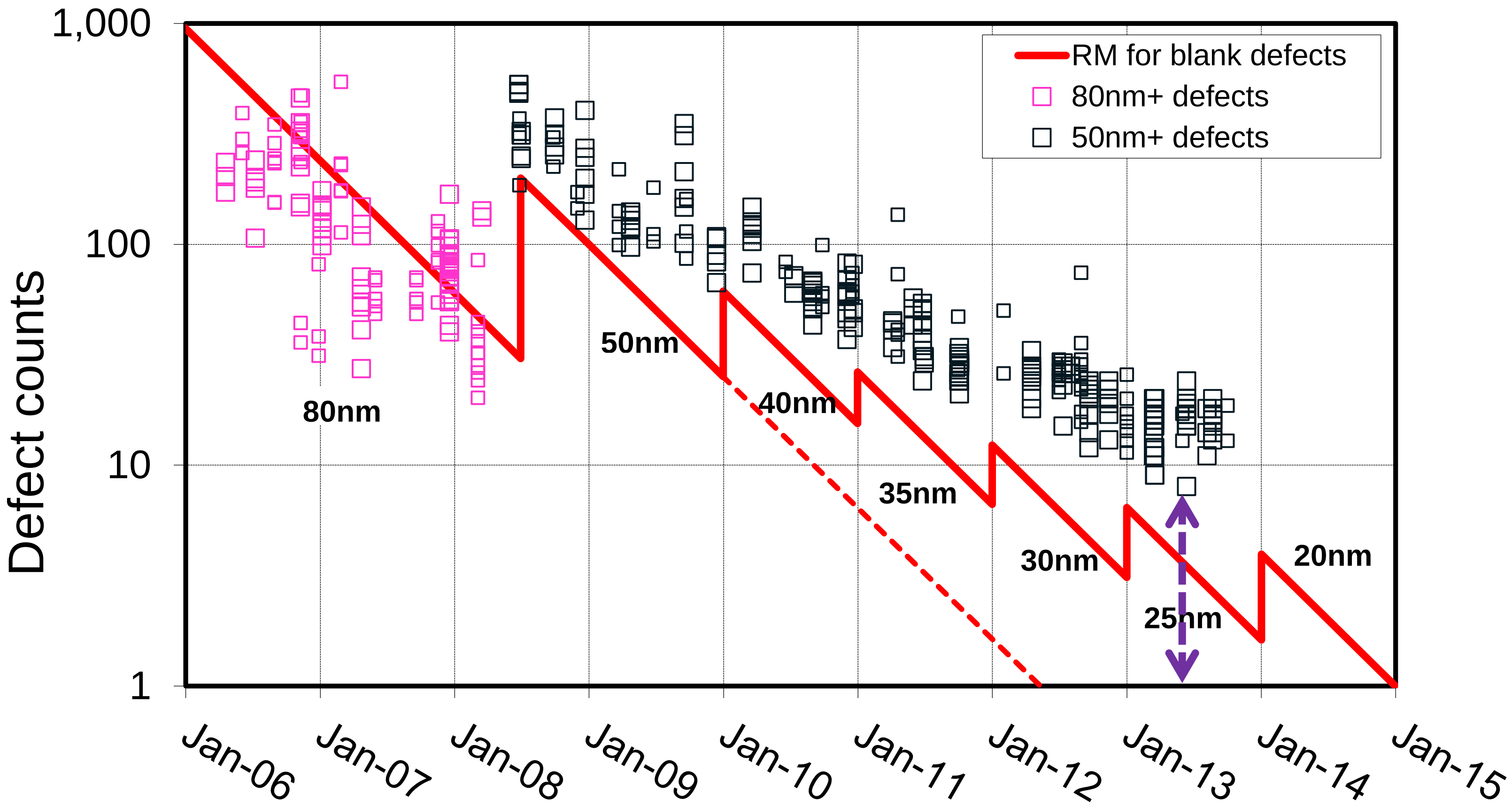
Reticle

Defectivity

- Killer defect impact >> wafer process defect impact
- Mitigation strategies
  - Reticle inspection
  - Patterned wafer inspection
  - Alternative strategies

EUV HVM implementation depends on satisfactory progress on all these fronts!

EUV Mask Blank ML Defect Reduction Trend

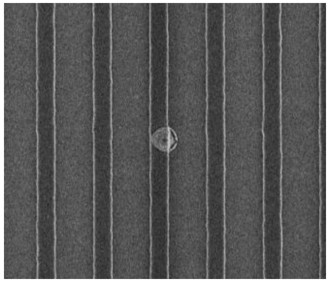


- Steady progress in reducing EUV mask bank defects
- Persistent gap with respect to the roadmap

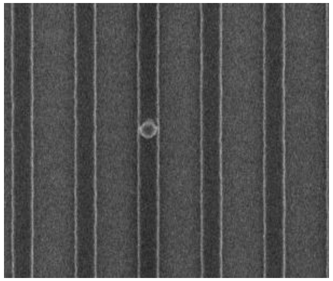
Blank ML defect mitigation with pattern shifting

Final mask SEM imaging

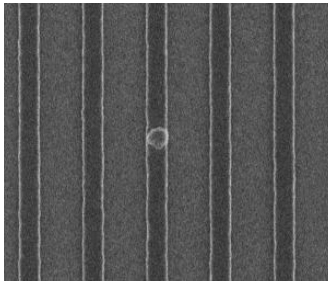
Defect #1

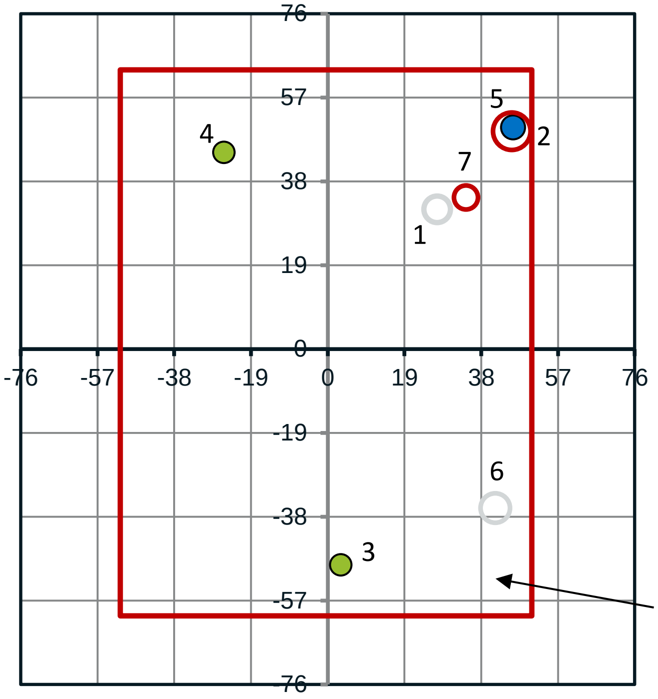


Defect #2



Defect #3



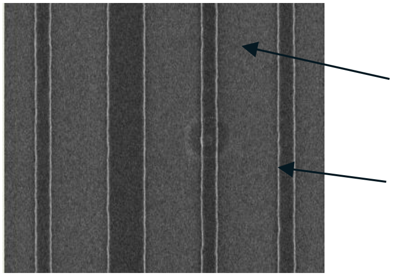


Device: 1X271B FBB-9EX

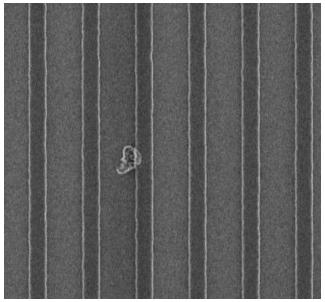
Blue circles: 3 defects mitigated (hidden under absorber)

Red circles: 4 partially or not covered but possibly repaired

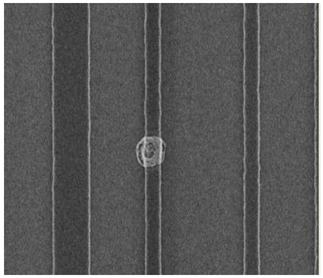
Defect #4



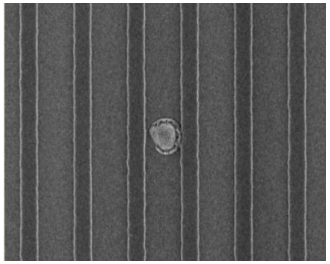
Defect #7



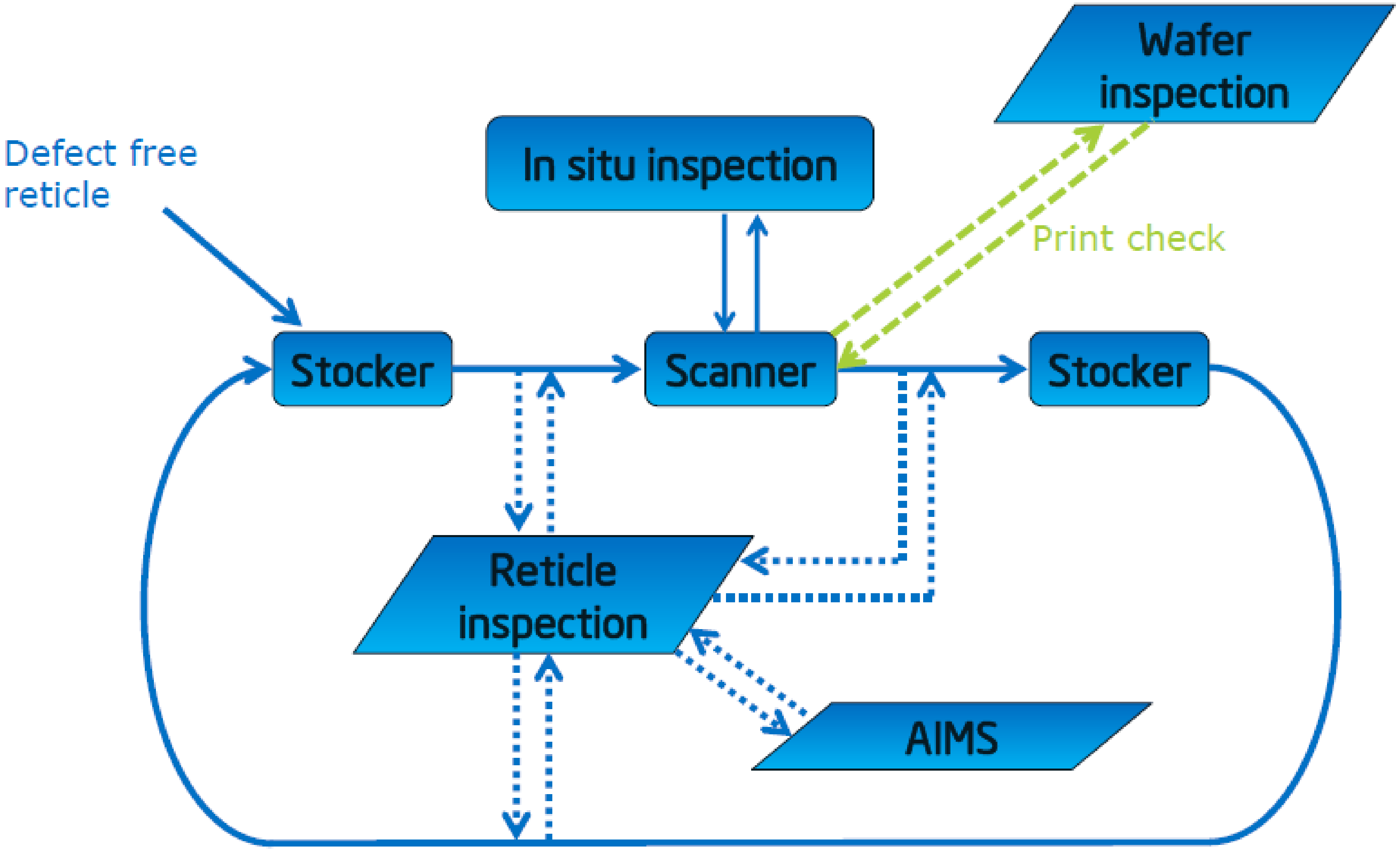
Defect #6



Defect #5



ArF In-Fab Reticle Flow



Defect free reticle

In situ inspection

Wafer inspection

Print check

Stocker

Scanner

Stocker

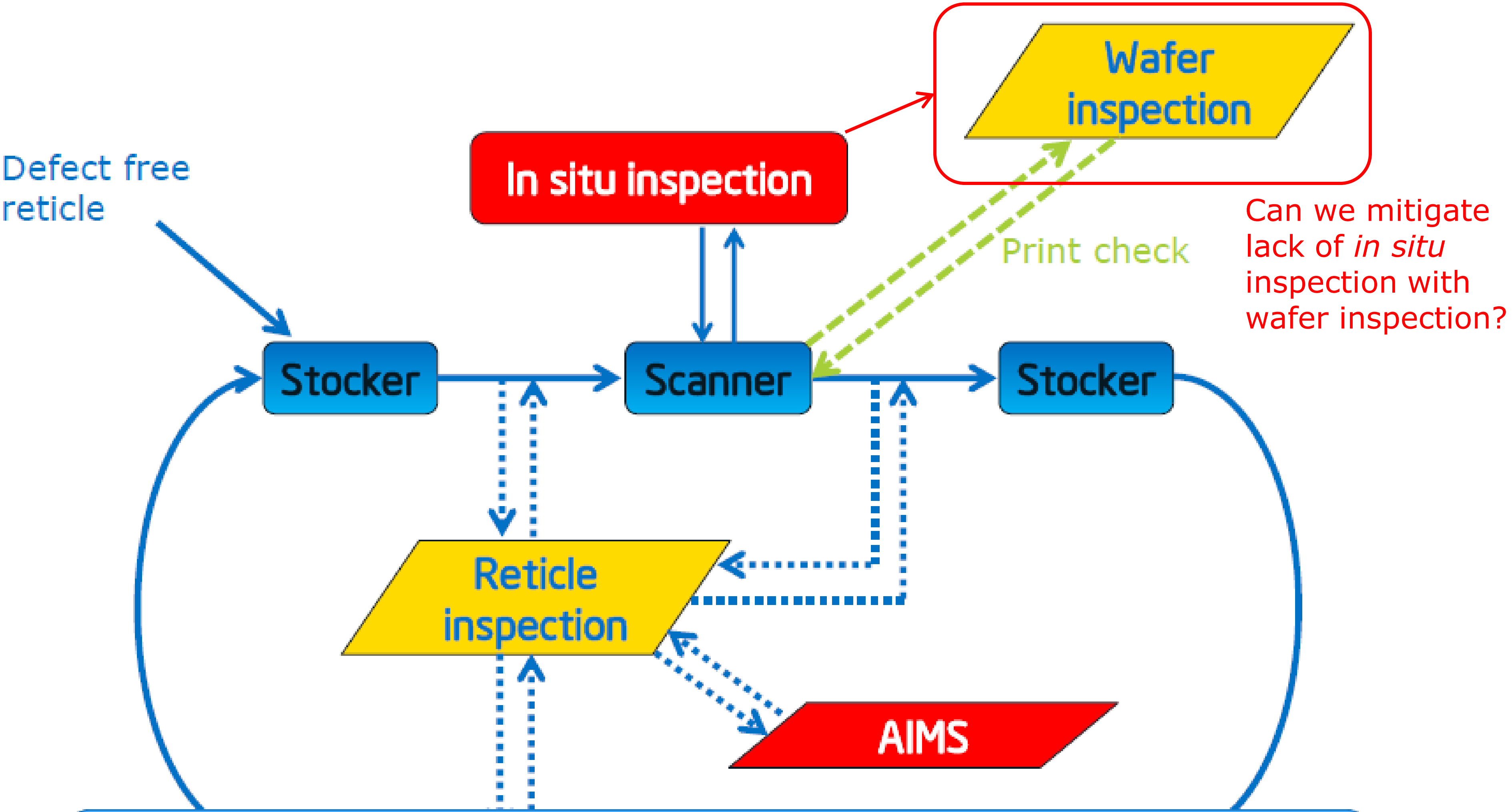
Reticle inspection

AIMS

Tim Crimmins, Litho Workshop 2012

Tim Crimmins,
Litho Workshop 2012

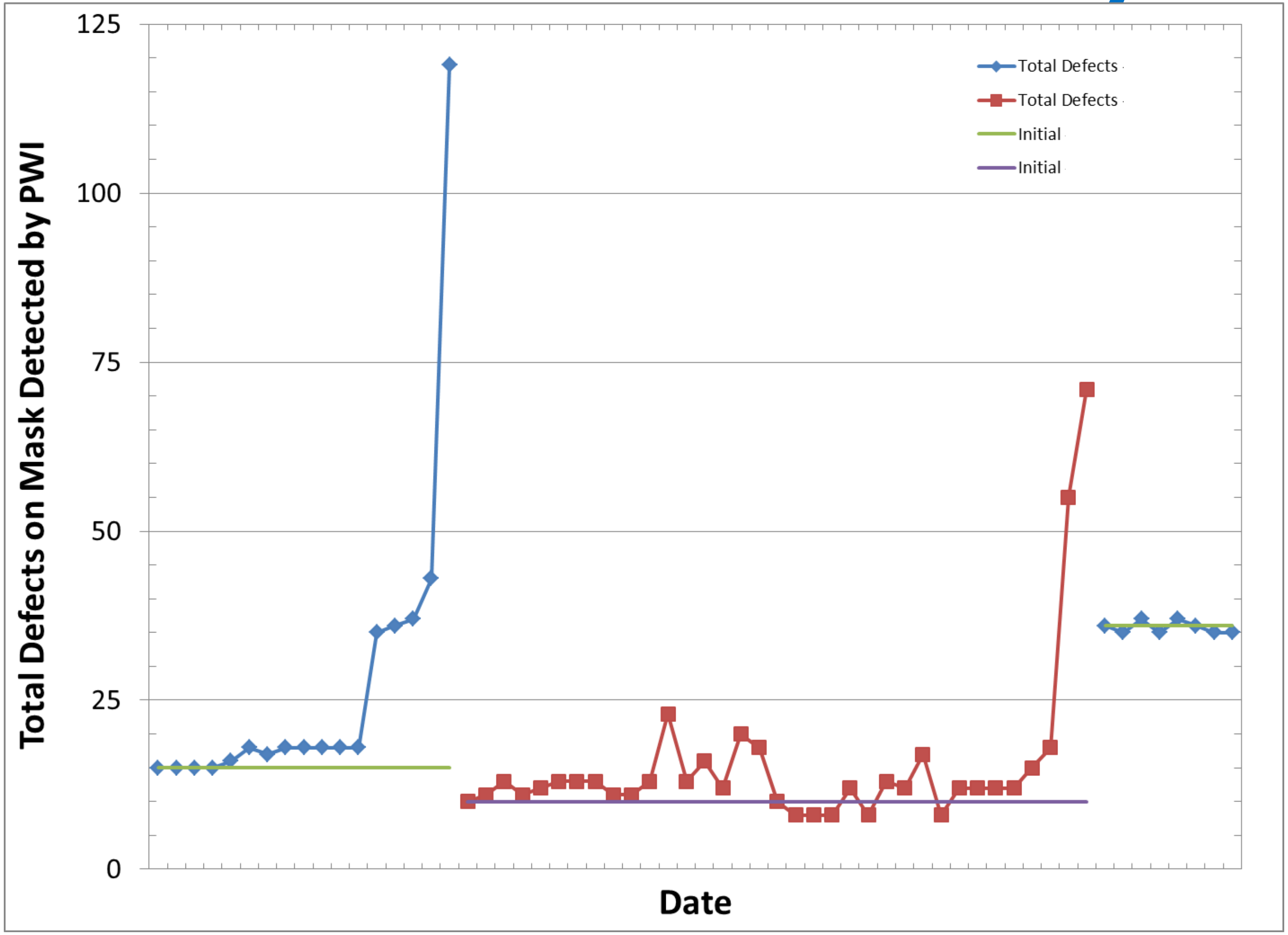
EUV In-Fab Reticle Flow



Can we mitigate lack of *in situ* inspection with wafer inspection?

Reticle, mask and wafer inspection metrology need to be ready to support the EUV launch

Specific Adder Events – Canary Mask



Reticle lives in tool ALL THE TIME!!!

Reticle defects added during wafer exposure

- Load 100x100 defect reticle on stage
- Shoot a defect wafer
- Cycle 3 dry wafers with same scanner job as above
- Shoot a defect wafer
- Repeat the steps in the red box 3 times

○ Adder

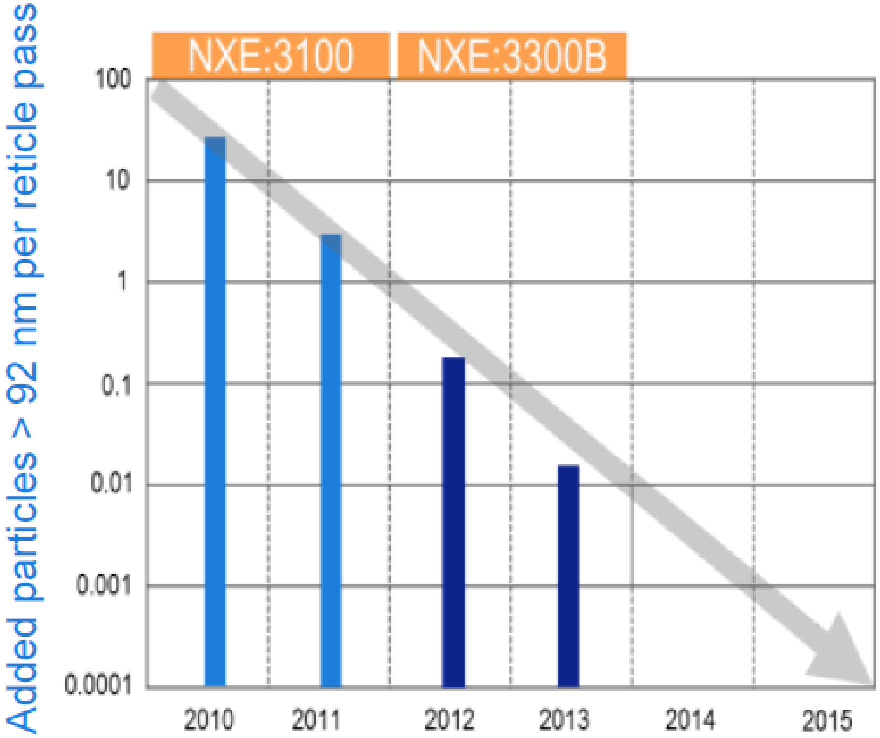
- Pass 1 is the first of 4 passes
- Adders are determined with respect to the cumulative particles in the previous passes

Measurement times

🟥	03/26/13 18:22:49
🟦	03/26/13 21:58:44
🟪	03/27/13 00:52:32
🟩	03/27/13 01:15:16

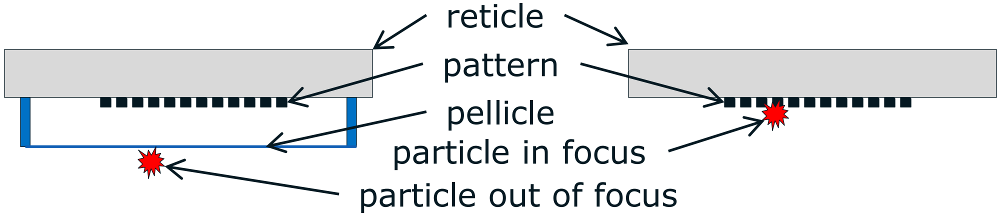
1) Reticles must be re-inspected after use
2) Wafers cannot leave area until post-inspection is passed

EUV Reticle Contamination



From Jim Wiley, IEUVI Mask TWG, 6 Oct 2013

- Steady progress
- What is required for success?
- Optical lithography OK with 0.01 particles per load for generations.
- Is this OK for EUV?
- For ≤193i, this is the probability of pausing to blow off pellicle
- For EUV without pellicle, this is the probability of an uncontained excursion
- Need PRP* < 0.0001



*PRP = added particles Per Reticle Pass

How long will it take to make EUV reticle defect experiments?

Testing to 0.01 PRP will take 12 hrs at full TPT

Testing to 0.001 PRP will take ~5 days

Testing to 0.0001 PRP will take ~50 days

At 0.0001 PRP, there will be no way to test a new tool; no way to run meaningful experiments; no way to debug/requalify problem tool.

→ Need EUV pellicle technology

ASML Pellicle Project overview

ASML pellicle program now in Phase 1 started early 2013

ASML

Public

Slide 6

2H '12	2013	2014	2015

Research and scoping of work

Phase 0

Prototyping phase – towards full-size pellicle incl lithographic performance

Phase 1

Phase 2

Industrialization

- Tested EUV transmission, deflection, heat loads, imaging
- Next step: continue scaling towards half size

Good progress in free standing material development

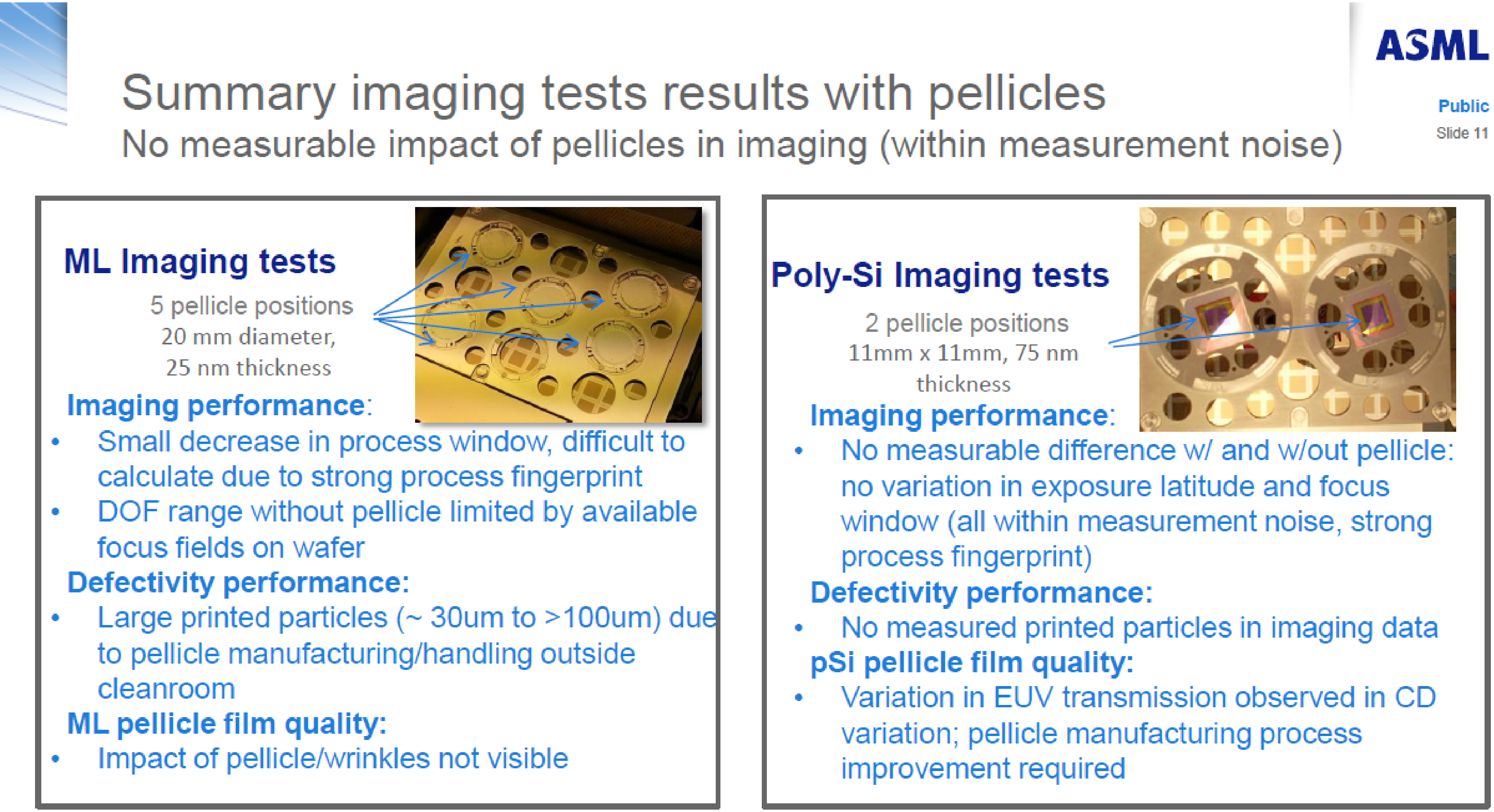
50mm x 50mm and 80mm x 80mm poly Si samples tested

½ size
~75mmx 115mm
planned for
2013

full size
~110mmx 144mm
planned for 2014

From Jim Wiley, IEUVI Mask TWG, 6 Oct 2013

Pellicle imaging test results



ASML

Public

Slide 11

Summary imaging tests results with pellicles

No measurable impact of pellicles in imaging (within measurement noise)

ML Imaging tests

5 pellicle positions
20 mm diameter,
25 nm thickness

Imaging performance:

- Small decrease in process window, difficult to calculate due to strong process fingerprint
- DOF range without pellicle limited by available focus fields on wafer

Defectivity performance:

- Large printed particles (~ 30um to >100um) due to pellicle manufacturing/handling outside cleanroom

ML pellicle film quality:

- Impact of pellicle/wrinkles not visible

Poly-Si Imaging tests

2 pellicle positions
11mm x 11mm, 75 nm
thickness

Imaging performance:

- No measurable difference w/ and w/out pellicle: no variation in exposure latitude and focus window (all within measurement noise, strong process fingerprint)

Defectivity performance:

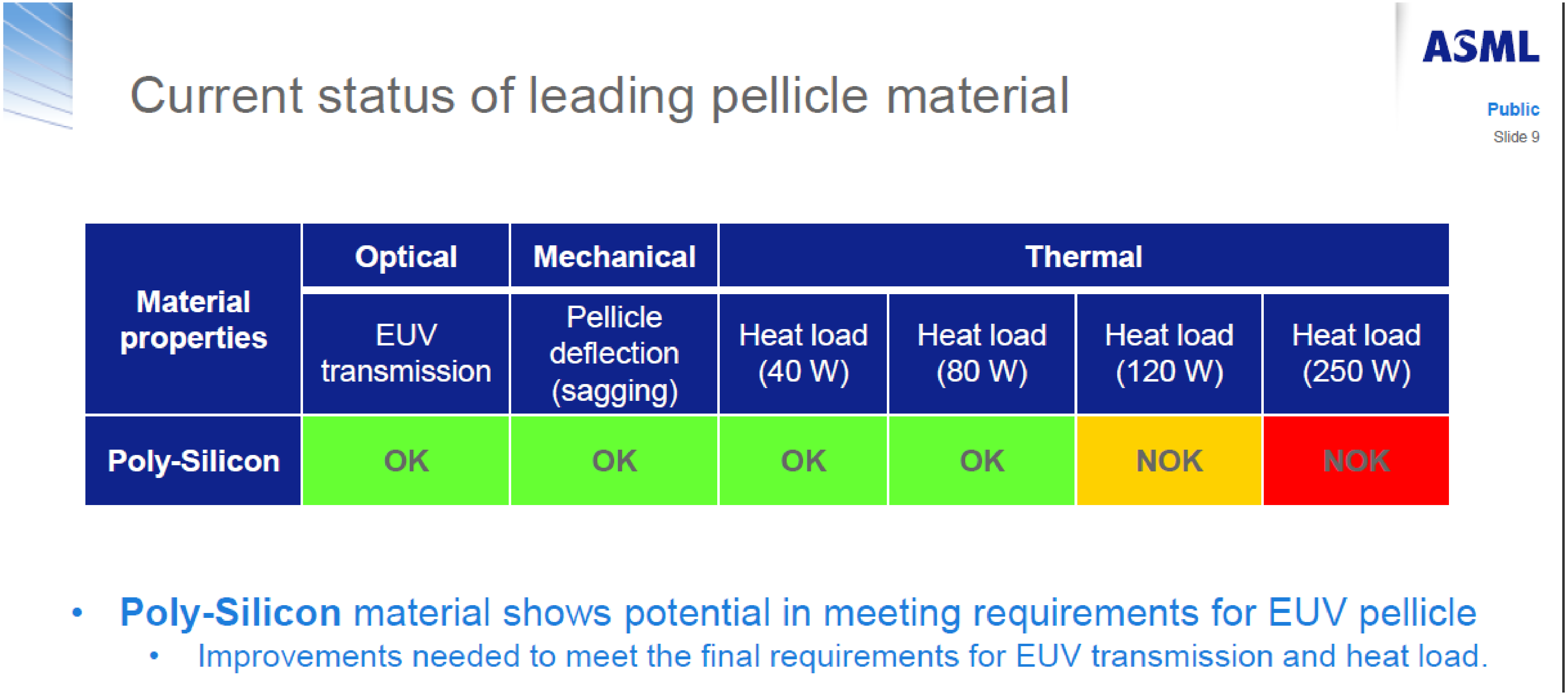
- No measured printed particles in imaging data

pSi pellicle film quality:

- Variation in EUV transmission observed in CD variation; pellicle manufacturing process improvement required

From Jim Wiley, IEUVI Mask TWG, 6 Oct 2013

Poly-Silicon is leading pellicle material



ASML

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Slide 9

Current status of leading pellicle material

Material properties	Optical	Mechanical	Thermal			
	EUV transmission	Pellicle deflection (sagging)	Heat load (40 W)	Heat load (80 W)	Heat load (120 W)	Heat load (250 W)
Poly-Silicon	🟩 OK	🟩 OK	🟩 OK	🟩 OK	🟨 NOK	🟥 NOK

- **Poly-Silicon** material shows potential in meeting requirements for EUV pellicle
    - Improvements needed to meet the final requirements for EUV transmission and heat load.

From Jim Wiley, IEUVI Mask TWG, 6 Oct 2013

From Sivakumar, 2103 International Workshop on EUV Lithography

The Challenges of EUV

Resists

Patterning requirements...

- Resolution – On track
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Outgassing- *Testing issues slow development*

- IDM TPT requirements
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Tool

Source

- Availability - *Critical*
- Power - *Critical*

Scanner Hardware - On track

Reticle

Defectivity

- Killer defect impact >> wafer process defect impact - *need pellicle*
- Mitigation strategies
    - Reticle inspection - ?
    - Patterned wafer inspection - *not a substitute for A-PI or pellicle in HVM*
    - Alternative strategies

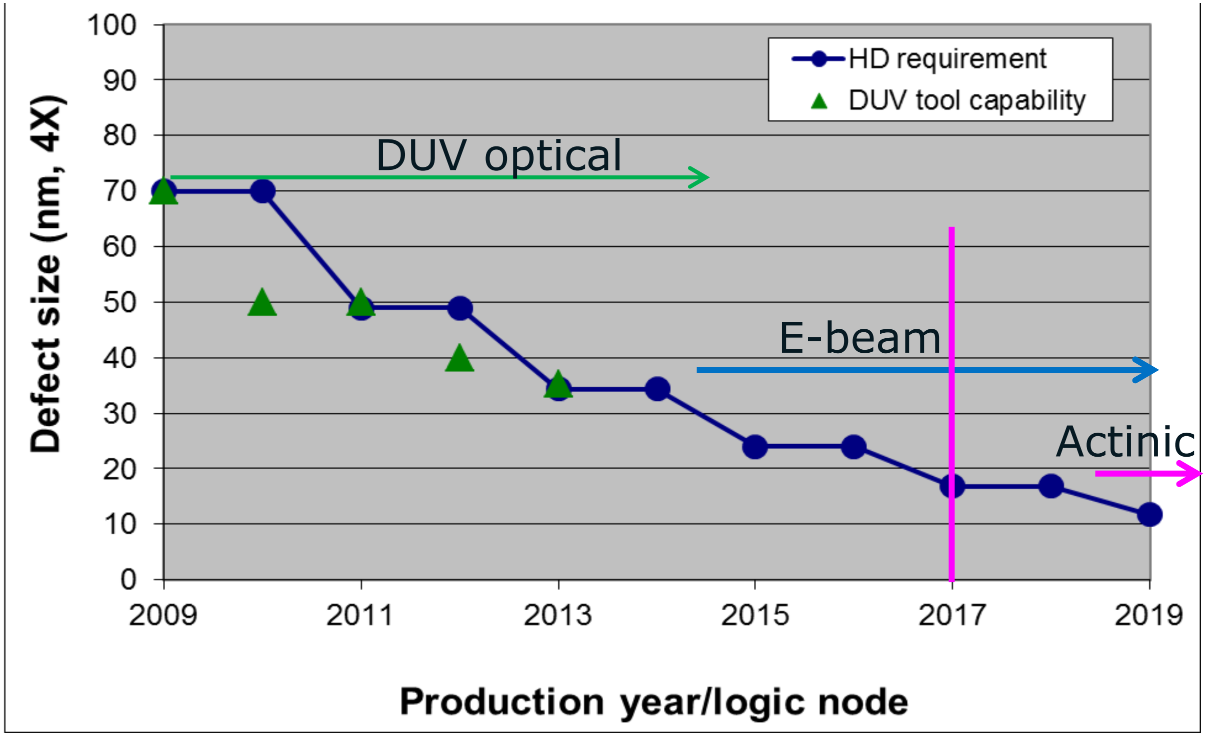
EUV HVM implementation depends on satisfactory progress on all these fronts!

EUV actinic metrology for reticles

Three actinic metrology techniques are critical for EUVL in HVM

- A-BI: actinic blank inspection, to check quality of multilayer reflector stack
- A-PI: actinic pattern inspection, to detect minimum printing particles, and inspect through pellicle
- EUV AIMS: actinic aerial image metrology, to determine defect printability

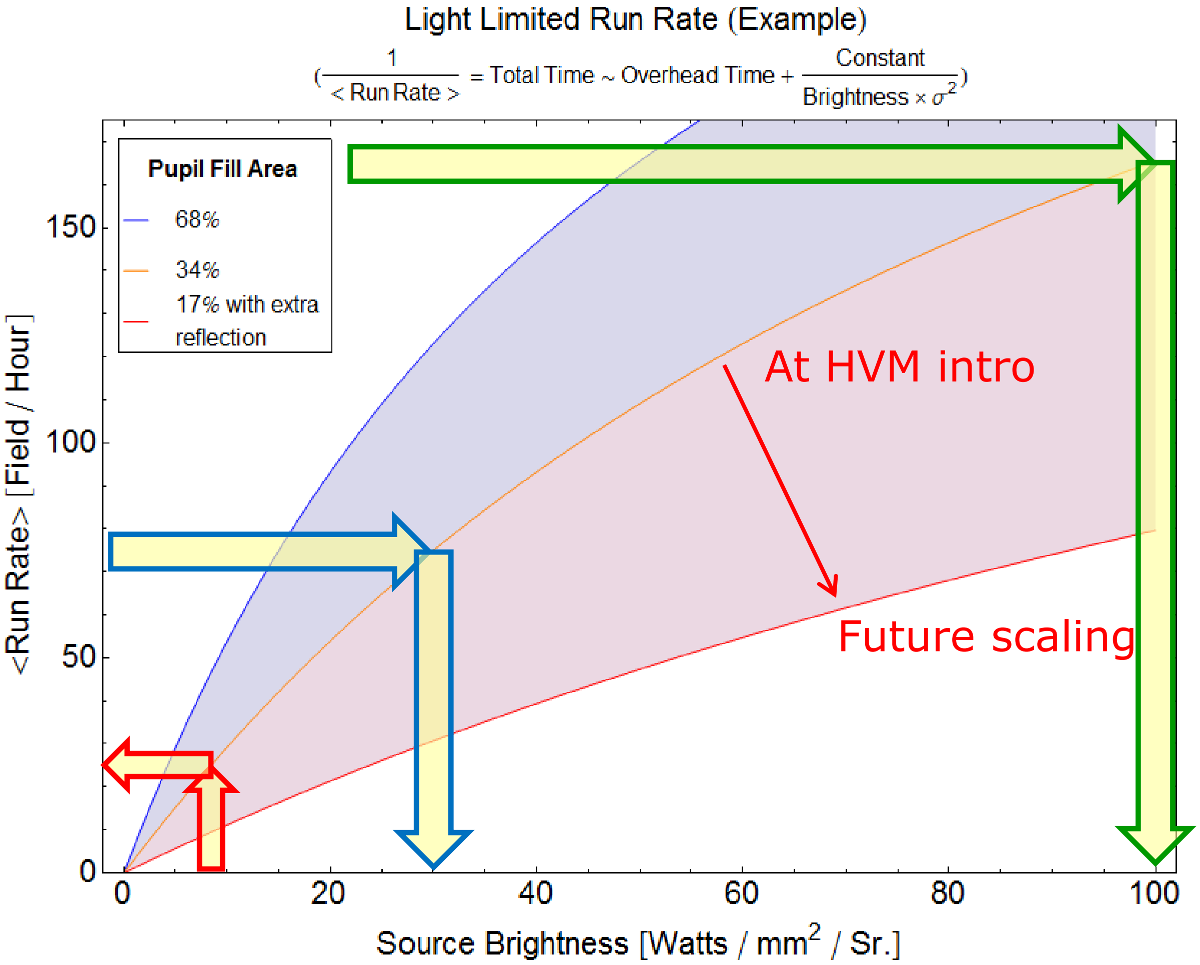
EUV reticle inspection requirements versus capability



- Optical inspection tools (193nm inspection wavelength) are currently used in pilot-line for defect learning
- Projected E-beam tool availability from 2014
- Beta-phase capable actinic capability needed in 2017 for pattern, and thru-pellicle pattern inspections
  - > 1 year delay exists already in the current roadmap

Why Brightness Matters (canonical AIMS model)

Estimates by Michael Goldstein (Intel)



This is what the industry *wants*. ⇨ ⇨ ⇨

This is the need. ⇨ ⇨ ⇨

This is about where we are. ⇨ ⇨ ⇨ ⇨

Challenge to actinic metrology source community

Based on input from metrology tool suppliers and Intel metrology experts:

- Existing sources do not meet brightness, homogeneity, stability, and COO requirements
  - Requirements are feasible, but already late to need
  - Requires focused development activity and funding
- Requirements are specific to each tool design, and are proprietary
  - Source is an integrated part of tool design
  - Correct model is funding through metrology tool suppliers

From Sivakumar, 2103 International Workshop on EUV Lithography

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Reticle

Defectivity

- Killer defect impact >> wafer process defect impact - *need pellicle*
- Mitigation strategies
  - Reticle inspection - *A-PI late, sources for A-PI, AIMS, A-BI are inadequate*
  - Patterned wafer inspection - *not a substitute for A-PI or pellicle in HVM*
  - Alternative strategies

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Conclusions

- Realization of 40~80W stable MOPA+PP sources in the field linked to NXE:3300B scanners over next two quarters looks feasible
- This would enable meaningful integrated process development with 0.33 NA EUVL and re-establish confidence in a source power roadmap to HVM levels
- Need to re-invigorate EUVL infrastructure development, especially:
  - Exposure source power scaling beyond 250W with dramatically improved COO
  - Actinic metrology source development to meet performance, productivity, COO and schedule
  - Commercial EUV pellicle infrastructure

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