EUV: The Computational Landscape

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EUVL Workshop, 2014

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Outline

- What the world wants (hint: 3D transistors)
- Lithography: Choices for 14 nm and 10 nm
  - Inverse lithography and SMO
  - “Double” patterning
  - EUV lithography
- Computational techniques for EUV
  - Flare
  - Shadowing
  - Out of band radiation

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The World Ahead

Connecting People to a World of Opportunity

Access

Making Technology Available To More People

Connectivity

Extending Broadband Connections

Education

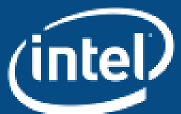
Transforming Education To Improve Teaching And Learning

Healthcare

Delivering Innovative Healthcare Solutions

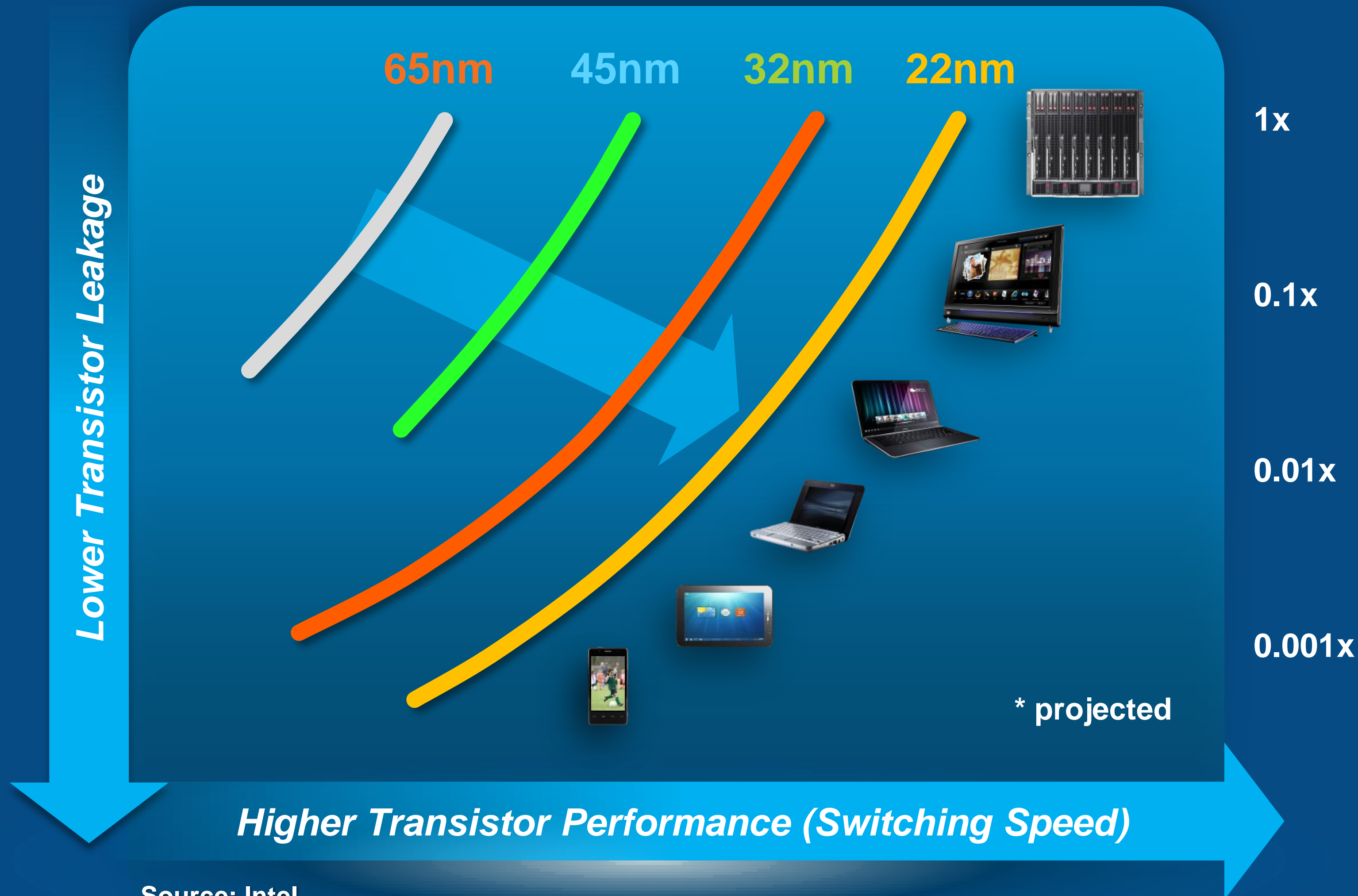
Needs a Continuum of Personal Computing Experiences

Desktops | Laptops | Ultrabook™ | Tablets | Smartphones | Intelligent Systems



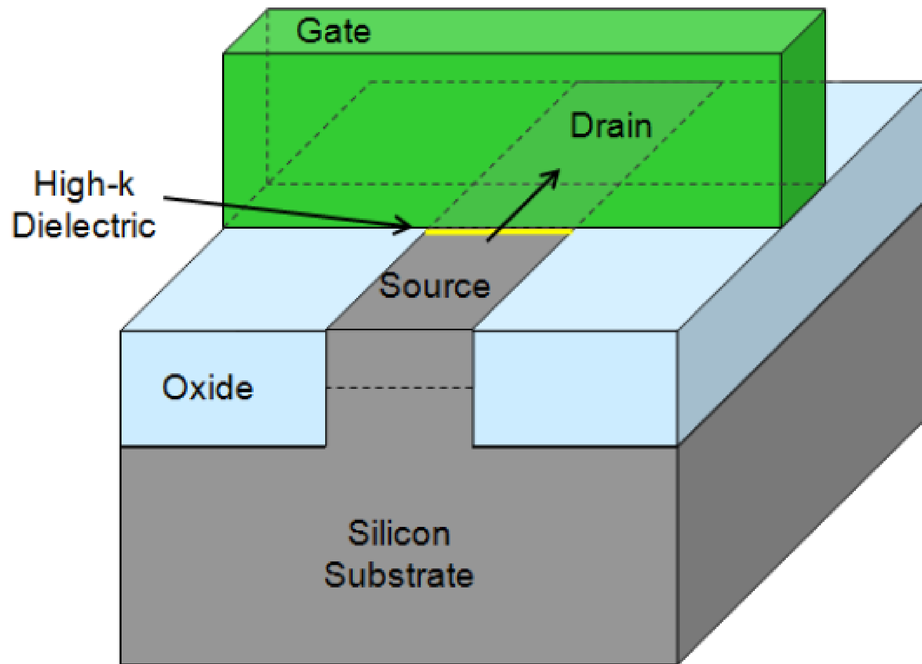
And that needs leading edge technology

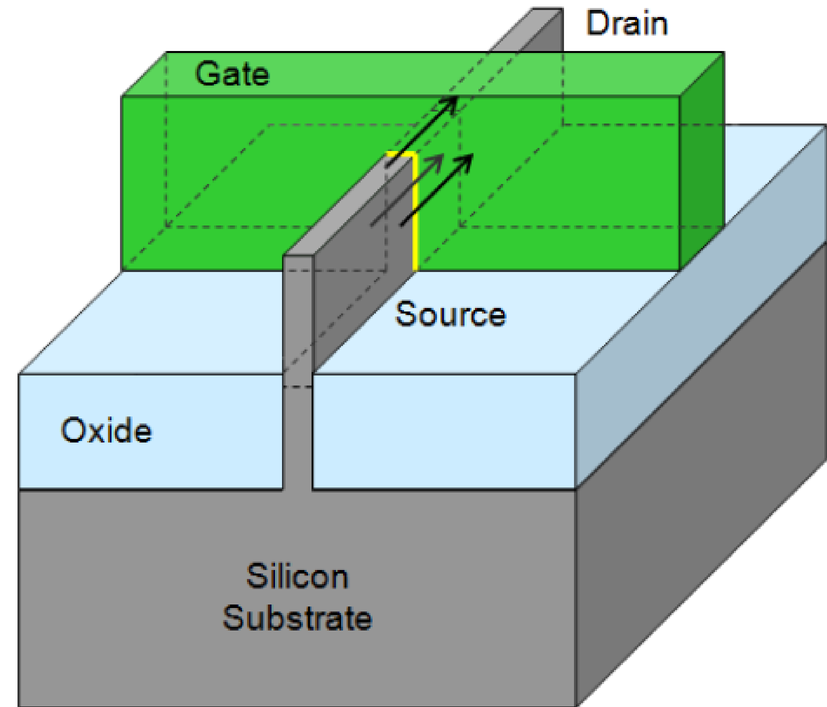
Every new node: more performance on more features at lower power



Source: Intel

Such as... 3D transistors!





Intel 22nm technology introduces revolutionary 3-D Tri-Gate transistors

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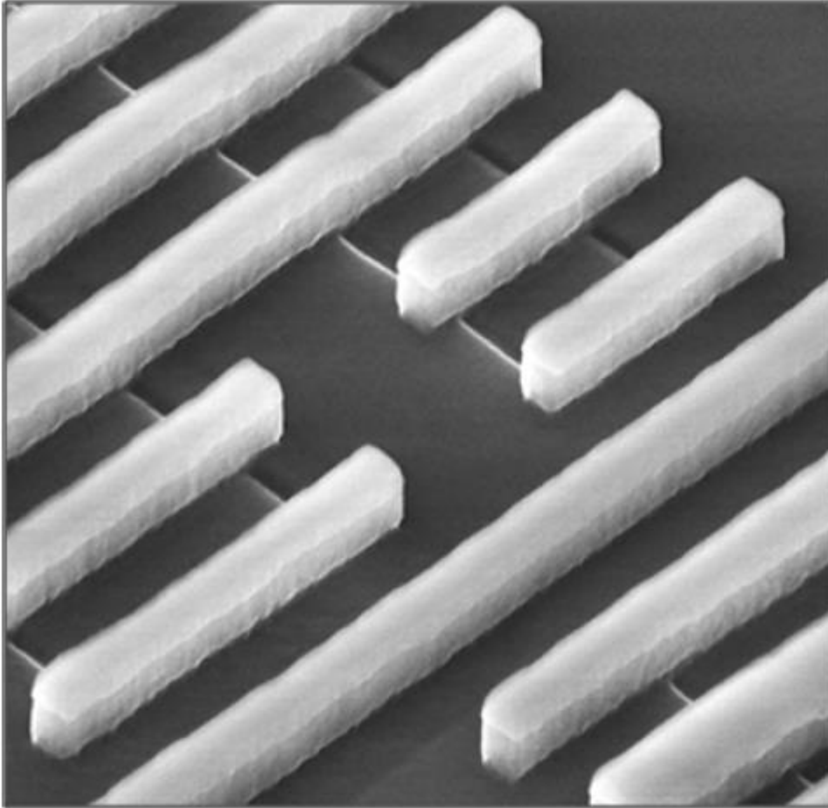
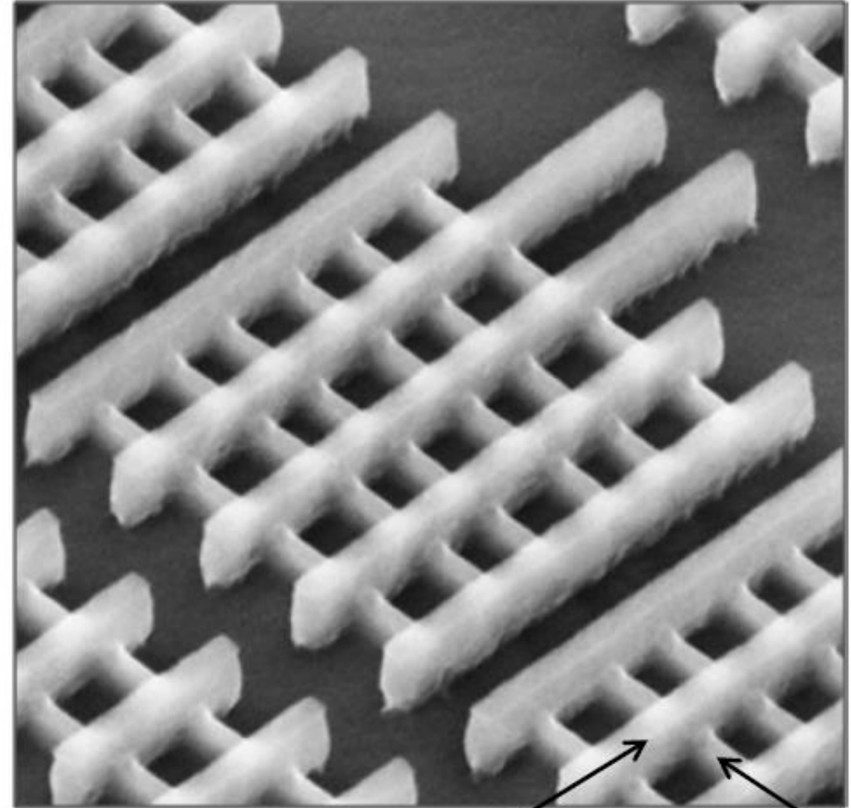
Real, high volume stuff

32 nm Planar Transistors



22 nm Tri-Gate Transistors



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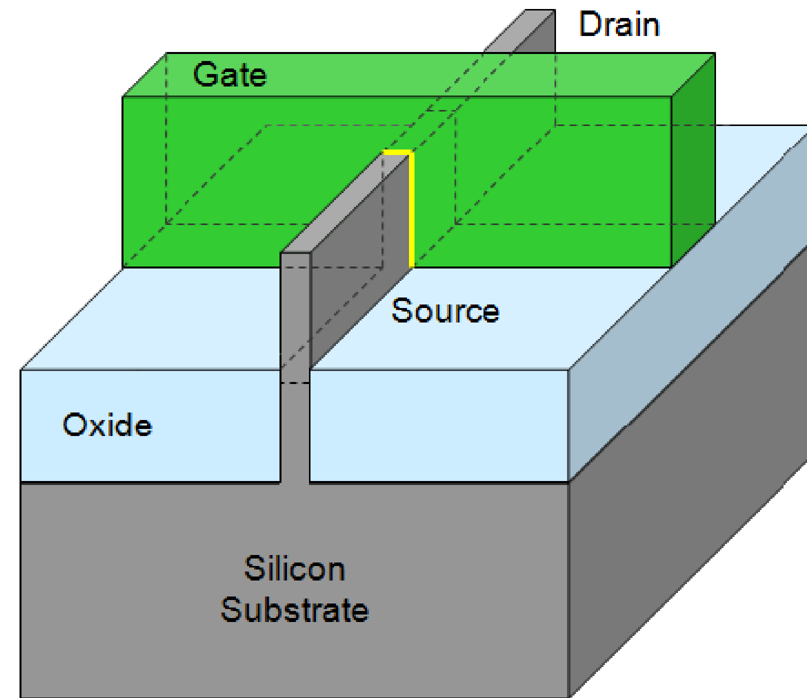
22nm Tri-Gate Transistor Benefits

- 37% performance increase at low voltage
- 50% power reduction at constant performance
- Adds only 2-3% wafer cost compared to 22 nm planar
- Planar transistors can not provide expected performance and power improvements at 22 nm



Moore's Law, at its heart, is about continuing innovation to give the world what it wants

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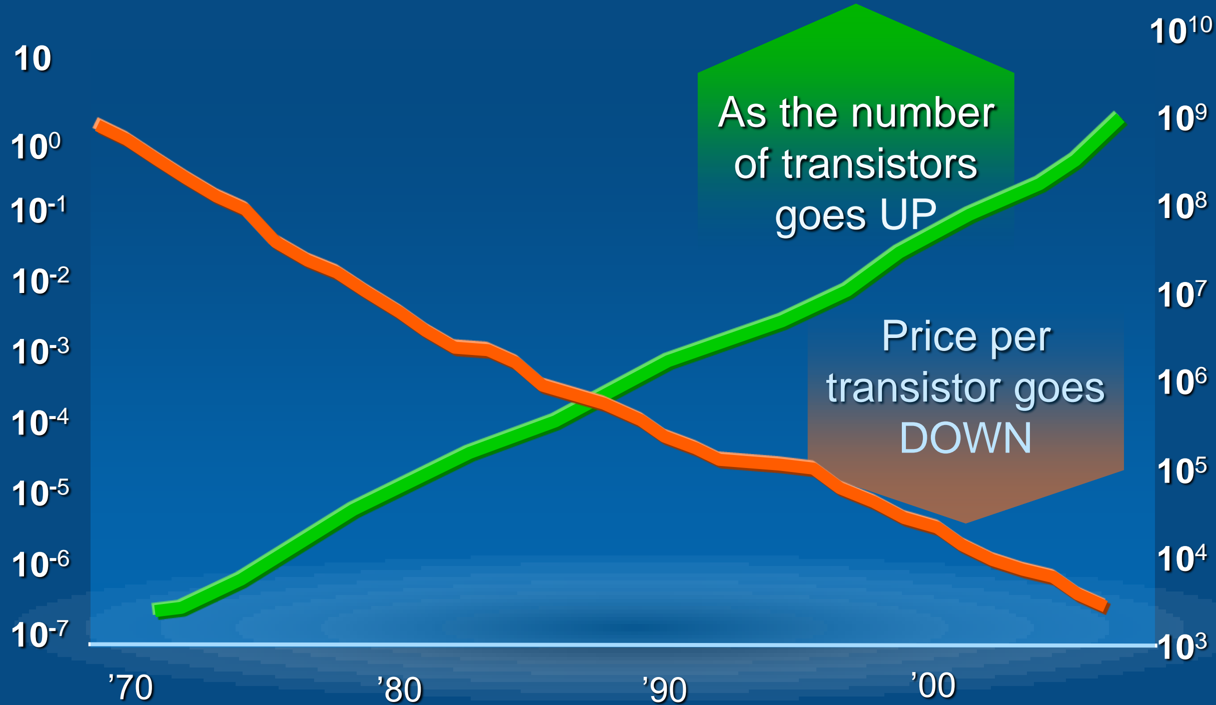
But can we afford Moore's Law?

The Benefit:



Source: WSTS/Gartner/Intel

The Cost:

FAB	$4 B
PILOT LINE	$1-2 B
R&D PROCESS TEAM	$0.5-1 B

Source: Intel

Yes. It makes our gadgets cheaper.

The End of Scaling is Near?

Various industry comments over the past 30 years

"Optical lithography will reach its limits in the range of 0.75-0.50 microns"

"Minimum geometries will saturate in the range of 0.3 to 0.5 microns"

"X-ray lithography will be needed below 1 micron"

"Minimum gate oxide thickness is limited to ~2 nm"

"Copper interconnects will never work"

"Scaling will end in ~10 years"

Source: Mark Bohr ISSCC keynote, Feb. 2009

To paraphrase Mark Twain, rumors of Scaling's death are greatly exaggerated

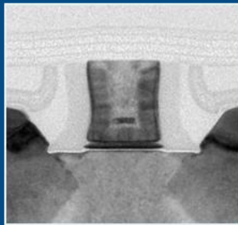
In 2014, things look no different

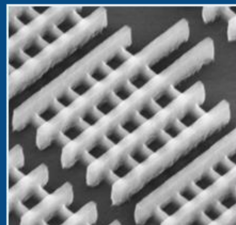
Innovation-Enabled Technology Pipeline is Full

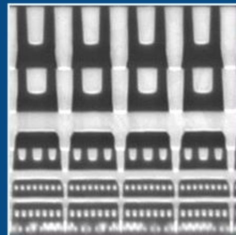
45nm
World's 1st
High K/
Metal Gate

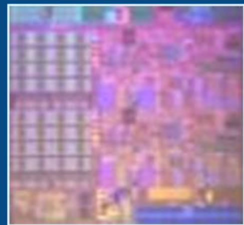
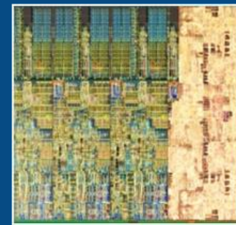
32nm
World's 1st
2nd Gen High K/
Metal Gate

22nm
World's 1st
Trigate
Transistors



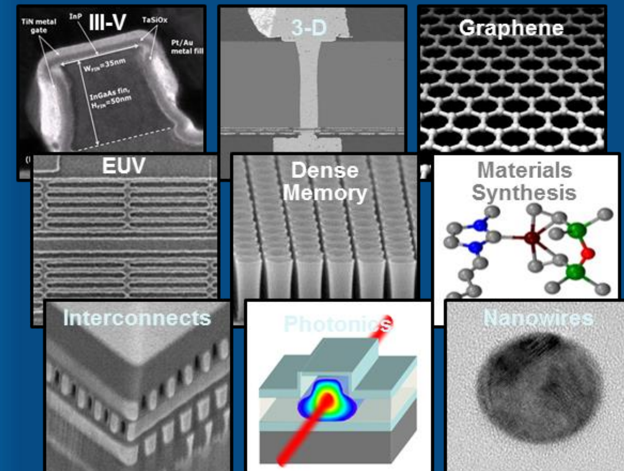




Source: Intel

Future
Better Performance
Lower Power
Higher Density and Integration
New Materials and Equipment
Lower Cost Per Transistor



Future options subject to change

Our limit to visibility goes out ~10 years

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Moore's Law: circa 2008

Intel® Atom™ - dual-core

Rice – single grain

47 Million Transistors
45nm node
Hi-k Metal Gate
193 dry Litho

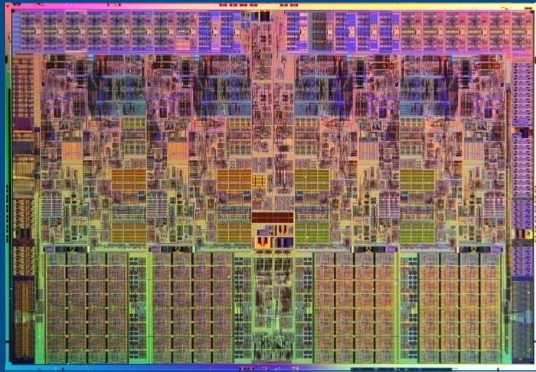
In 2012, on 22nm technology, the above chip would be ¼ the size
- Smaller than the grain of rice!

Moore's Law: circa 2010

Intel® Xeon® 5500 Processor
(Gainstown), 45 nm Hi-k
731M Transistors, 4 Core, 8 MB Cache

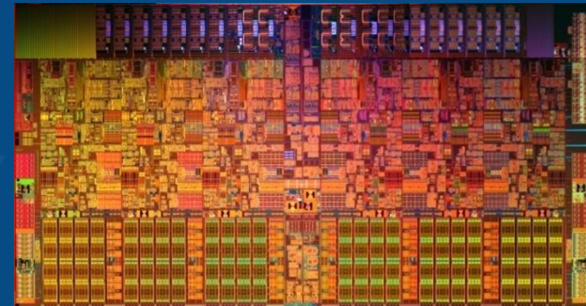
Intel® "Westmere-EP" Processor
(Gulftown), 32 nm 2nd Generation Hi-k
1.17B Transistors, 6 Core, 12 MB Cache

45 nm



50% More Cores
50% More Cache

sistors/mm²



32 nm

263 mm²

240 mm²

Perf.	130W	4 Core, 3.33 GHz	→	6 Core, 3.33 GHz
Volume	95W	4 Core, 2.93 GHz	→	6 Core, 2.93 GHz

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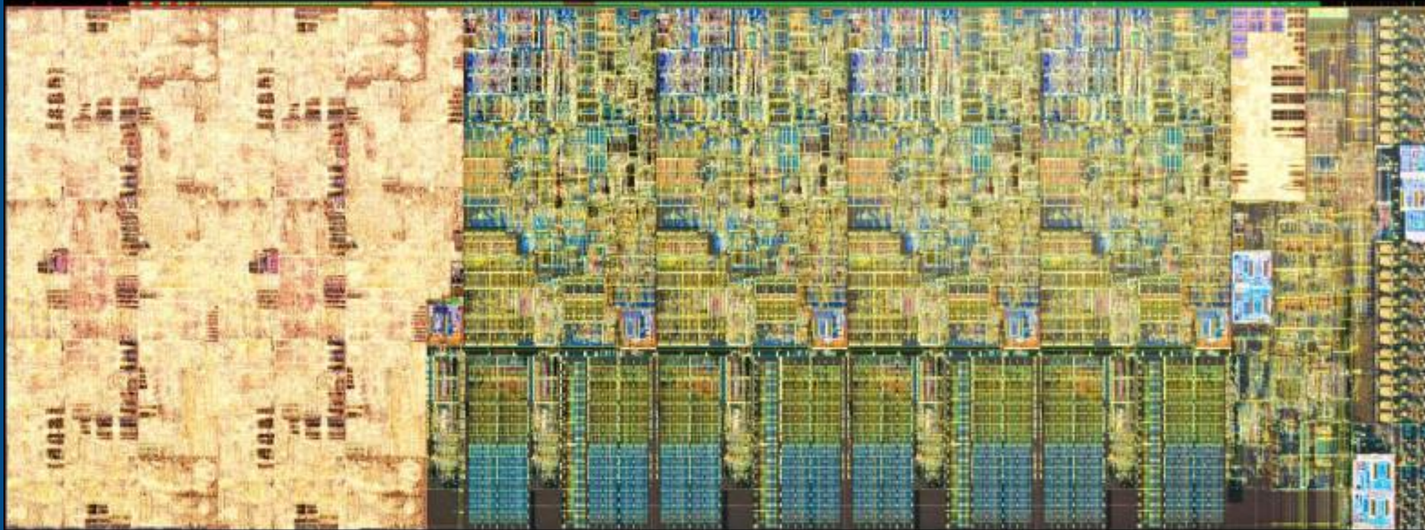
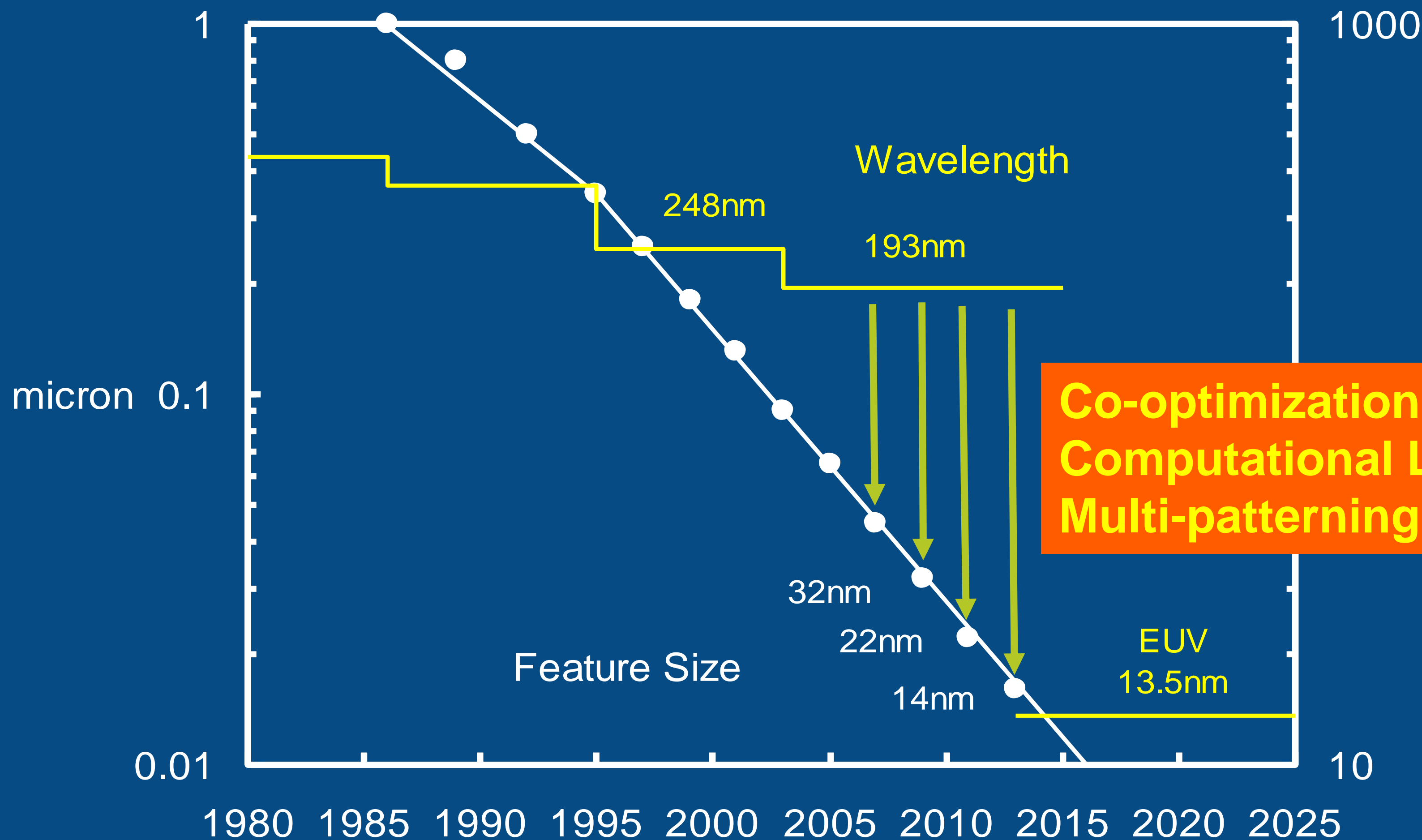
Moore's Law: circa 2012



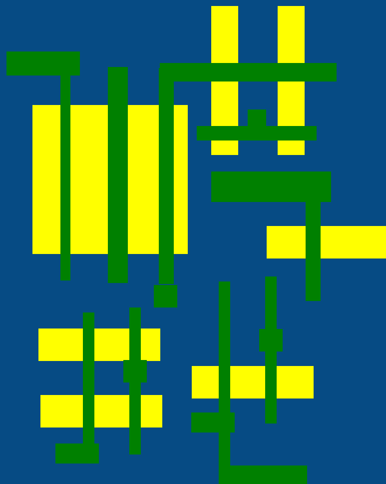
22nm Intel Microprocessor codenamed Ivy Bridge
(image released at Sept IDF)

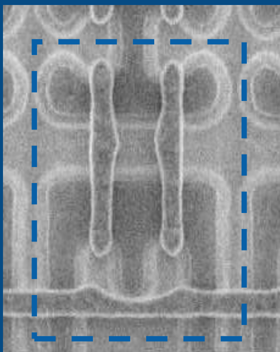
Too small for the light we use…
…have to find ways to bridge the gap



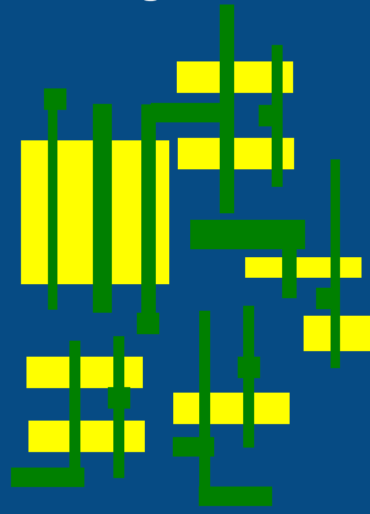
Co-optimization: Living within your means

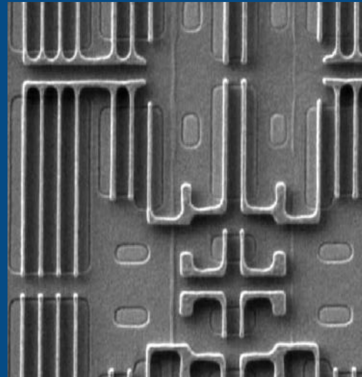
90nm
- All gates in one direction except SRAM.



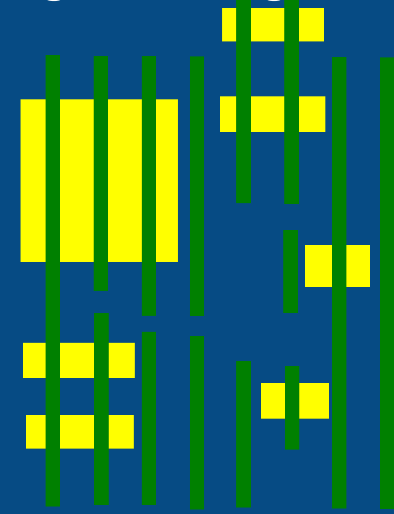


65nm
- All gates in one direction everywhere.
- Different rules for minimum pitch, larger gate pitch and gate routing.

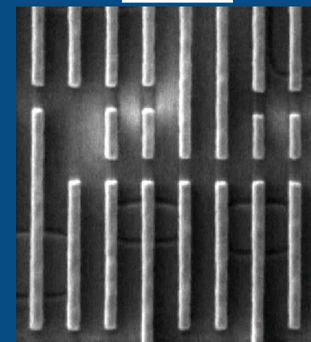




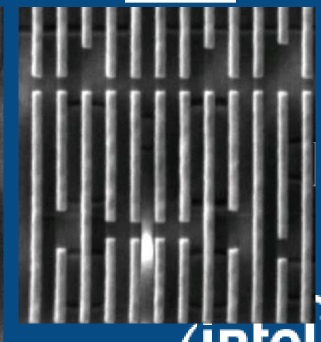
45nm/32nm
- All gates in one direction and one pitch.
- Trench contact local routing replaces orthogonal to gate routing.



45nm

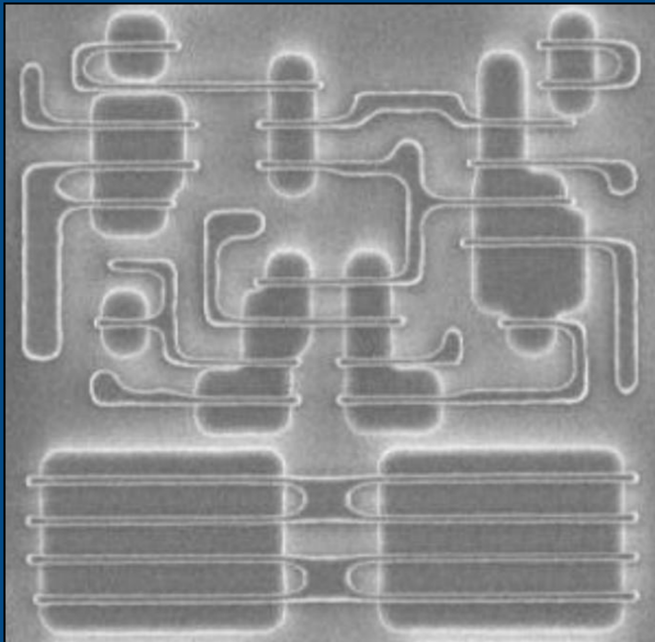


32nm



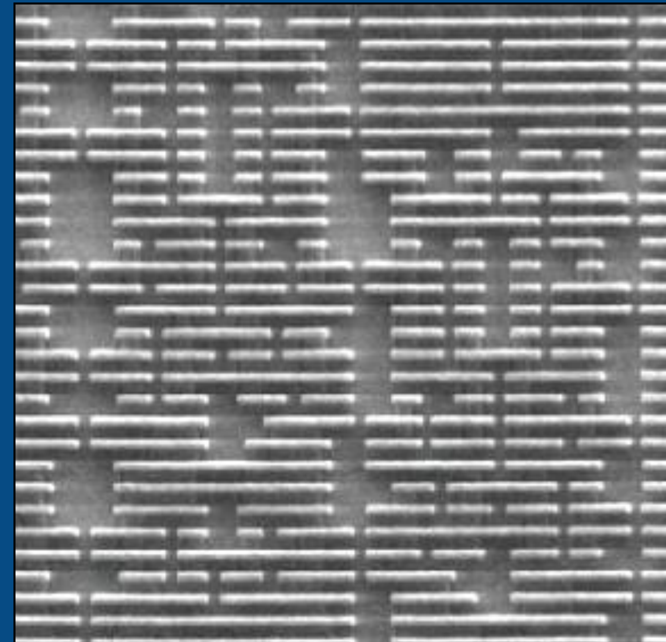
Layout has adapted to litho constraints, without affecting Moore's march

65 nm Layout Style



- Bi-directional features
- Varied gate dimensions
- Varied pitches

32 nm Layout Style



- Uni-directional features
- Uniform gate dimension
- Gridded layout

M. Bohr, ISCC, 2009

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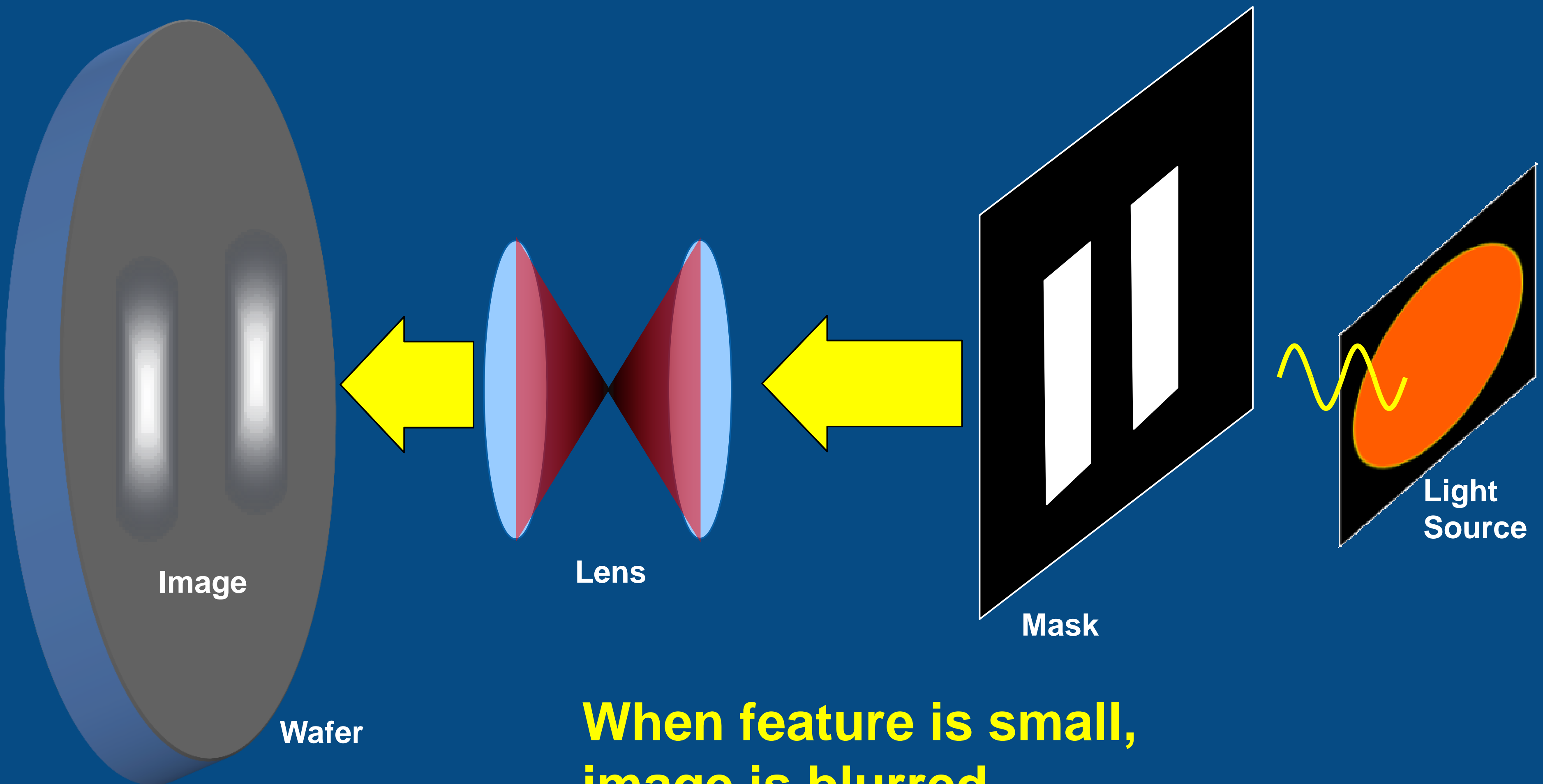
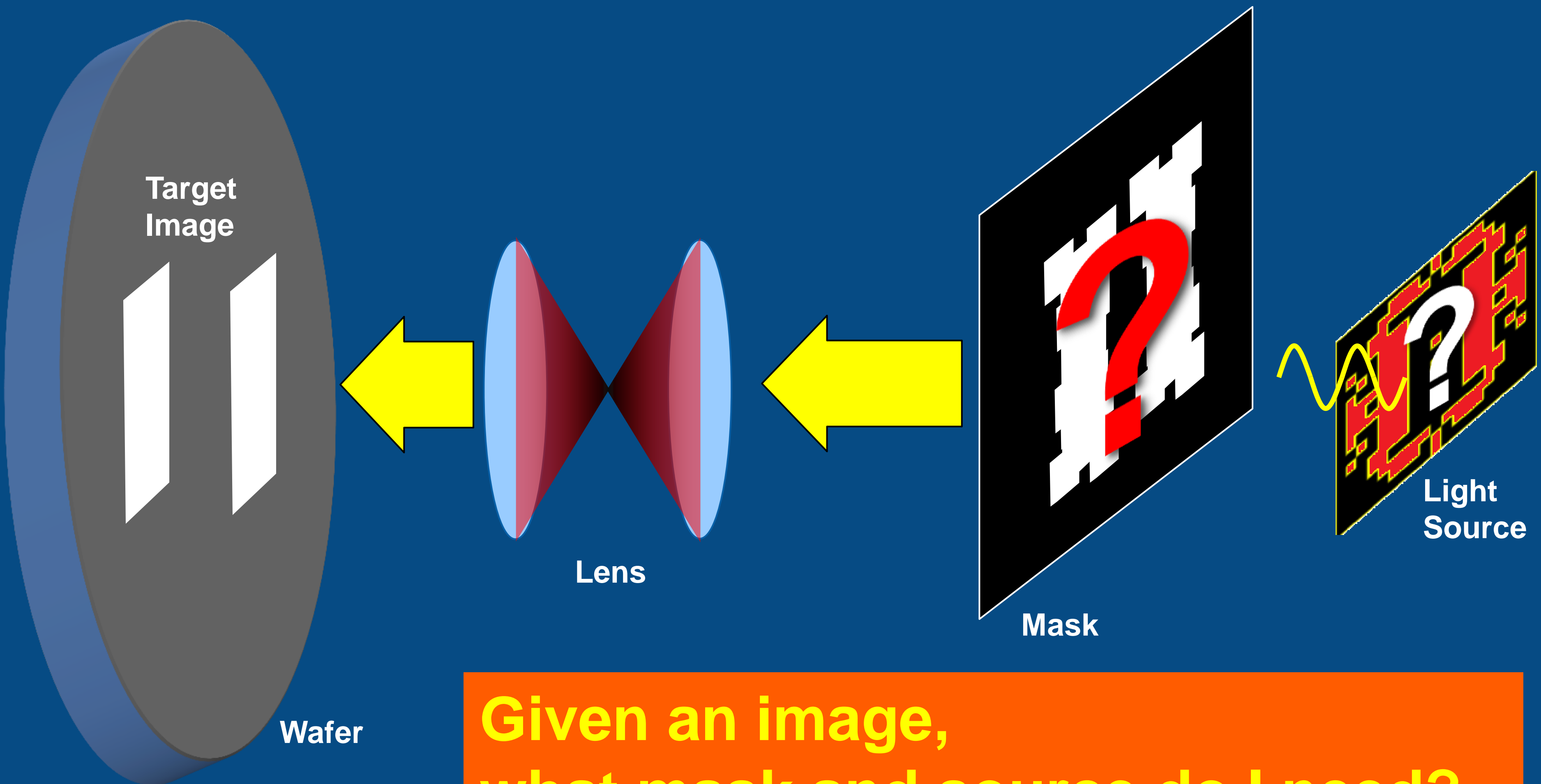
Lithography stepper, simplified



When feature is small, image is blurred

Can we "bend" light by inverting the problem?



**Given an image,
what mask and source do I need?**

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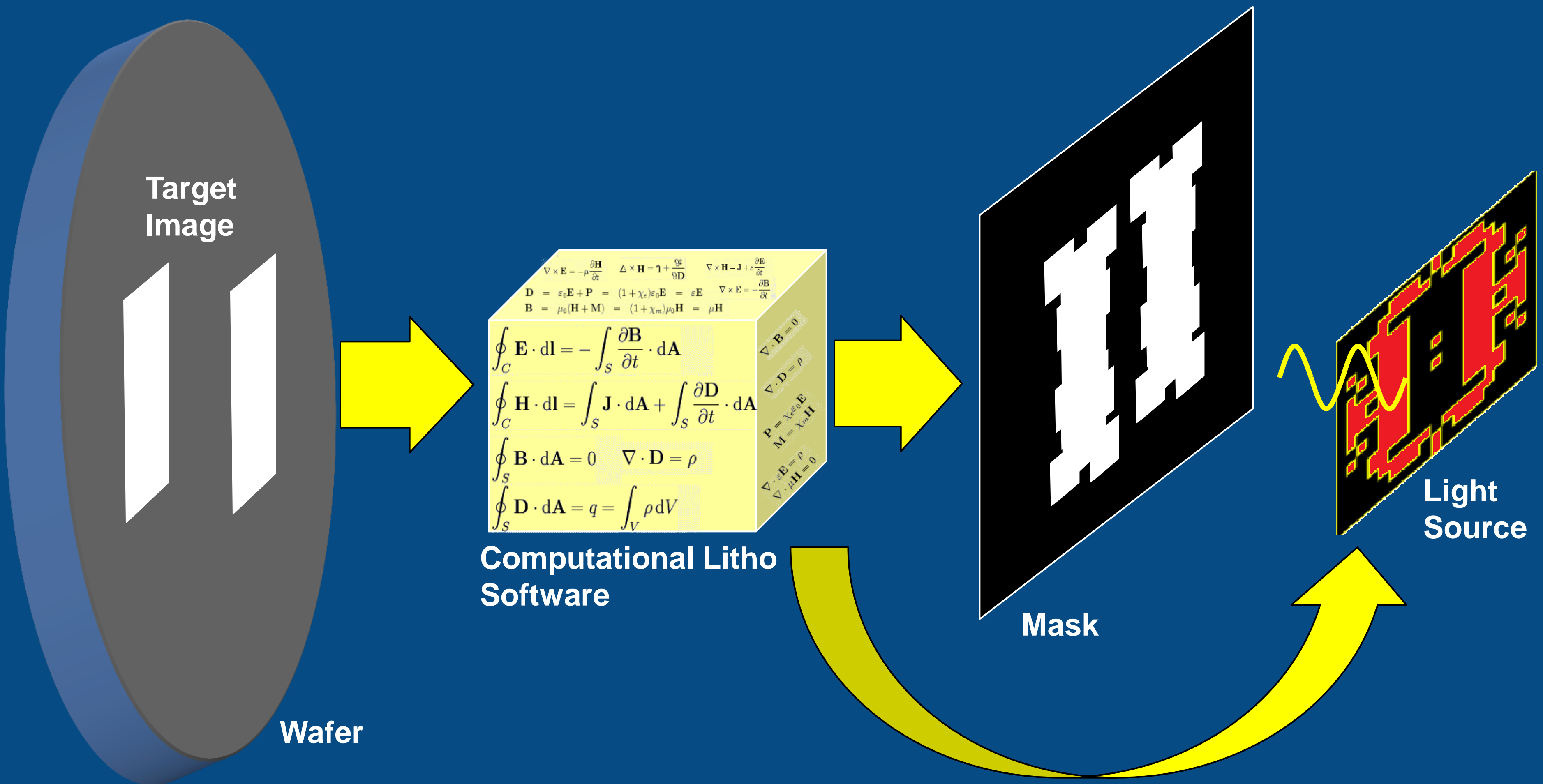
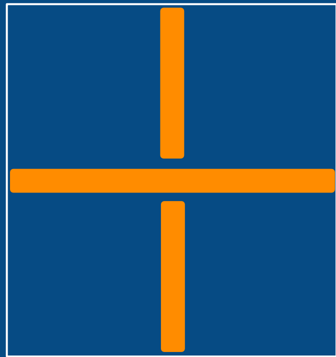
Answer: Inverse Lithography (ILT)

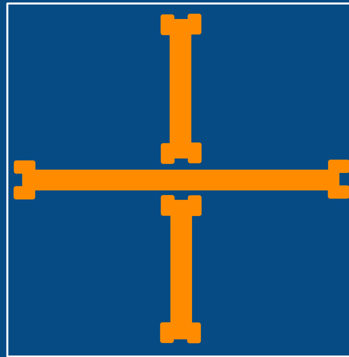
Input = design,   Output = mask + source



Increasing need for mask "correction"



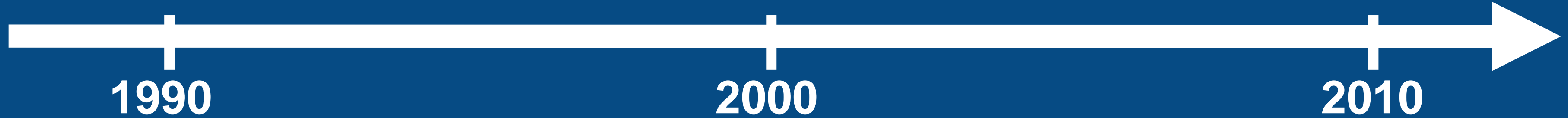
no correction



dog ears

model-based OPC

OPC + rule based assist features



- From simple decorations to complex "distortions"
- Intuition finally breaks down, optimal solution comes from math/computation

ILT

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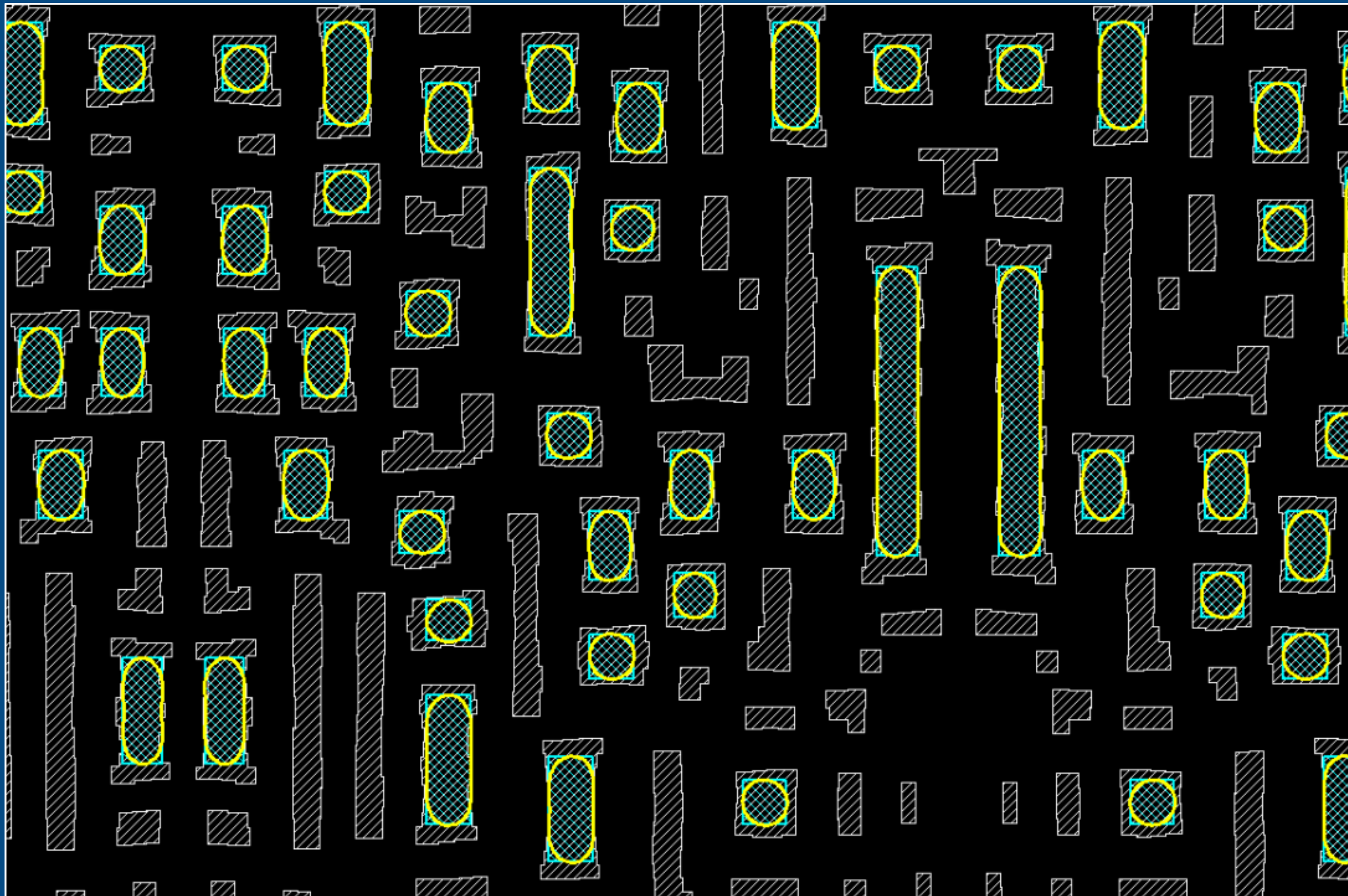
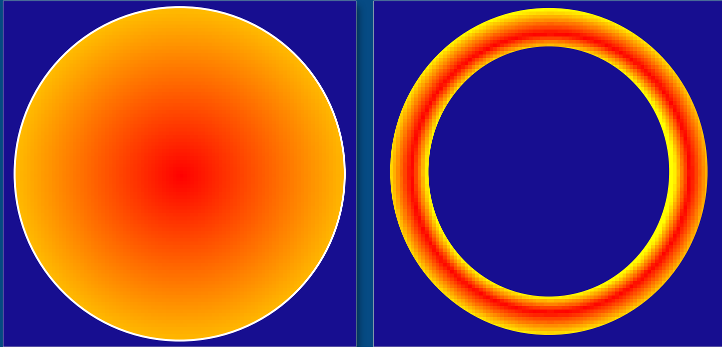
ILT is non-intuitive

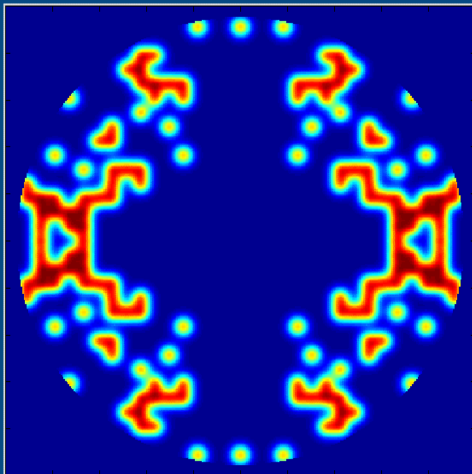


Changing shape of light source helps

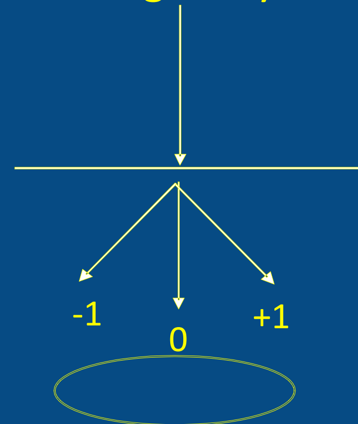
Traditional light sources

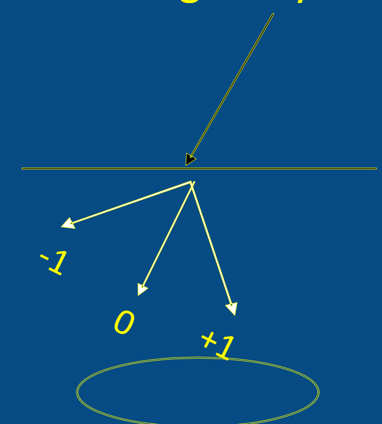


ILT source



lens must capture at least two diffracted orders





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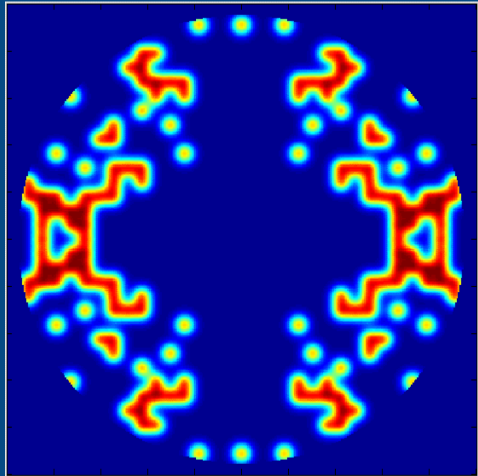
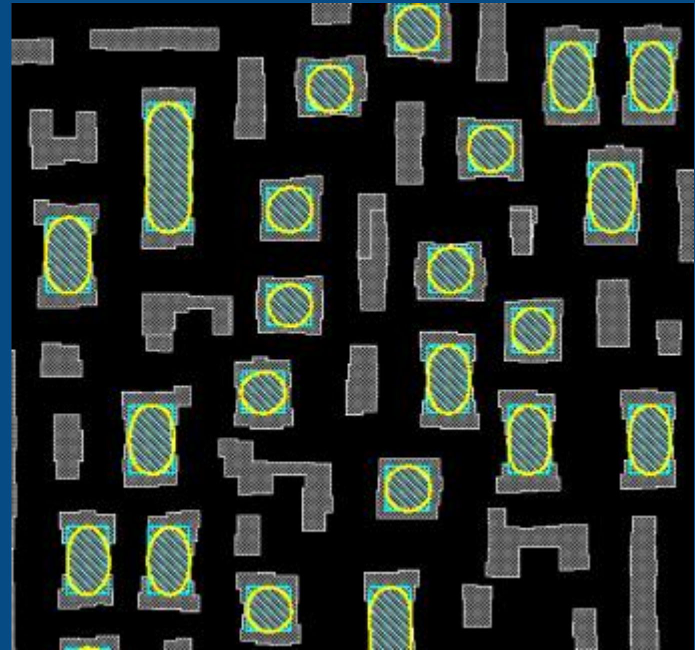
Solving the two problems simultaneously



+



ILT+SMO are used to sharpen the image of critical masks for 14nm and 10nm nodes

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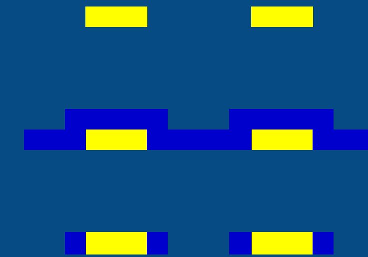
Double Patterning:
Capability.....with headaches!



Conventional

All linewidths correlated

Pitch Halving

2 linewidth types
A & B anti-correlated

Pitch Quartering

3 linewidth types
A uncorrelated
B & C anti-correlated

Problems:
Cost, Complexity, Design Impact

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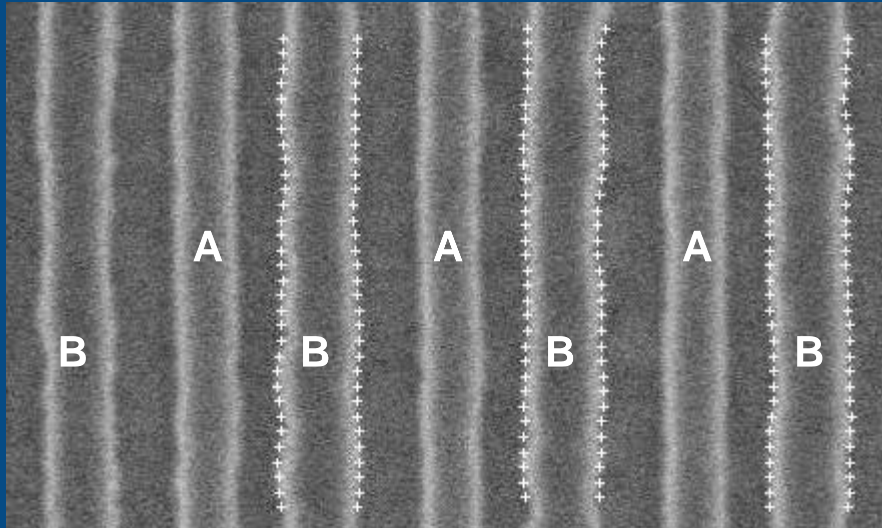
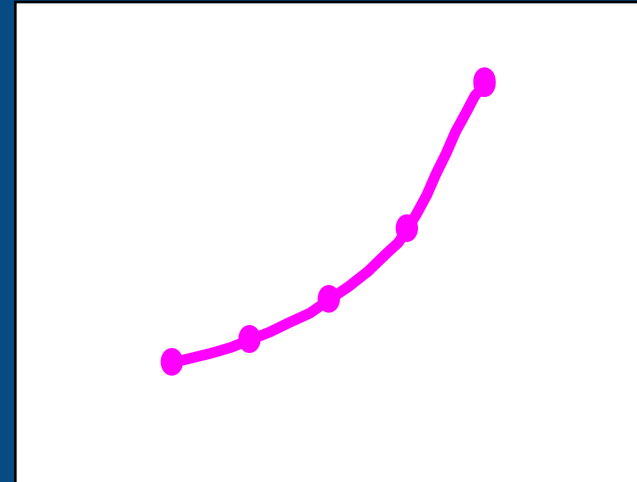
Pitch halving and gate CD matching



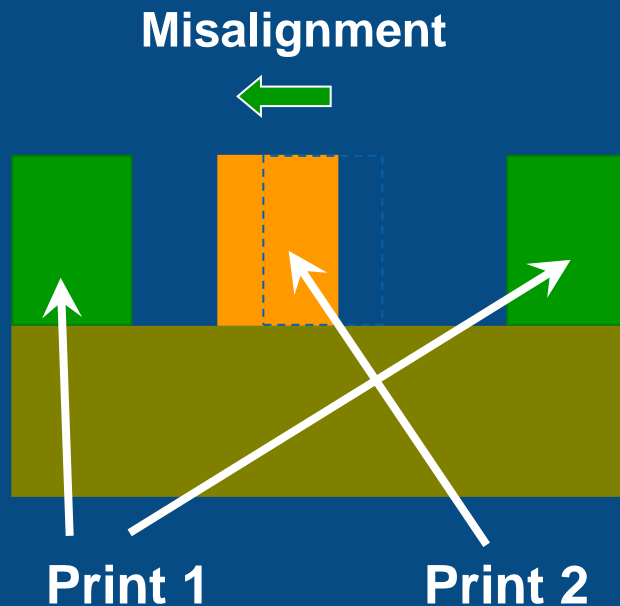


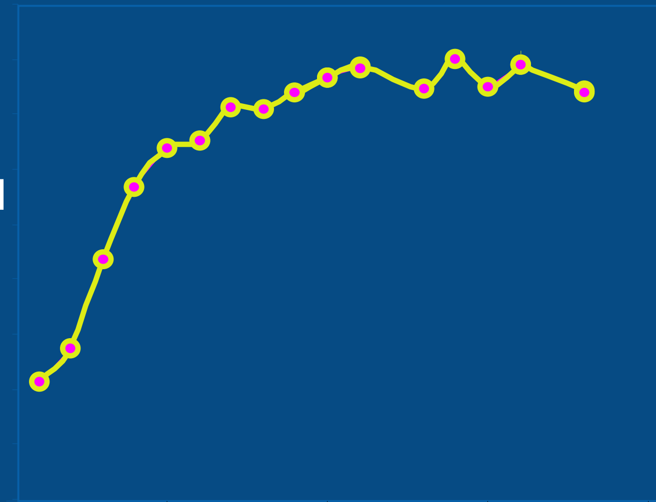
Pitch halving eliminates the close correlation which currently exists between the CDs of adjacent gates

This has implications for memory cells and other circuits which depend upon this CD matching

C. Kenyon, TOK conf., Dec. 2008

Misalignment in double-patterning



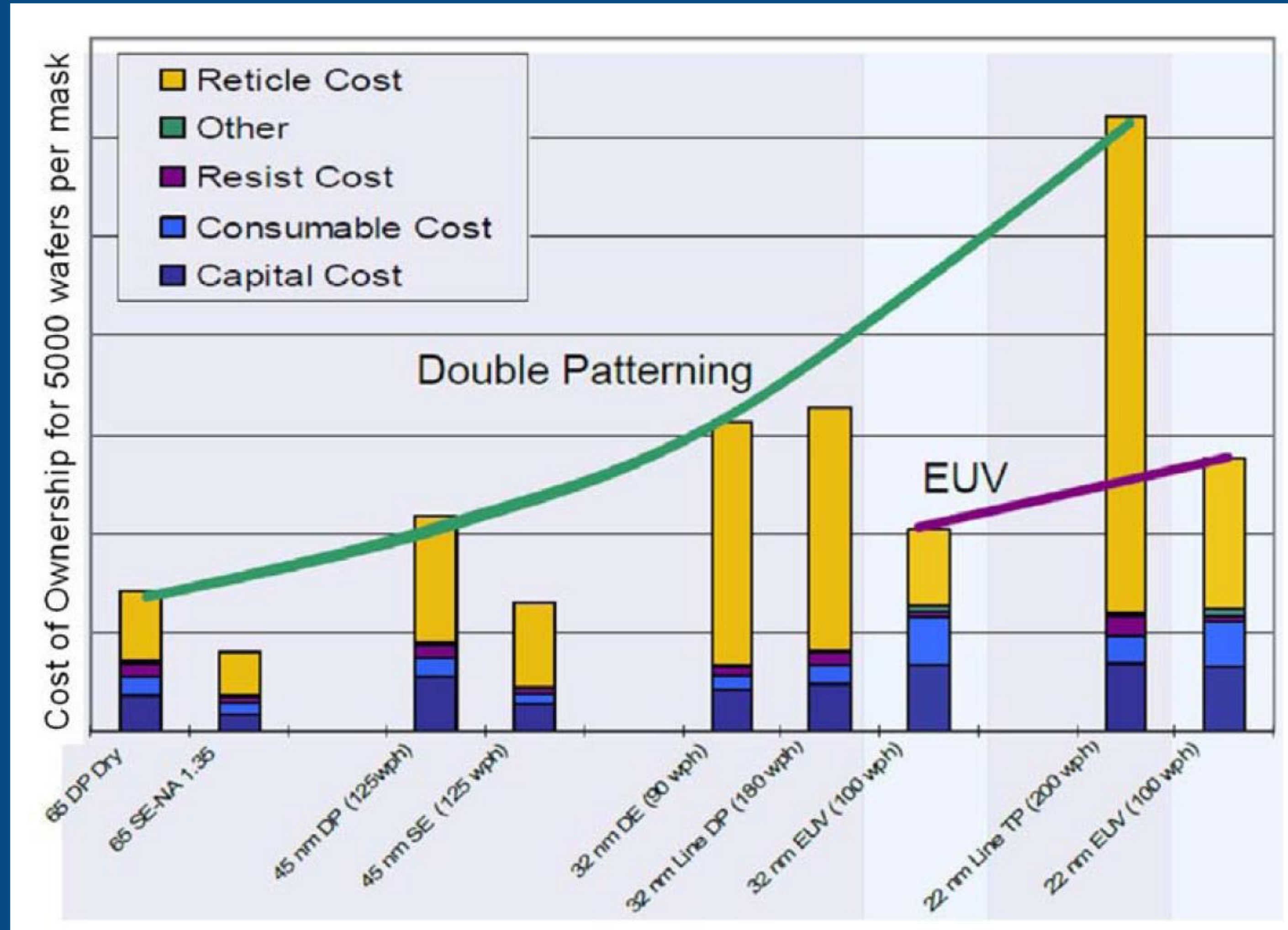


K. Kuhn, ICVC, 2009

Misalignment between the 2 exposures is a crucial liability for this technique and can limit its usability

Transistor parameters can be affected by asymmetry between the source and drain regions

EUV to the rescue!
...can help contain rising cost of DP

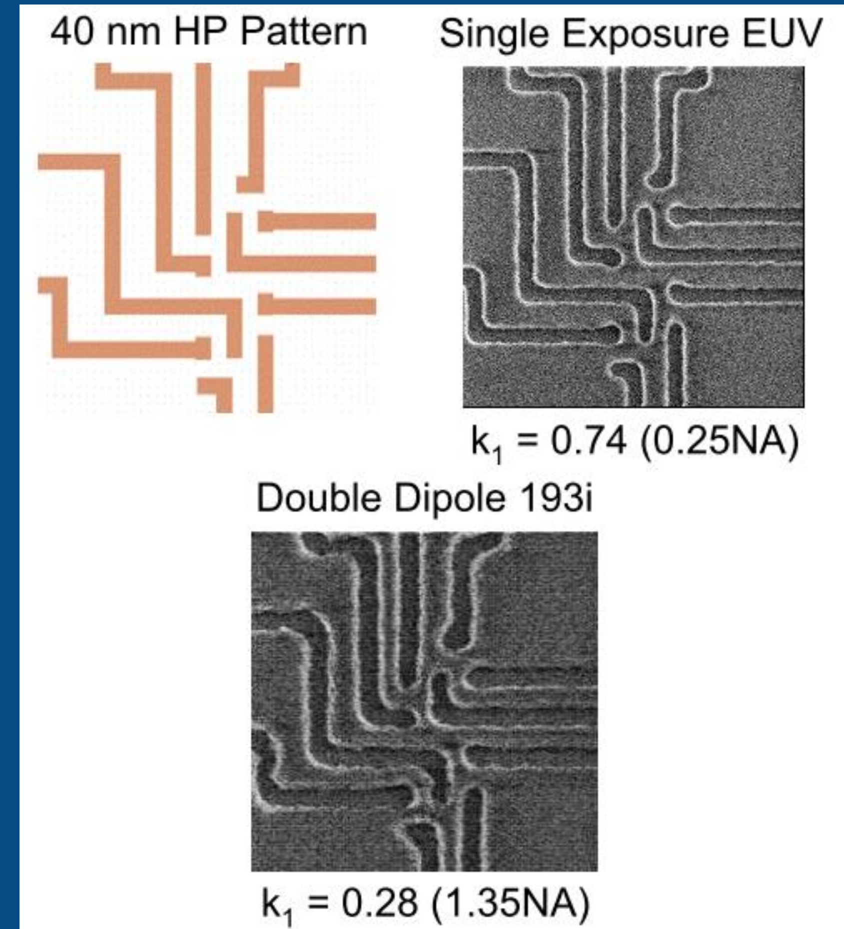


Source: ITRS 2009

Single exposure EUV, simplified DRs

Advantages of EUV

- High k_1 relative to ArF
- Single exposure simplifies process flow
- OPC is simpler
- SE provides simpler DRs



Source: Obert Wood, EUV Workshop, July 2010
S. Sivakumar, SPIE 2011

The Challenges of EUV

Resists

Patterning requirements...
- Resolution – On track
- LWR/Dose – Need high power

Outgassing - *Testing issues slow development*
- IDM TPT requirements
- Scanner outgassing requirements

Tool

Source
- Availability - Critical
- Power - Critical

Scanner Hardware
- On track

Reticle

Defectivity
- Killer defect impact >> wafer process defect impact – Need pellicle
- Mitigation strategies
  - Reticle inspection - *A-PI late, sources for A-PI, AIMS, A-BI are inadequate*
  - Patterned wafer inspection - *not a substitute for A-PI or pellicle in HVM*
  - Alternative strategies

EUV HVM implementation depends on satisfactory progress on all these fronts!

M. Phillips, SPIE, 2014

Short-term power outlook

- Need 40~80W stable MOPA+PP sources in the field linked to NXE:3300B scanners
- Not enough power for HVM, but enough to start TD and re-establish confidence in EUVL
- Seems achievable by Q1'14 given current status of program
- Need to look at remainder of EUV infrastructure and make sure it is on track for HVM introduction ~2017

M. Phillips, SPIE, 2014

The current lithography plan

Node	Intel Approach
14nm	ArF DP EUV Pilot Line
10nm	ArF Extension EUV Pilot Line

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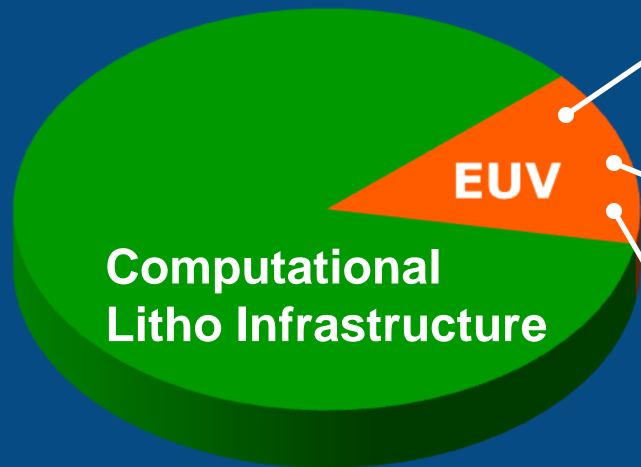
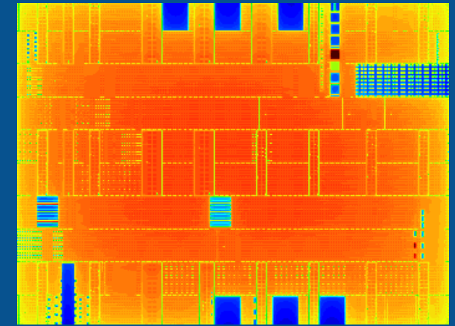
Computational Lithography Infrastructure extends to EUV

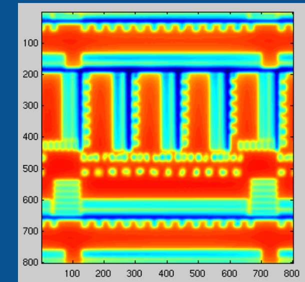


(Not to scale)

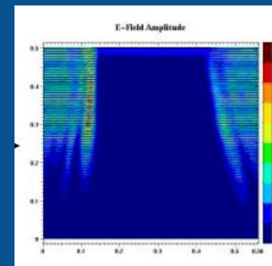
Flare

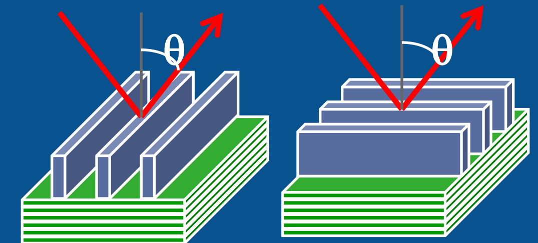


Out-of-Band (OOB) Radiation



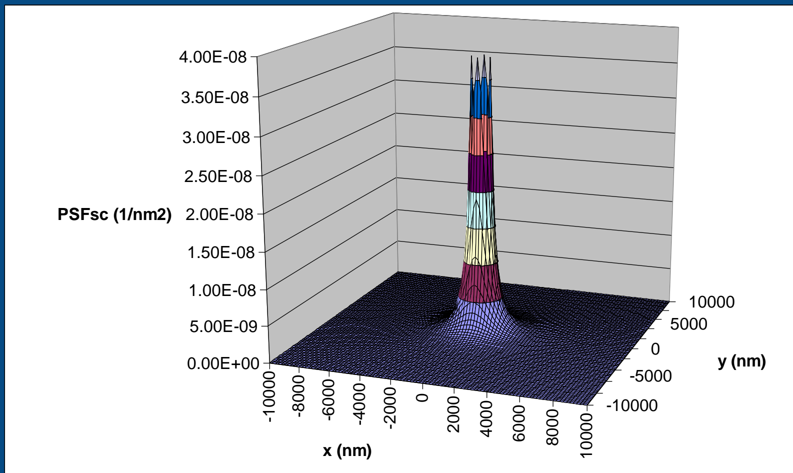
Shadowing

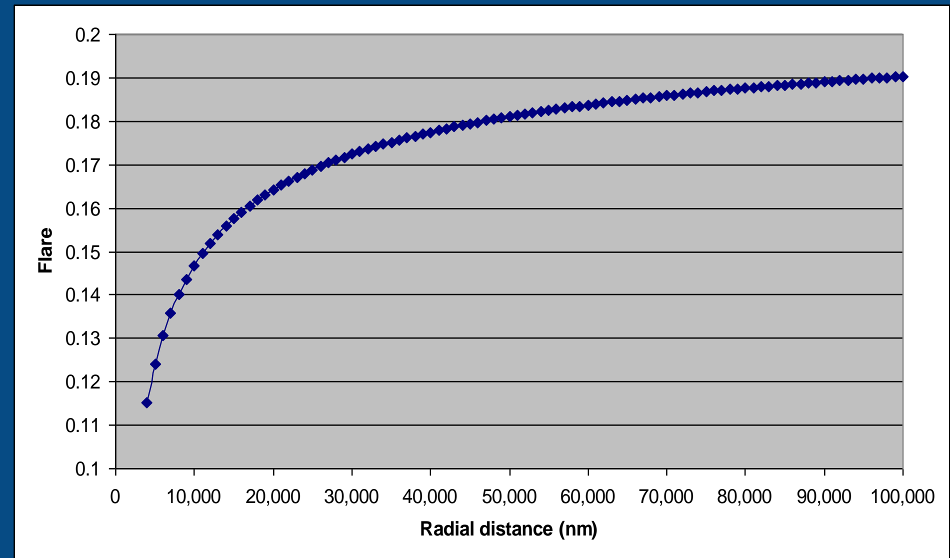




Lets start with Flare

$$PSF = \frac{0.166}{r^{2.39}} \frac{1}{nm^2} \quad \text{for } r > 600\text{nm, zero otherwise}$$

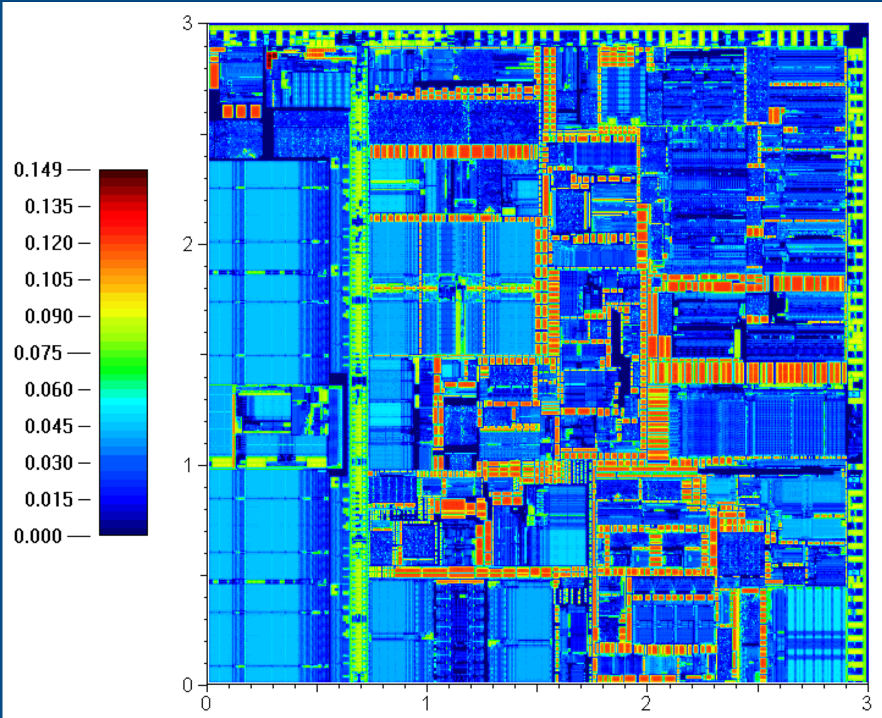




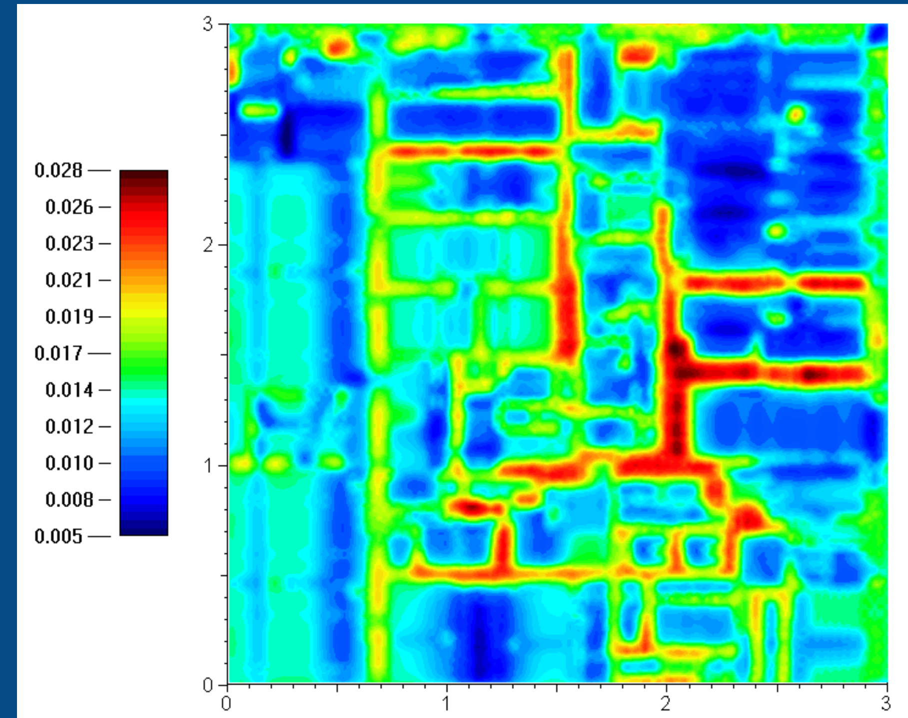
After a sharp fall, PSF decays very slowly

As a result, “far away” layout geometry affects local flare

Components of flare contributions



Short range (μm) component



Long range (mm) component

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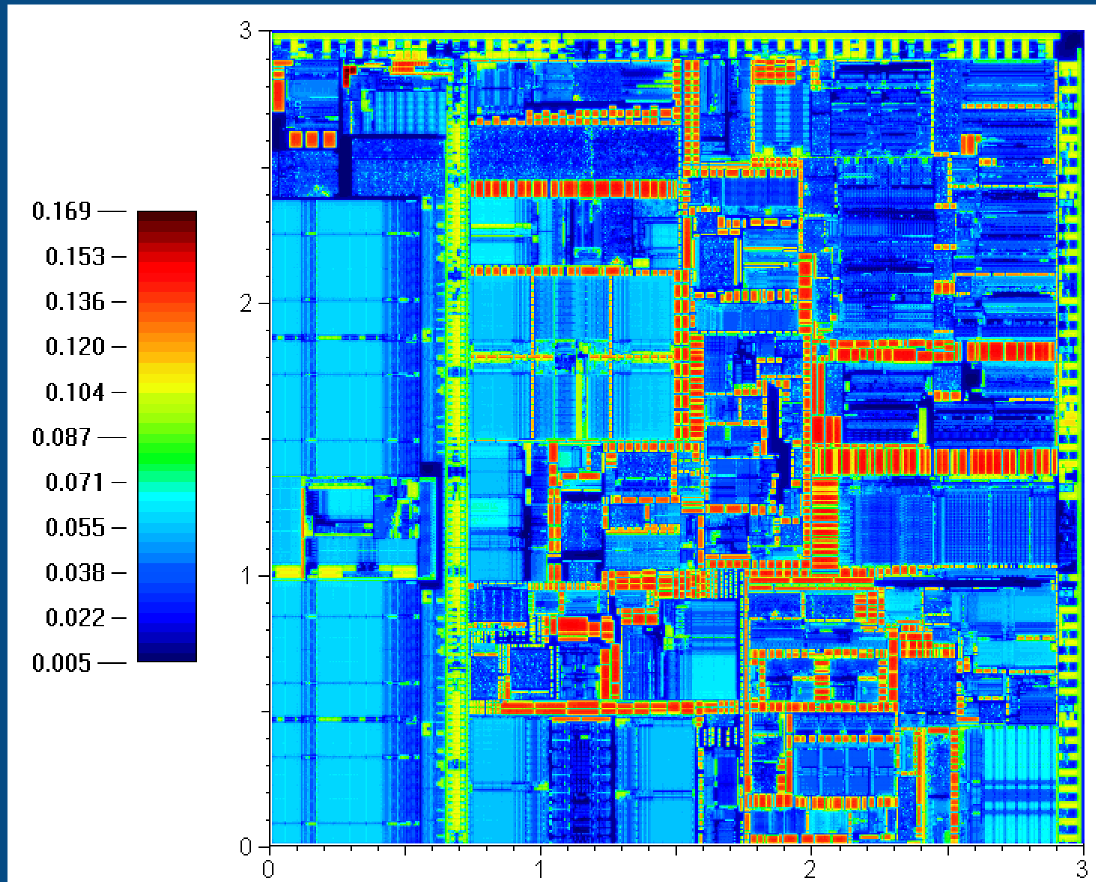
Final flare result for $3mm^2$ patch



Max = 16.9%

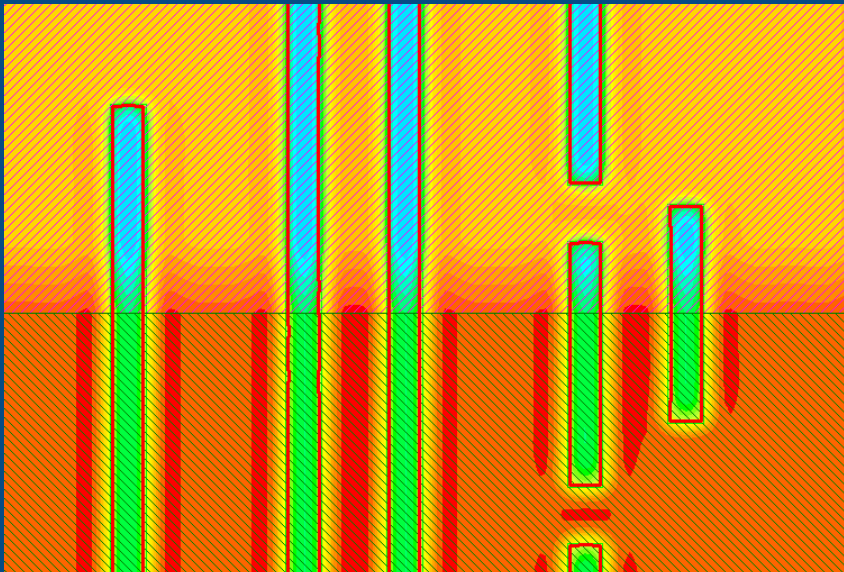
Min = 0.54%

Rng = 16.4%

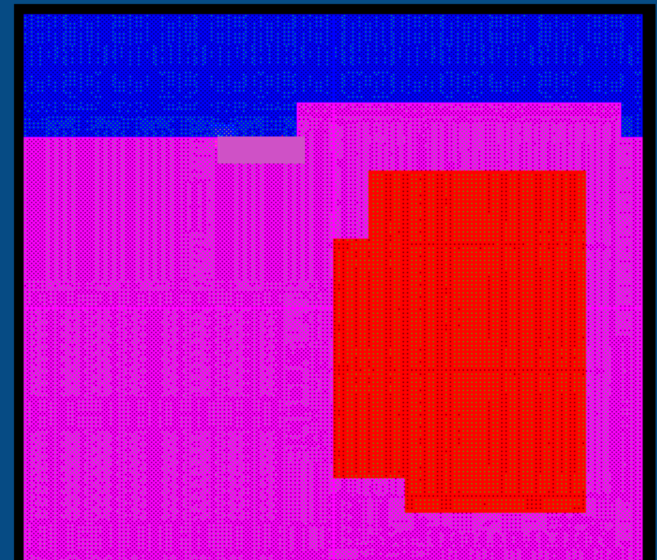
Avg = 5.62%

Full Chip Flare Compensation

(work is in handling boundaries)



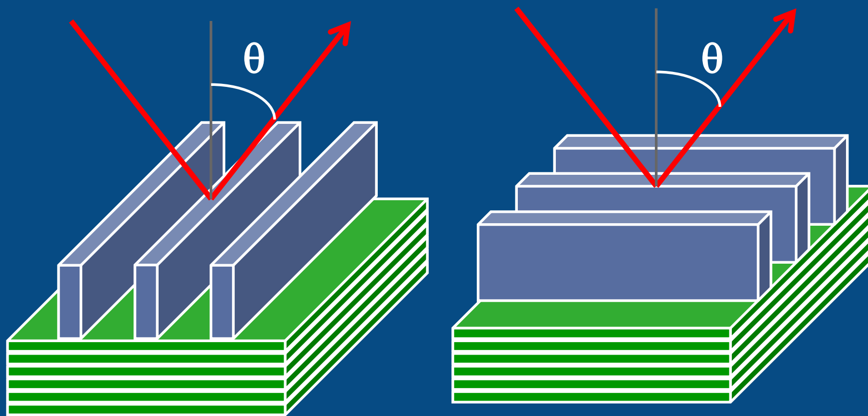
Effect of flare on Image intensity



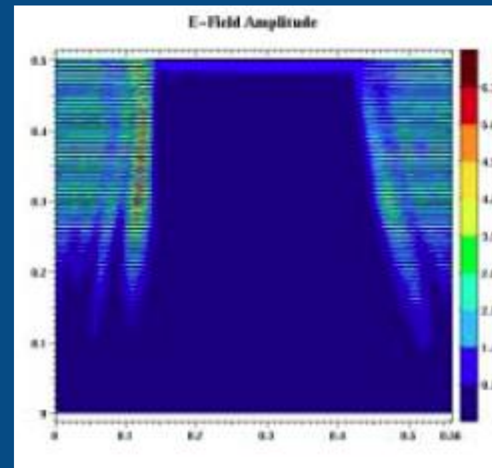
Domain with Flare Data

Modeling of Mask Shadowing

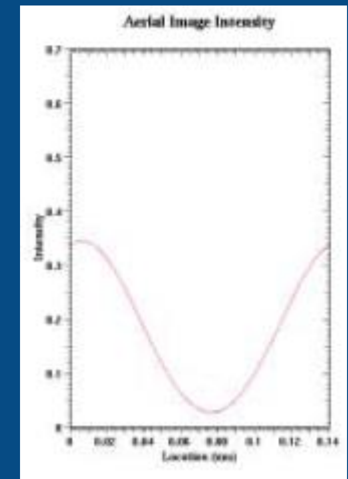
1. Create Mask Geometry



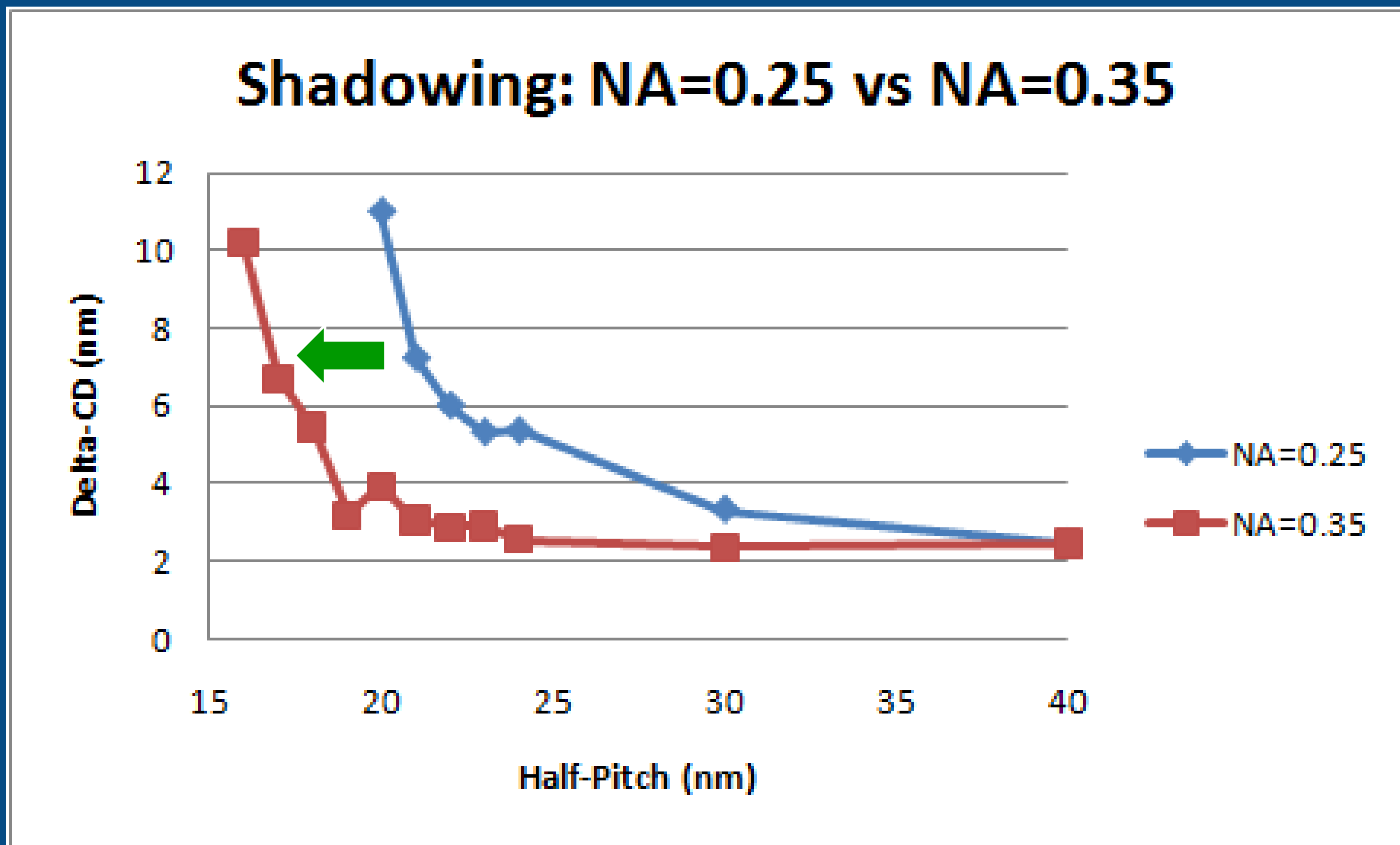
2. Calculate E-fields



3. Calculate Wafer Image



H-V Delta for 0.25NA vs 0.35NA



OOB: Out-of-band radiation
Problem: Resist is more sensitive to OOB

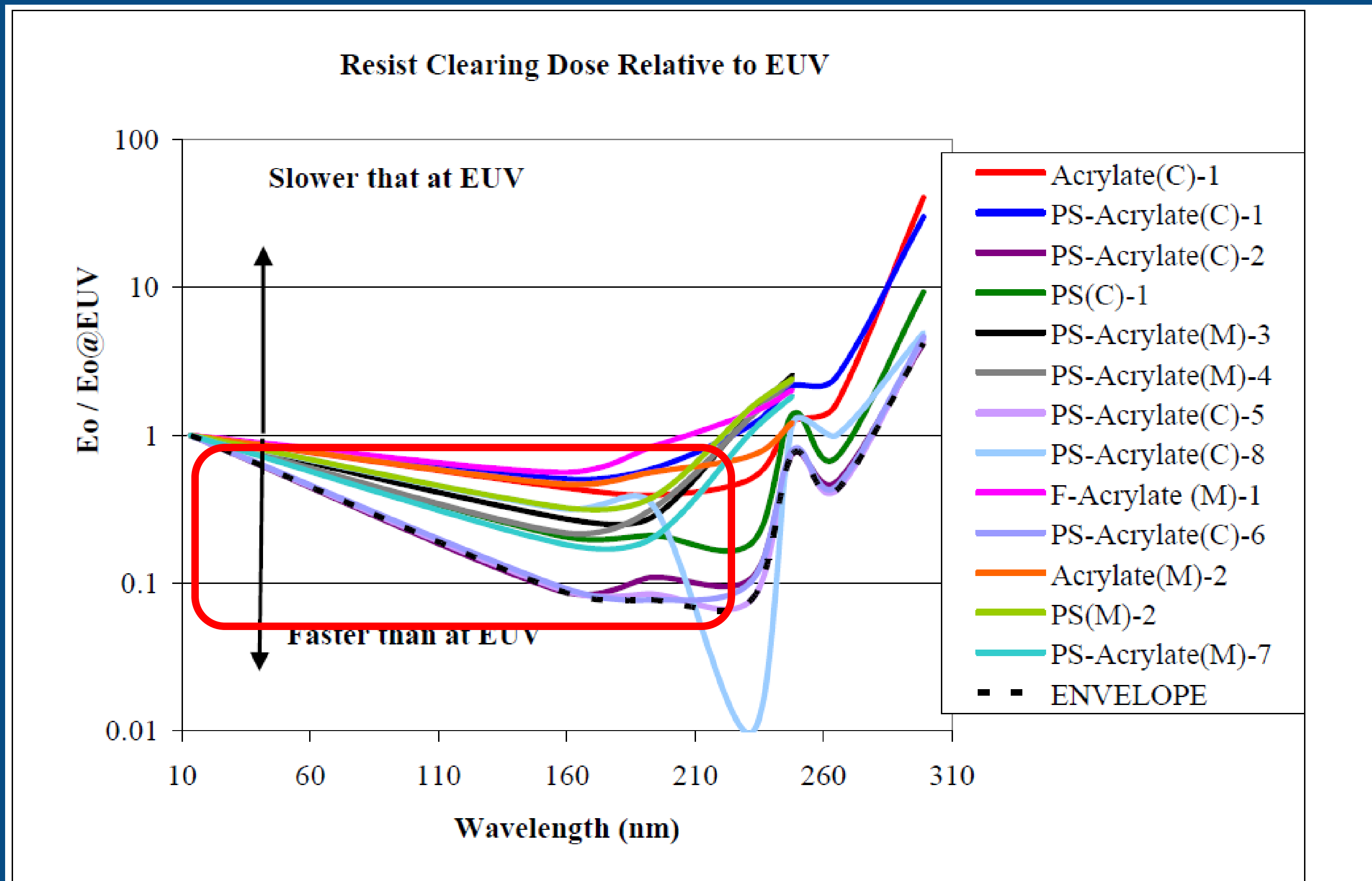


Figure 2 – The clearing dose (E_o) of each resist relative to that at EUV for exposure wavelengths from 13.5 to 299 nm. In the legend, (C) denotes resists provided by commercial suppliers and (M) denotes the model resists formulated at MIT-LL. The envelope encompassing the worst-case data points is shown as the dashed line.

Source: J. Roberts, R.Bristol. T. Younkin, T. Fedynyshyn, D. Astolfi, A.Cabral Proc. SPIE 7272 (2009)

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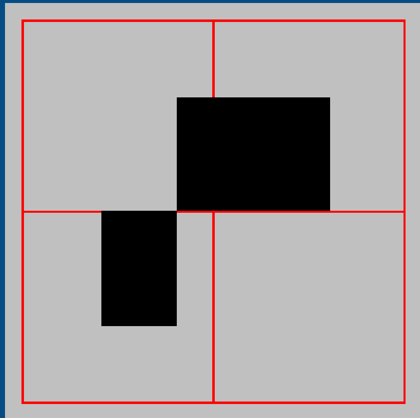
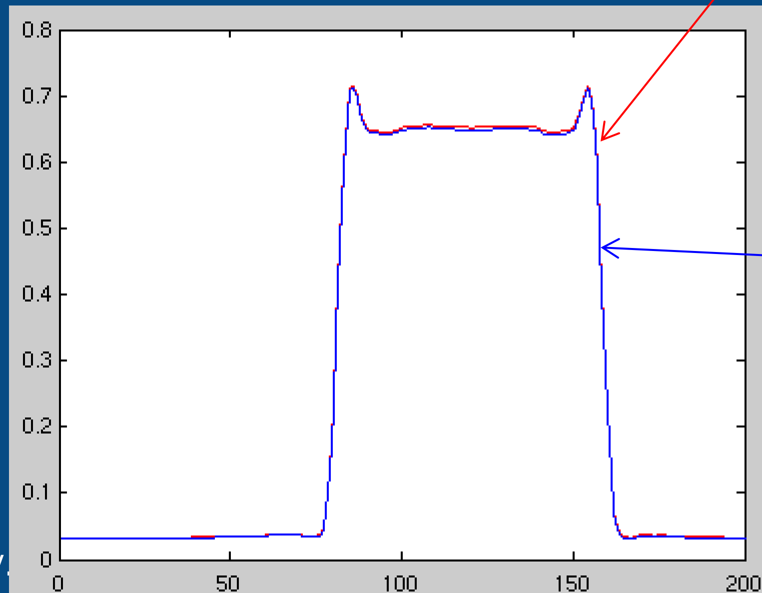
EUV image comparison with OOB (rigorous simulation is too slow)

- Resulting EUV+OOB images match within ± 0.003 (assuming 4% total flare from OOB).





EUV+OOB (fast)

EUV+OOB (rigorous)

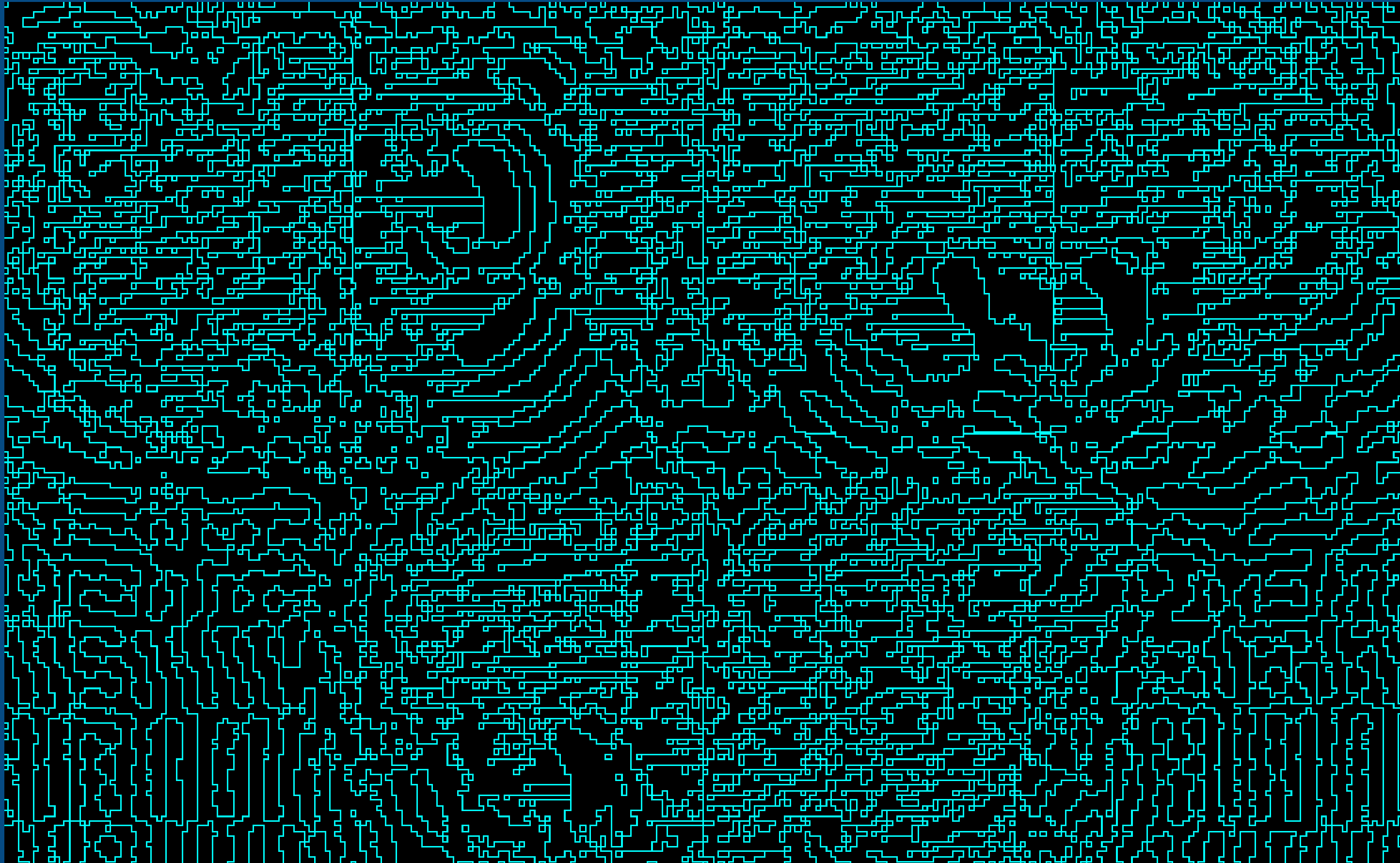
Computational Litho for EUV is not a problem

“If you build it, they will come”

Summary

- What the world wants (hint: 3D transistors)
  - Demand and Economics drive Moore's Law
- Lithography: Choices for 14 nm and 10 nm
  - Double Patterning is the workhorse, with caveats
- Computational techniques for EUV
  - Computational Litho for EUV is not a problem

How will this mask print?



The image from 193 pixelation

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…if you used EUV, however…

Acknowledgments

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