2014 International Workshop on EUV Lithography

Panel Discussion: Introduction (P10)

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Agenda: Panel Introduction

- Review of panel discussion from June 2013
- Major Developments since June 2013
- Questions for Panelists for 2014 Panel
- Introduction to the Panel

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Questions for Panelists (2013 EUVL Workshop Panel Discussion)

- What are the HVM Litho roadmaps for next 10 years?
- At what node do you expect EUVL to be competitive with 193 nm lithography and for what throughput? Will this comparison be for 300 mm and 450 mm wafers?
- What are the EUV source requirements as a function of NA, Resolution, throughput metric for 300mm and 450mm?
- Panelists opinion about multi-patterning EUV vs. BEUV (6.x nm) for future nodes

Response from Panelists (2013 EUVL Workshop Panel Discussion)

- Sam Sivakumar (P72), *Intel Corporation*

- **EUV currently targeted as primary option for 7nm node (2015 development, 2017 HVM)**

- Main questions to ask is if the key technical challenges going to be solved in time to deliver a COO less than ArF MP in this time frame

Response from Panelists (2013 EUVL Workshop Panel Discussion)

- Sushil Padiyar (P74), *Applied Materials*

- **12 to 8 nm HP Patterning Paths with EUVL for 2017-2020 (Options and Challenges)**
  - 13.5 nm DP, 13.5 nm with Hyper NA or 6.x nm, 193i MP

- **Best Guess for 7 to 5 nm (Options and Challenges)**
  - 13.5 nm EUV / SADP
  - 193i Multi patterning +EUV

Response from Panelists (2013 EUVL Workshop Panel Discussion)

- Tatsuhiko Higashiki (P71), *TOSHIBA*

- All kind of memory will be shrinking
- **Semiconductor business will mature, if lithography & mask cost reduction is not performed**
- **For 450 mm, Investment improvement is 7%**
- **9 inch Mask is preferred to shrinking exposure field in memory device**
- **EUVL+DSA DSA may become one big choice in the future.**

Response from Panelists (2013 EUVL Workshop Panel Discussion)

- Pawitter Mangat (P73), *GlobalFoundries*

- Semiconductor Industry cannot afford any more delay for EUV Industrialization. **Need EUVL ready in the next 2 years (by 2015)**
- Maximizing Lithographic performance from current 0.33NA systems is critical for HVM for multi-node solutions
  - EUV mask optimization (thinner absorber) will enable EUV extensibility
- **High NA decision for future needs to be agreed upon by industry soon due to long lead time for development**

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Major Developments Since June 2013

- 450 mm transition has been pushed out
- BEUV (6.x nm) is not on the roadmaps
- Six EUVL Scanner (NXE3300 B) have been shipped with Cymer's source and some chip makers are using them for 10 nm HP node product development
- Impact of High NA options on mask and throughput is being discussed (0.5 NA 4 x is a significant challenge) and no decision yet
- Development of high sensitivity resists (~ 2mJ) that may help in meeting throughput goals
- ~40 W – 62 W source power levels reported at supplier sites for stand alone sources

Questions for Panelists (2014)

- **Can EUV deliver patterning solutions for 7nm node? Also, please list your opinion on topics listed below:**
- A: What is the latest status for source power, available for NXE 3300B? What is your opinion on source power requirements for 7 and 5 nm nodes?
- B: Will EUV Double patterning be required at 7 nm? What will be required at 5nm node? Do you expect any OPC related issues?

Questions for Panelists (2014)

- C: Mask: What will be the new material requirements and mask size requirements to accommodate higher NA patterning? Do you expect mask etch complexity with new materials? How ready are masks to support 7 nm manufacturing? What is the status of mask defect inspection and repair tools?
- D. Pellicle: Is a no-pellicle approach a show-stopper for HVM insertion of EUVL? What additional restrictions do you expect on inspection due to pellicle?
- E. What are different device types and lithography needed at various nodes, e.g., 3D NAND, III-V Logic, Post FINFET Era etc.

Panelists – 2014 EUVL Workshop

- Hakaru Mizoguchi, *Gigaphoton* (P12)
- Takayuki Uchiyama, *Toshiba* (P13)
- Sushil Padiyar, *AMAT* (P14)
- Nigel Farrar, Cymer /ASML (P15)

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