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Leading Innovation

2014 International Workshop on EUV Lithography

Panel discussion

Topic: Can EUVL deliver patterning solutions for 7nm node?

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Panel discussion

A: What is the latest status for source power, available for NXE 3300B?

20 - 40W@IF

What is your opinion on source power requirements for 7 and 5 nm nodes?

1kW@IF will be required for high NA.

B: Will EUV Double patterning be required at 7 nm?

It depends on resist performance, design restriction and real half pitch size.

Limit of 193nm & 1.35 NA SE	13.5nm/SE	0.33NA	0.45NA	0.50NA	0.60NA
Min. k1 of 2D=0.31 (hp=45nm)→	Min hp of 2D	12.7 nm	9.3 nm	8.4 nm	7.0 nm
Min. k1 of 1D=0.26 (ho=38nm)→	Min hp of 1D	10.6 nm	7.8 nm	7.0 nm	5.9 nm

What will be required at 5nm node? Do you expect any OPC related issues?

High NA EUV (> 0.5) with high power source.

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Panel discussion

C: Mask: What will be the new material requirements and mask size requirements to accommodate higher NA patterning? Do you expect mask etch complexity with new materials? How ready are masks to support 7 nm manufacturing? What is the status of mask defect inspection and repair tools?

An etched ML mask will be one of the solution for high NA EUVL tradeoff.

Challenges:

- **Pattern collapse**
- **Cleaning**
- **Repair**
- **Durability**

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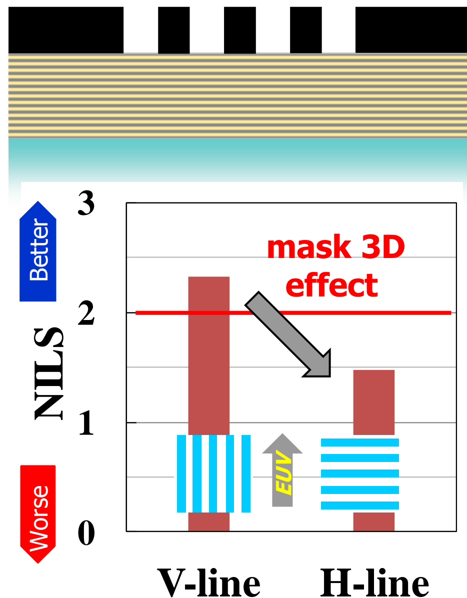
Etched ML pattern for high NA EUVL

In order to overcome the tradeoff of high NA EUVL, mask structure is optimized.

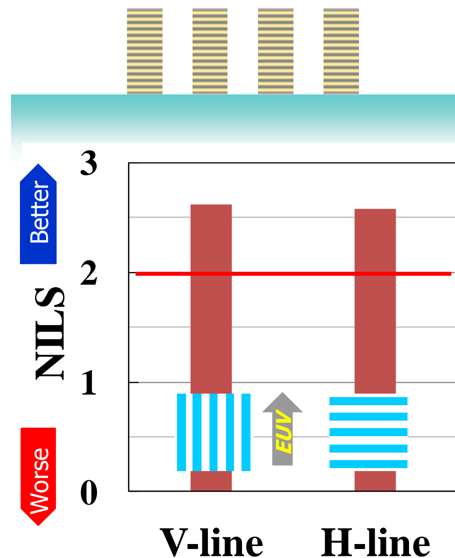
After HM/Ta removal

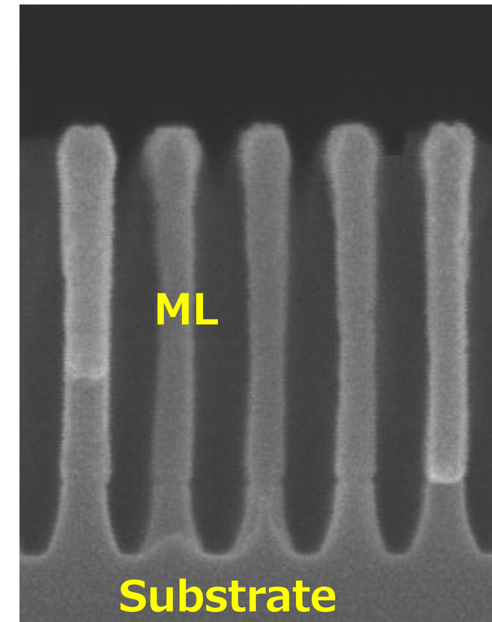
Ta based absorber



lower mask 3D effect

Etched Multilayer





Etched multilayer L/S pattern of 40 nm hp on mask (**10 nm hp on wafer** using 4X optics) is achieved.

Takashi Kamo, et al, 2013 International Symposium on Extreme Ultraviolet Lithography

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Panel discussion

D. Pellicle: Is a no-pellicle approach a show-stopper for HVM insertion of EUVL?

More and more effort at scanner cleanness is needed for no-pellicle approach, especially for logic.

What additional restrictions do you expect on inspection due to pellicle?

Particle and haze inspection tool will be needed for EUV mask with pellicle.

Actinic pattern inspection may be expensive···. Alternative inspection is a future challenge.

E. What are different device types and lithography needed at various nodes, e.g., 3D NAND, III-V Logic, Post FINFET Era etc.

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Lithography candidates for each device generation

(Table ORTC & Table PIDS7b of ITRS 2013)

	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
Logic node	16/ 14		10		7		5		3.5		2.5		1.8		1.3
Logic Metal hp	40	32	32	28	25	23	20	18	16	14.2	12.6	11.3	10.0	8.9	8.0
Logic Fin hp	30	24	24	21	19	17	15	13	12	10.6	9.5	8.4	7.5	6.7	6.0
NAND Flash 2D															
NAND Flash 3D															
DRAM															
PCRAM															7
ReRAM															4

LELE

EUV LELELELE・・・

High NA EUV / DSA

SADP/QP

Multiple patterning or Low power EUV ➔ High NA EUV/DSA+EUV

We choose the lithography from the point of view of cost.

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