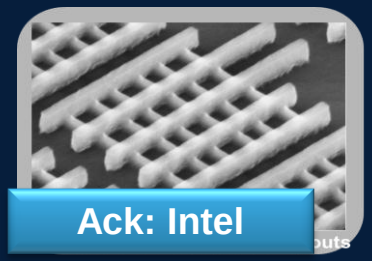
Patterning Paths @ 7nm

	Roadmap Outlook							
	2009	2011	2013	2015	2017	2019		
Node (nm)	32	22	14	10	7	5		
Approx. HP (nm)	50	40	20	18	12	8		
K1@0.33NA	1.18	0.78	0.5	0.4	0.3 (SE)	0.2		
K1@0.4NA	1.42	0.95	0.6	0.48	0.35	0.24		



193i/Dry Single Exposures/
Multi-Patterning
Gridded/Restricted Design Rules

"EUV + 193i" Multi-Patterning

DSA, E-beam, Higher NA EUV?

Multi-Patterning Techniques

Single Patterning | 193i Immersion + DP | EUV, EUV DP+193i MP

LELE, LFLE, SADP, SAQP | SAxP, Cuts, Hole Shrinks

Building Blocks

Spin-On/Deposited ARC's, HM's.
C-APF, Hard-Masks: a-Si, Sio2/SioN

Line Spacers/Hole Shrink Spacers

Total ETCH CDU: <5% 6S, Dry Cleans
Atomic Layer Etch (side-wall)

1. What is the latest status for source power available for NXE 3300B? Source power requirements for the 7nm and 5nm nodes?

1A. 55-80W per SPIE 2014 with stable operation planned by 2014 end. Sub10nm HVM likely will require > 120W for select applications and >250W for full-fledged adoption.

2. Will EUV double patterning be required at 7nm? What will be required at 5 nm?

2A. K1@0.33NA approaching single exposure limits at 7nm HP needs. K1<0.28 likely require double patterning. Higher NA options or layout trade-offs might be required to allow single exposures at 7/5nm.

3. Mask: What will be the new material requirements and mask size requirements to accommodate higher NA patterning? Do you expect mask etch complexity with new materials? How ready are masks to support 7nm manufacturing? What is the status of mask defect inspection and repair tools?

3A. AMAT Tetra EUV Etch and AMAT Reticlean Programs Scalable Across New Materials and Challenging Performance Specs Demonstrated.

4. Pellicle: Is a no-pellicle approach a show-stopper for HVM insertion of EUVL?

4A. Pellicle-based approach will certainly minimize defects and metrology/cleans frequency, assuming manageable thermal load @ 80-250W EUV power.