2014 International Workshop on
EUV Lithography

Current status and expectation of EUV lithography

June 26, 2014

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TOSHIBA Corporation

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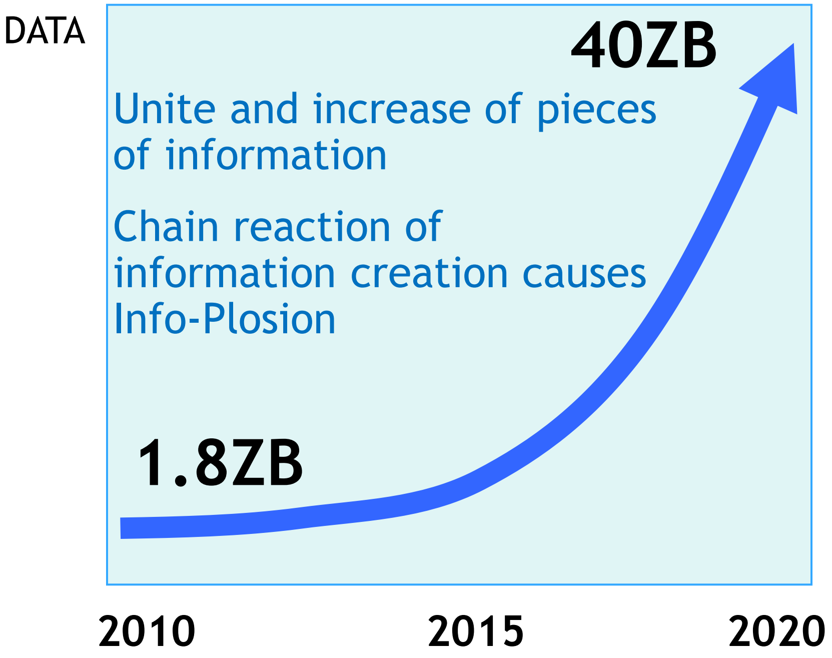
Introduction

Information-Explosion and Cloud Service & M2M

Scattering data to Cloud
New knowledge makes new values

Diversity of uses makes new data

Info-Plosion

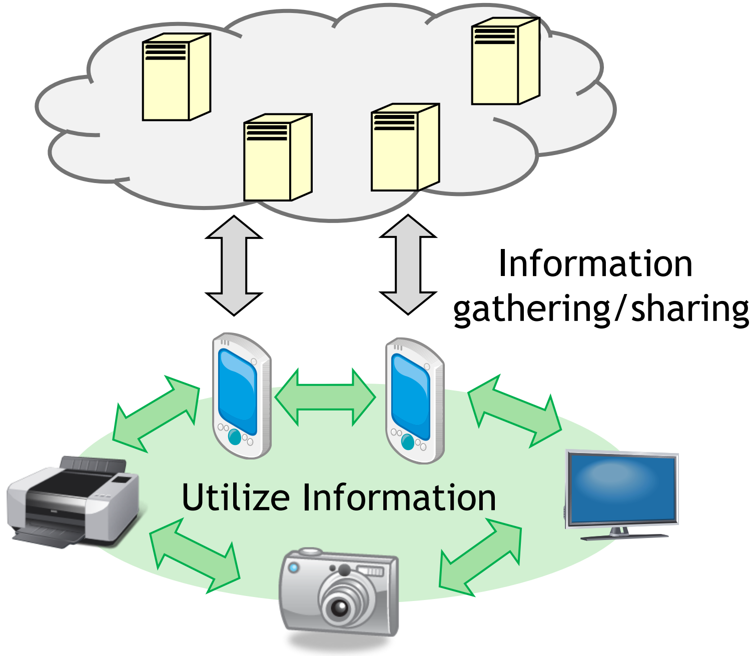


Unite and increase of pieces of information

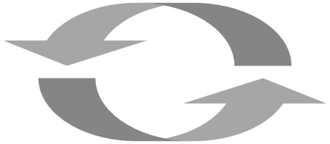
Chain reaction of information creation causes Info-Plosion

Source : IDC Digital Universe Study, May2010

Cloud service



M2M



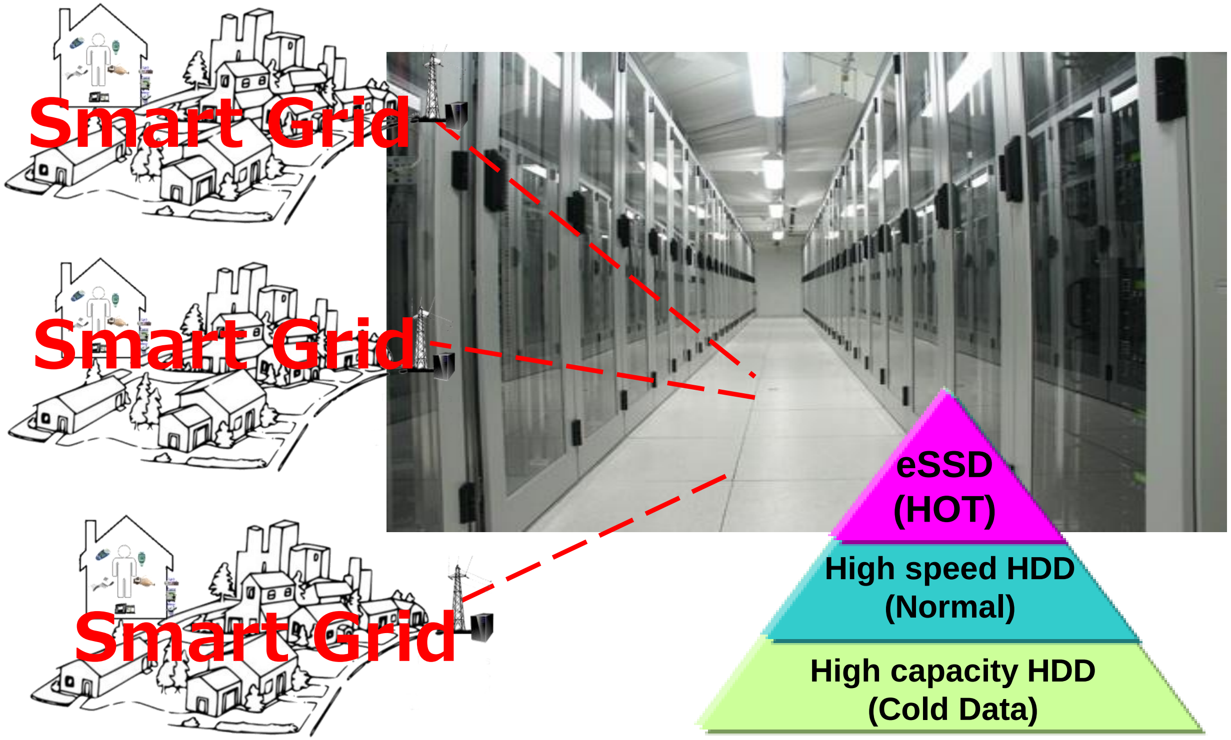
Cloud makes Big data

Sharing Data in Cloud service and utilizing with M2M

Nobuo Hayasaka, EIDEC Symposium 2014.

Toshiba Unified Storage Strategy

Total Storage Solution by Toshiba



In the Cloud Data Center

Is the Infrastructure (**IaaS**)

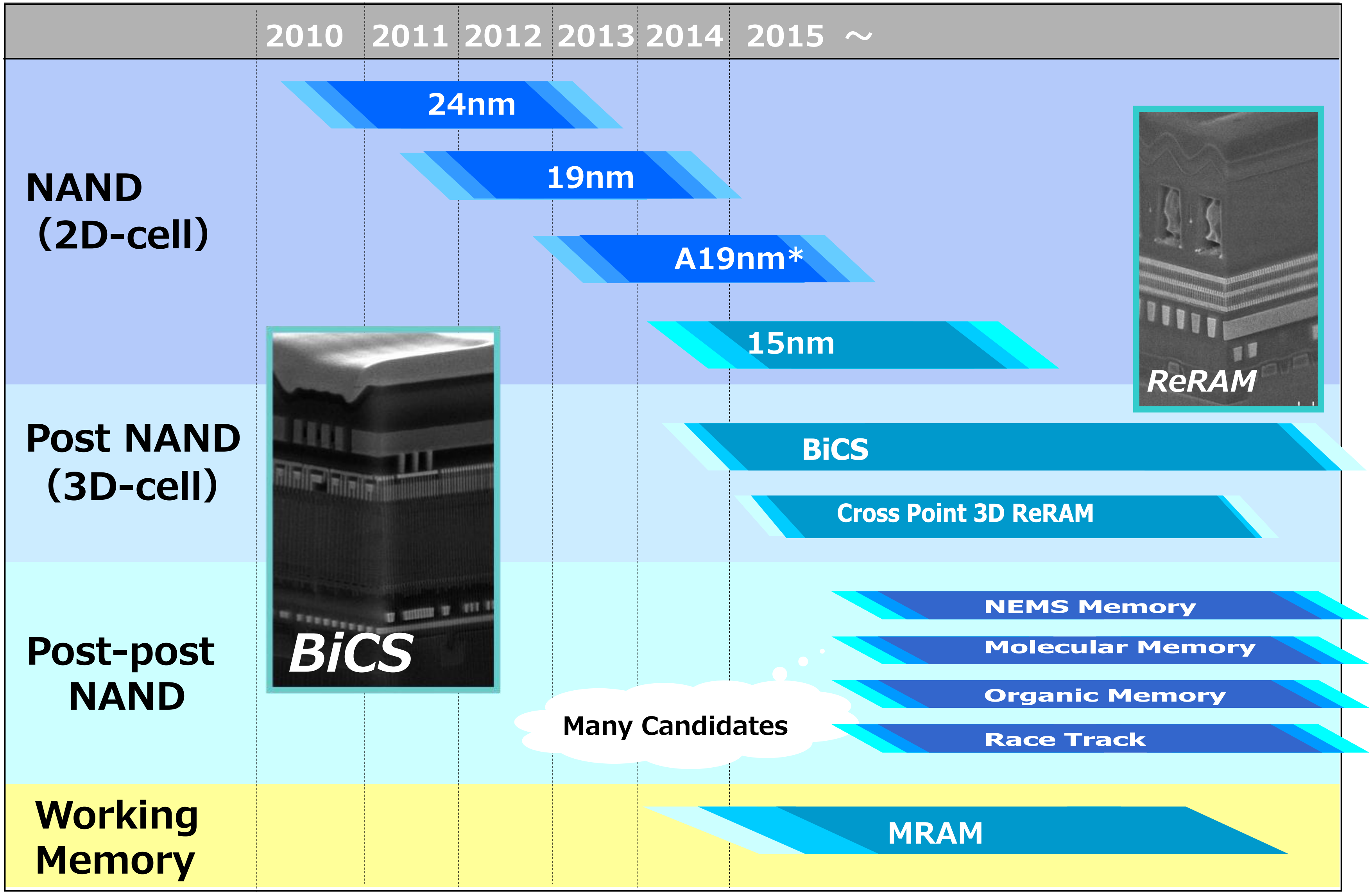
This Includes

- **High Performance Computing (HPC)**
- **Normal Computing**
- **Storage**
  - **HOT (SSD/PCIe)**
  - **Normal (HDD)**
  - **Quick Frozen (TLC)**
  - **Cold Storage (HDD)**

HDD **SSD** **NAND Flash**

Nobuo Hayasaka, EIDEC Symposium 2014.

Roadmap for future memory



2010 2011 2012 2013 2014 2015 ～

NAND (2D-cell)

24nm

19nm

A19nm*

15nm

ReRAM

Post NAND (3D-cell)

BiCS

Cross Point 3D ReRAM

Post-post NAND

BiCS

Many Candidates

NEMS Memory

Molecular Memory

Organic Memory

Race Track

Working Memory

MRAM

* A19nm : 19nm 2nd Generation

Nobuo Hayasaka, EIDEC Symposium 2014.

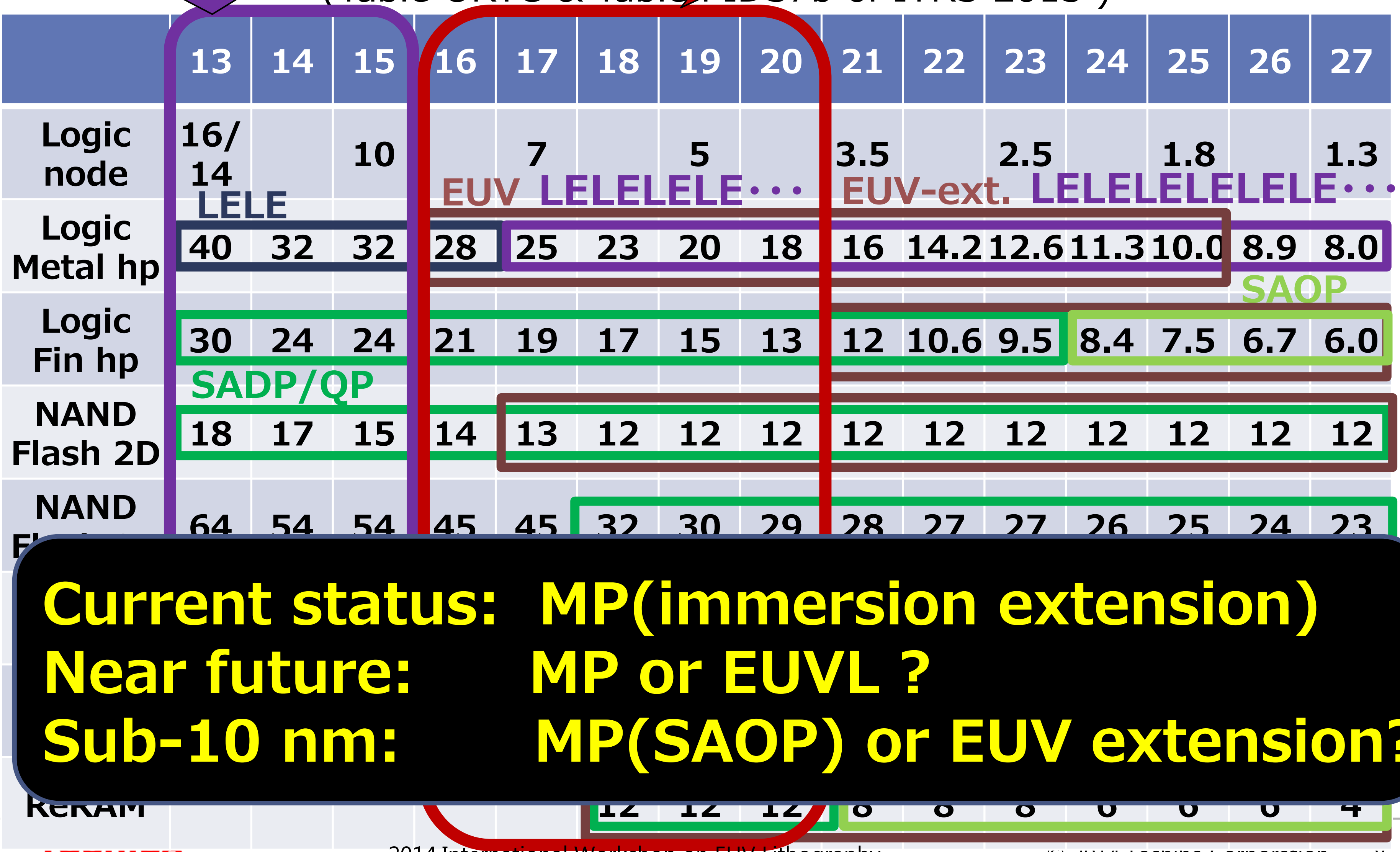
Lithography Challenges for Memory

Pattern shrink roadmap based on ITRS 2013

MP (multiple patterning)

EUVL ?

(Table ORTC & Table PIDS7b of ITRS 2013)



	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
Logic node	16/ 14		10		7		5		3.5		2.5		1.8		1.3
Logic Metal hp	40	32	32	28	25	23	20	18	16	14.2	12.6	11.3	10.0	8.9	8.0
Logic Fin hp	30	24	24	21	19	17	15	13	12	10.6	9.5	8.4	7.5	6.7	6.0
NAND Flash 2D	18	17	15	14	13	12	12	12	12	12	12	12	12	12	12
NAND Fl	64	54	54	45	45	32	30	29	28	27	27	26	25	24	23
ReRAM						12	12	12	8	8	8	6	6	6	4

Current status: MP(immersion extension)
Near future: MP or EUVL ?
Sub-10 nm: MP(SAOP) or EUV extension?

Lithography for sub-10nm

- Extension of immersion lithography
  - 1D layout by SAxP + cut mask
    - L&S by SADP(19 nm)➔SAQP(10 nm)➔SAOP(sub-10 nm)
    - Cut mask by LE^8~ or NGL

Issues **Restrict design**
Complex process control
Long process steps
➔ **High cost**

- NGL
  - 2D layout by single exposure
    - High NA EUVL

Field size, Source, Optics, Resist

  - Bottom-up patterning
    - DSAL + EUVL

Overlay, Defectivity

We need NGL for sub 10nm with low cost!

The potential of EUVL is attractive.

$$\text{Resolution} = k1\frac{\lambda}{NA}$$

λ : exposure wavelength
NA : Numerical Aperture
k1 : process constant[>0.25]

NA	0.40	0.35	0.30	0.25	k1
0.25	21.6	18.9	16.2	13.5	
0.30	18.0	15.8	13.5	11.3	
0.33	16.4	**14.3**	12.3	10.2	
0.35	15.4	13.5	11.6	9.6	
0.40	13.5	11.8	10.1	8.4	
0.45	12.0	10.5	9.0	7.5	
0.50	10.8	9.5	8.1	6.8	
0.55	9.8	8.6	7.4	6.1	
0.60	9.0	7.9	6.8	5.6	
			6.2	5.2	
0.70	7.7	6.8	5.8	4.8	

NA ≥ 0.6 will be desirable.

Concerns for high NA EUVL

High NA EUV tradeoff

- Resolution(high NA) / full field (throughput)/ 6 inch mask

High power source

- Power loss by increasing in PO mirror number (6 → 8?)
- Low sensitivity resist

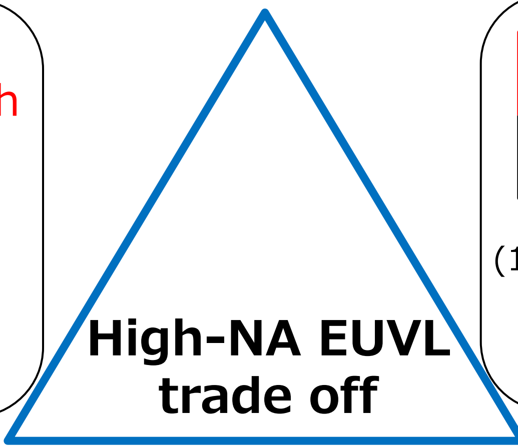
Optics for high NA and high power

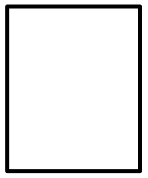
- Increase in NA (> 0.5)→ Tighter mirror roughness and aberration specification for larger mirror
- Damage due to high power EUV light
  - ML mirror, mask and Pellicle durability

Resist for high NA

- RLS tradeoff: Resolution / LER / Sensitivity ~shot noise issue

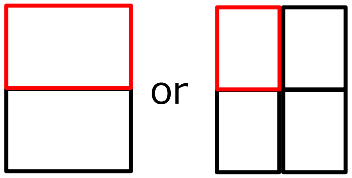
High-NA EUVL tradeoff





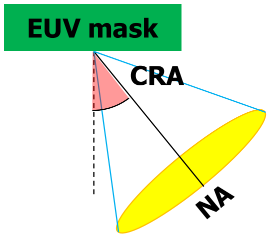
X Mag. = 9/12inch Mask
(6 or 8)

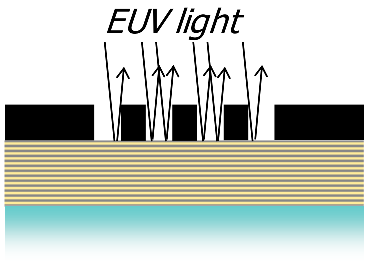
- **Infrastructure for large mask**

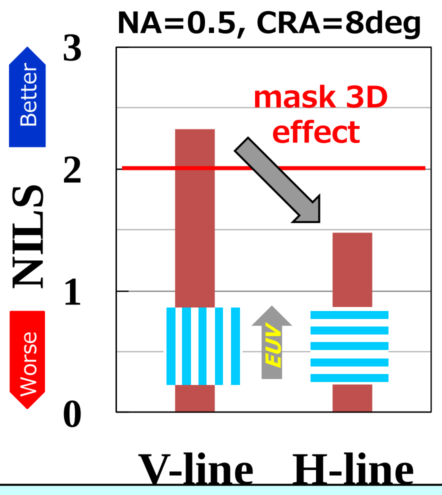


X Mag. = 6inch Mask
(5 or 8)

- **Low exposure throughput**
- **Stitching technology**



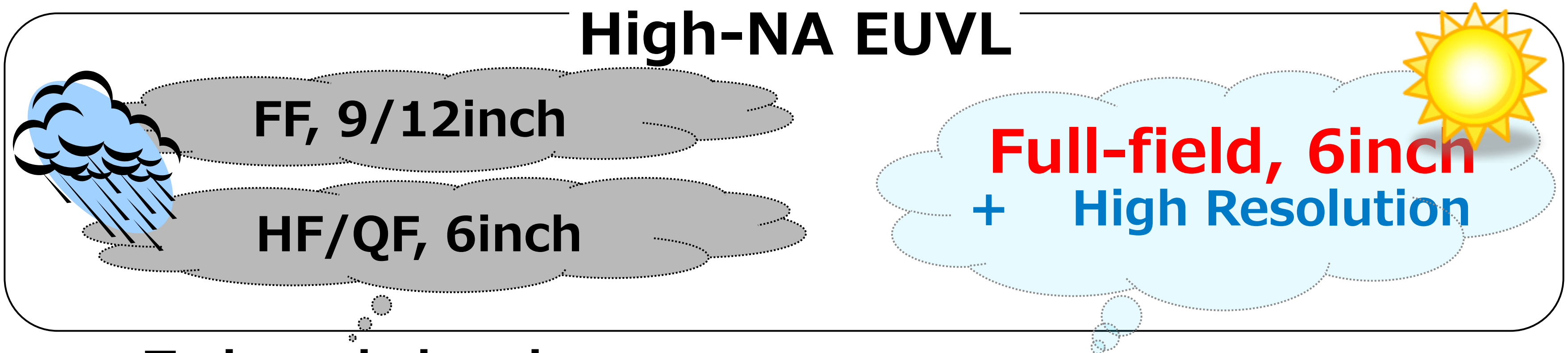




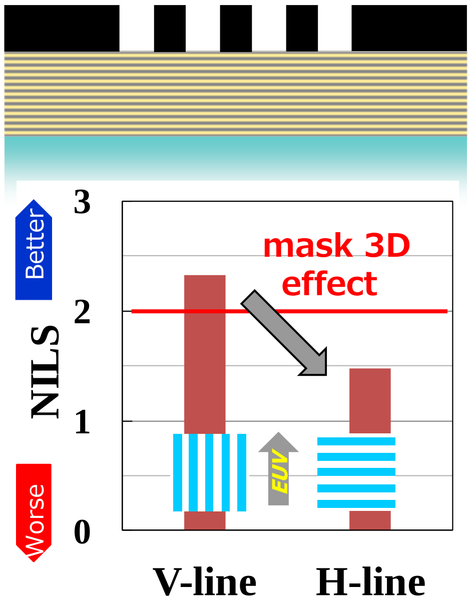
- **High NA by increasing CRA leads to large mask 3D effect**

Takashi Kamo, et al, 2013 International Symposium on Extreme Ultraviolet Lithography

High NA EUVL mask with new structure

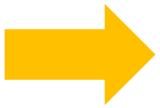


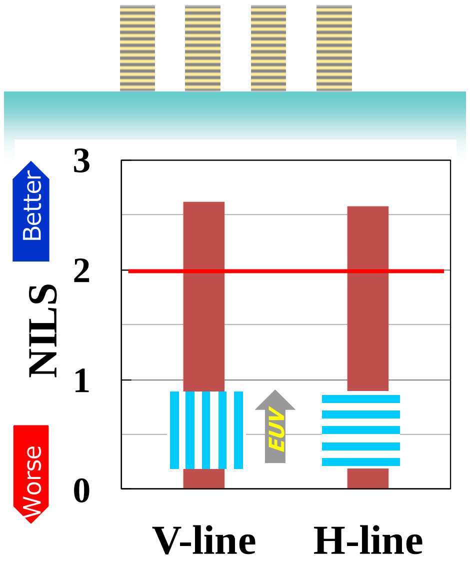
Ta based absorber



lower mask 3D effect

Etched Multilayer

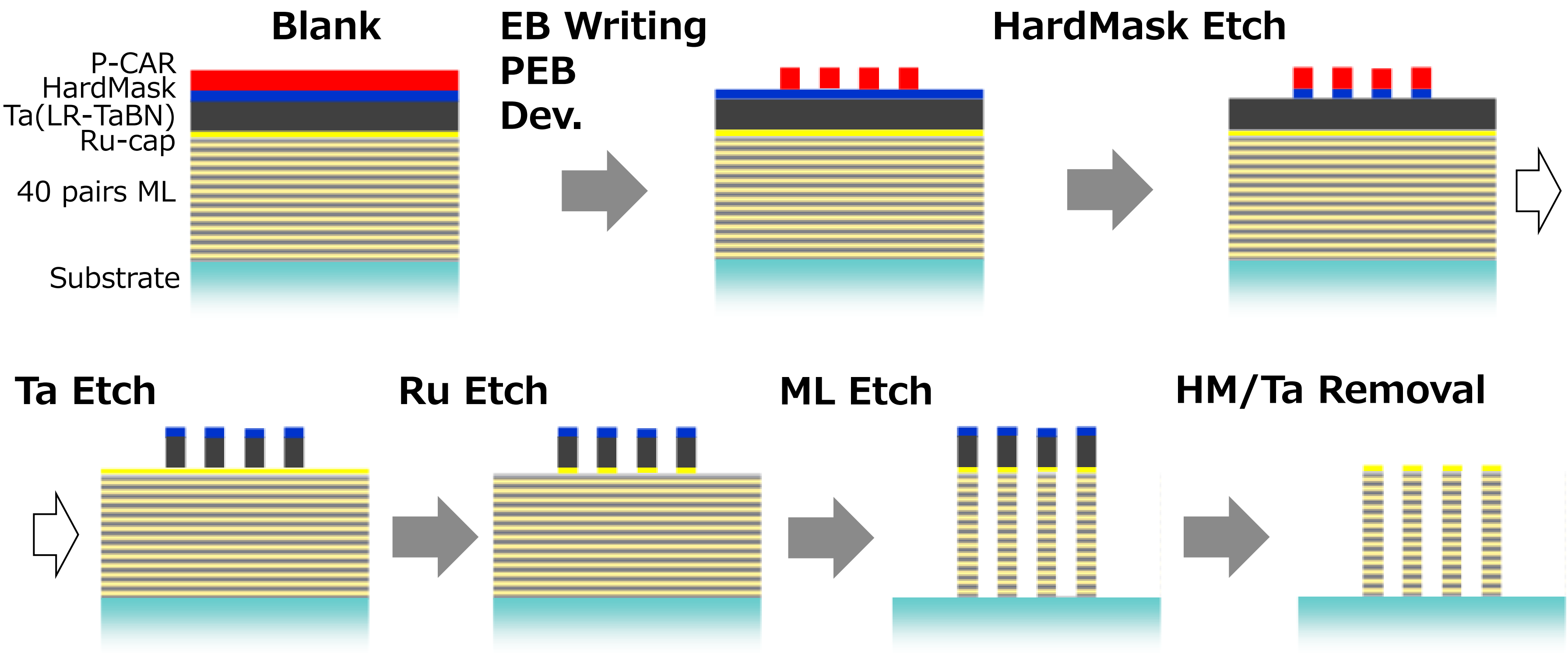




Full-field 6inch mask can keep with high NA by new mask structure !!

Takashi Kamo, et al, 2013 International Symposium on Extreme Ultraviolet Lithography

Process Flow

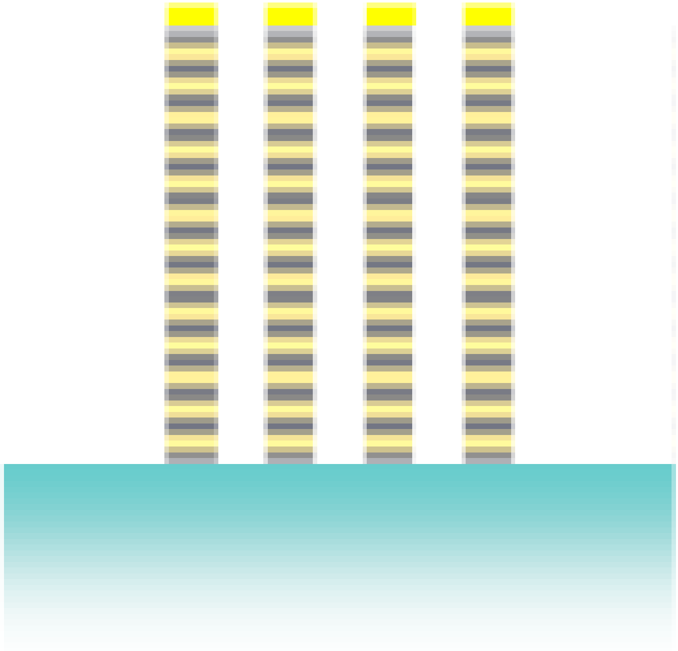


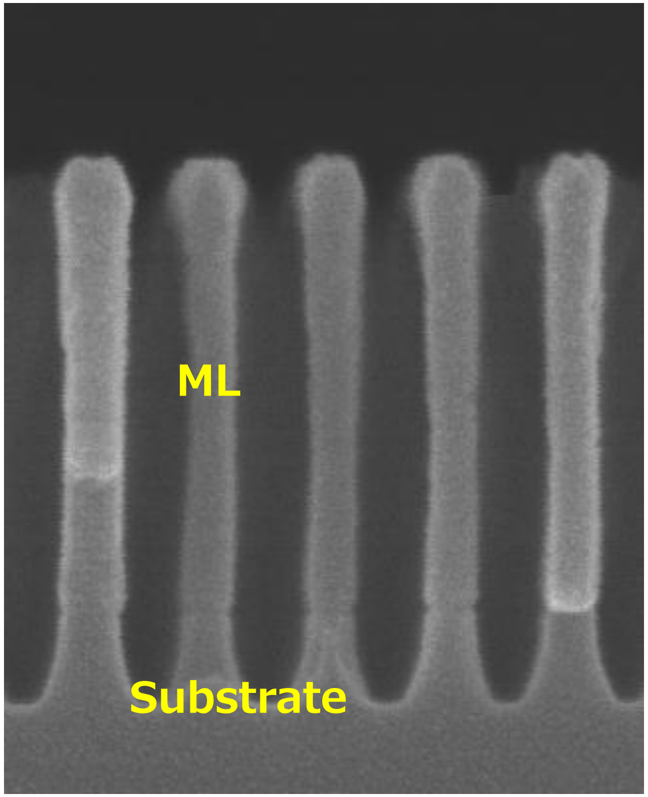
- In order to fabricate fine pattern, hardmask process is selected. Ta layer works as a secondary hardmask to etch underlying layers.
- All the dry etching processes are carried out by ARES™ (Advanced Reticle Etch System, Shibaura Mechatronics).

Takashi Kamo, et al, 2013 International Symposium on Extreme Ultraviolet Lithography

Etched ML pattern of 40 nm hp

After HM/Ta removal



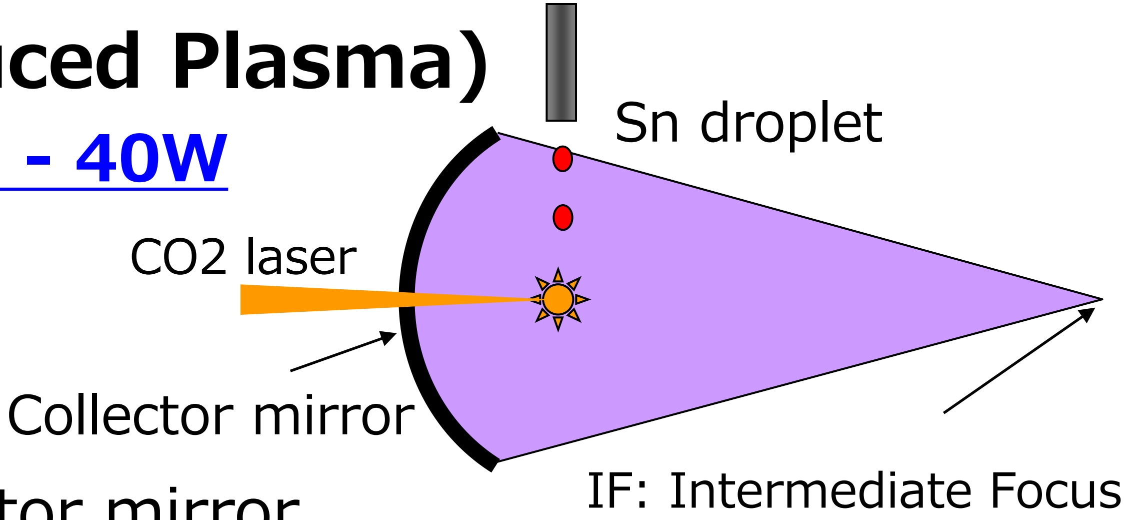


Takashi Kamo, et al, 2013 International Symposium on Extreme Ultraviolet Lithography

Etched multilayer L/S pattern of 40 nm hp on mask (10 nm hp on wafer using 4X optics) is achieved. High-NA EUVL with 4X full-field 6 inch mask will be implemented by etched ML mask.

High power source

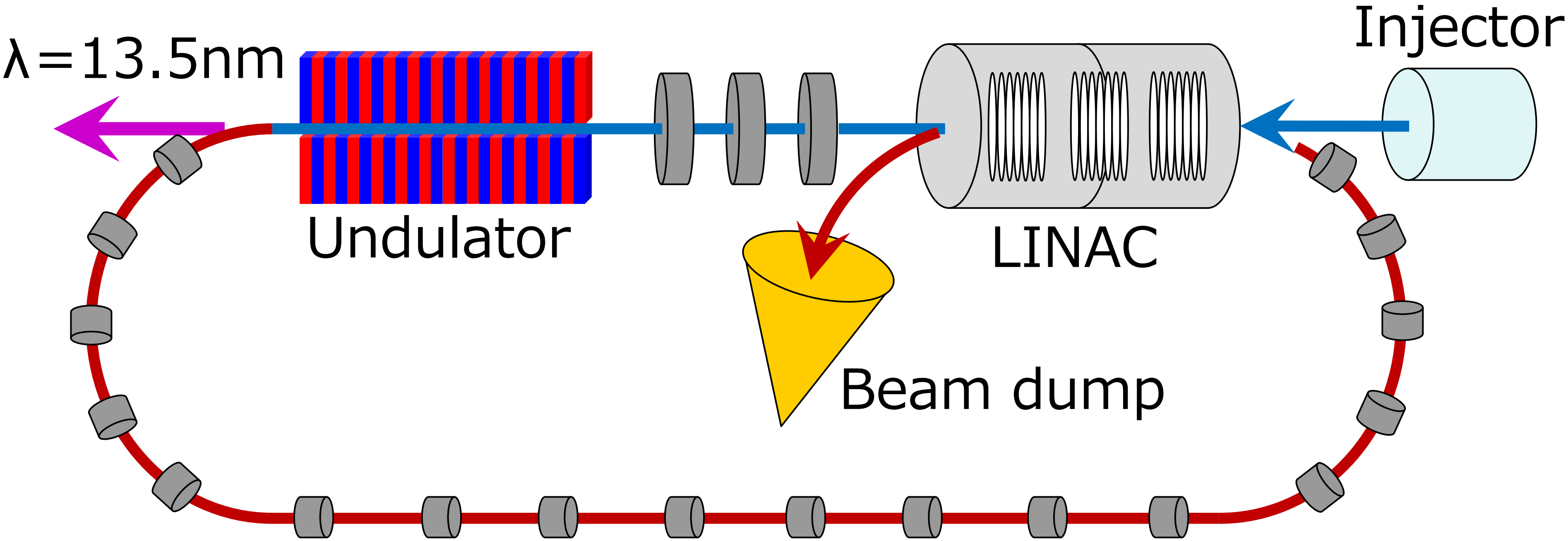
- **LPP(Laser Produced Plasma)**
  - **Current level: 20 - 40W**
  - Challenges
    - Heat treatment
    - Debris
    - Lifetime of collector mirror
    - Running cost



- **Target of source power: 250 W in 2015**
- **Big gap between target and current level**
- **High NA EUVL will need higher power**
- **Scalability of LPP source to >> 250 W ?**

FEL for EUV source

Example of high power FEL [~ >10kW]



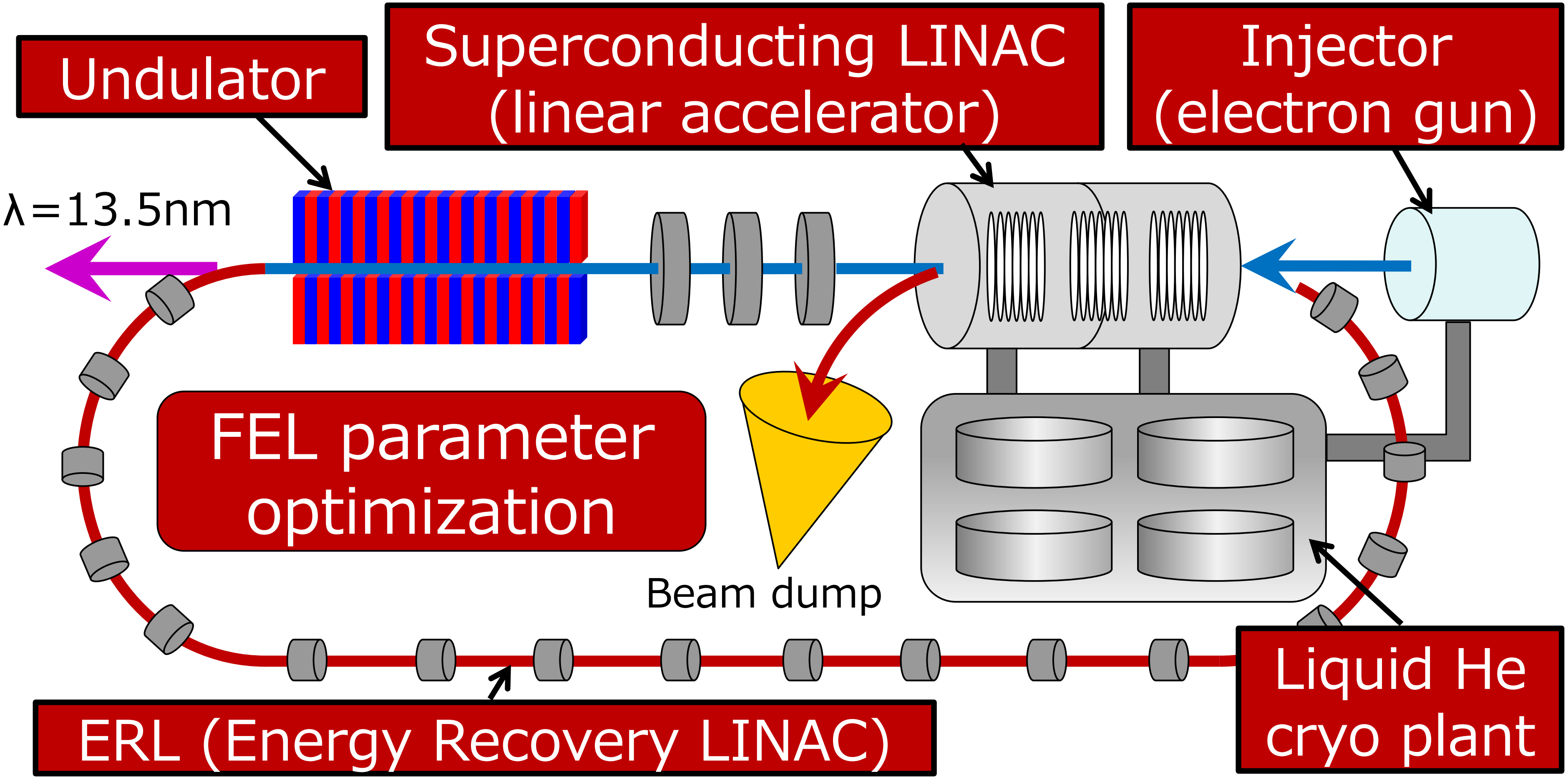
An FEL has the potential of high power source, for example over 10kW to multiple scanners.

But FEL for EUV source is still in the conceptual stage.

Concerns for FEL

- Proof of concept; FEL of λ=13.5 nm with high power of > 10 kW
- Availability for 365D/24H
- Impact for wafer cost
- Electrical power consumption
- Facilities size
- Timely readiness; long lead items

Key technologies of EUV-FEL



Undulator

Superconducting LINAC (linear accelerator)

Injector (electron gun)

FEL parameter optimization

Liquid He cryo plant

ERL (Energy Recovery LINAC)

There are many challenges for high power EUV-FEL. But nothing will be a show stopper, technically. Careful and sufficient optimization will be required.

XFEL in the world


SACLA (RIKEN, Japan)

SLAC (LCLS, USA)

FLASH (DESY, Germany)
Swiss FEL (PSI, Switzerland)
FERMI (Elettra, Italy)

We are here, Maui.

No FEL of λ=13.5nm in the world.

FEL and ERL technologies in Japan

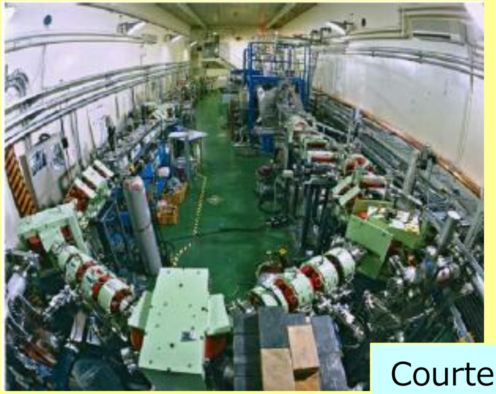
SACLA x-ray FEL (RIKEN, Hyogo)

λ=0.1nm
60Hz/24mW

Courtesy of RIKEN

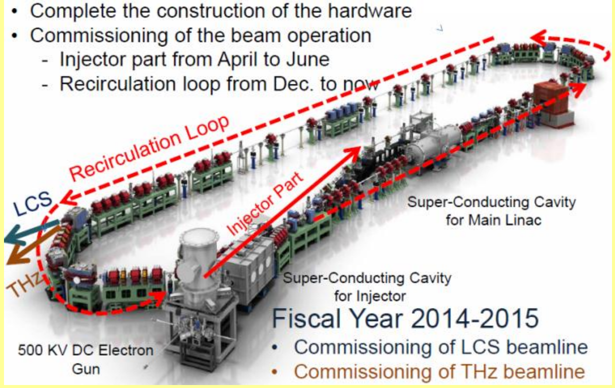
IR-ERL-FEL (JAEA, Tsukuba)

λ~50μm
2kW



Courtesy of R. Hajima

cERL (KEK, Tsukuba)



- Complete the construction of the hardware
- Commissioning of the beam operation
  - Injector part from April to June
  - Recirculation loop from Dec. to now

Fiscal Year 2014-2015

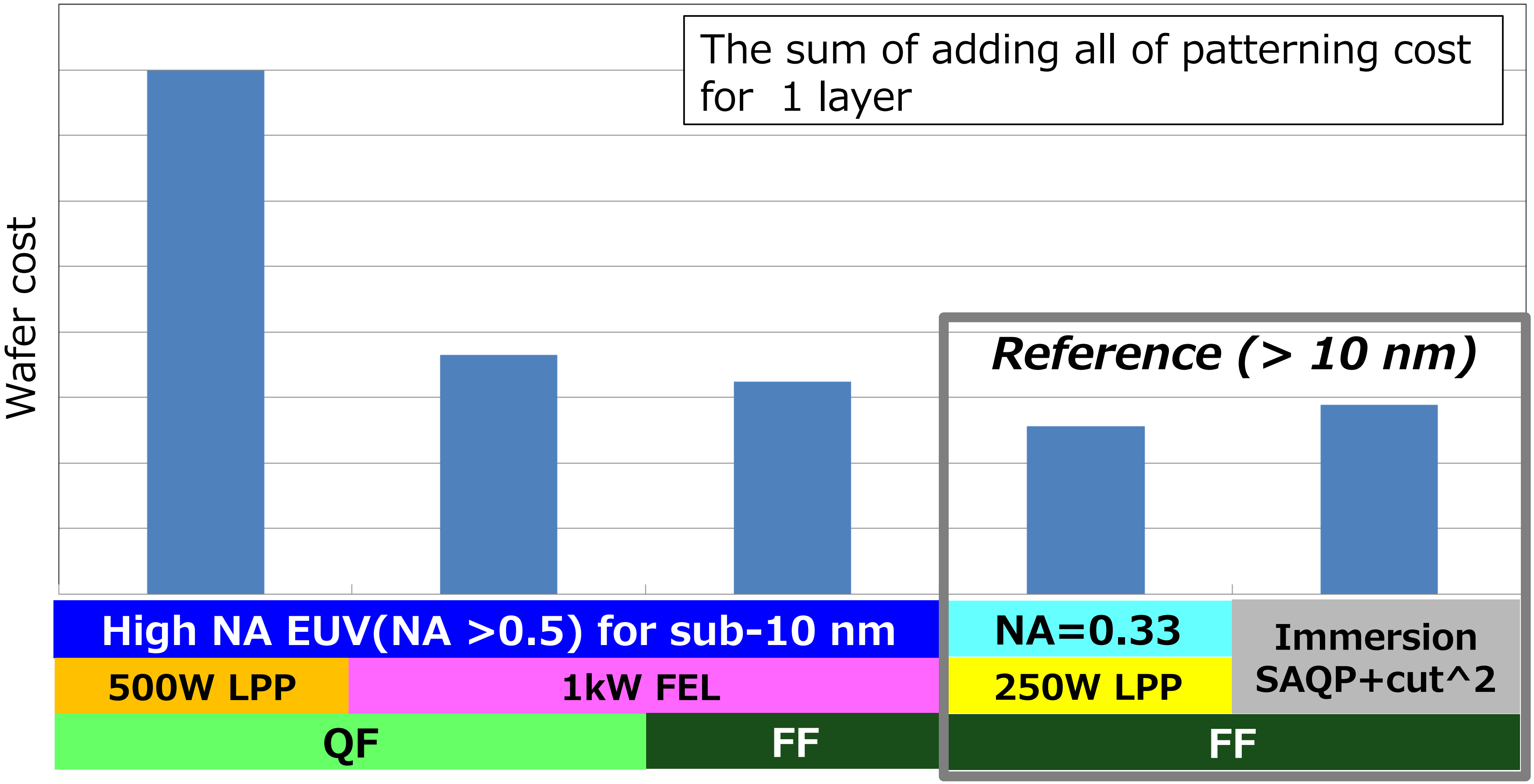
- Commissioning of LCS beamline
- Commissioning of THz beamline

Courtesy of KEK

There are many fundamental technologies related to FEL and ERL in Japan.
By using current technologies and experience, implementation of EUV-FEL source will be possible.
But it will take long time to develop.

Comparison of wafer cost

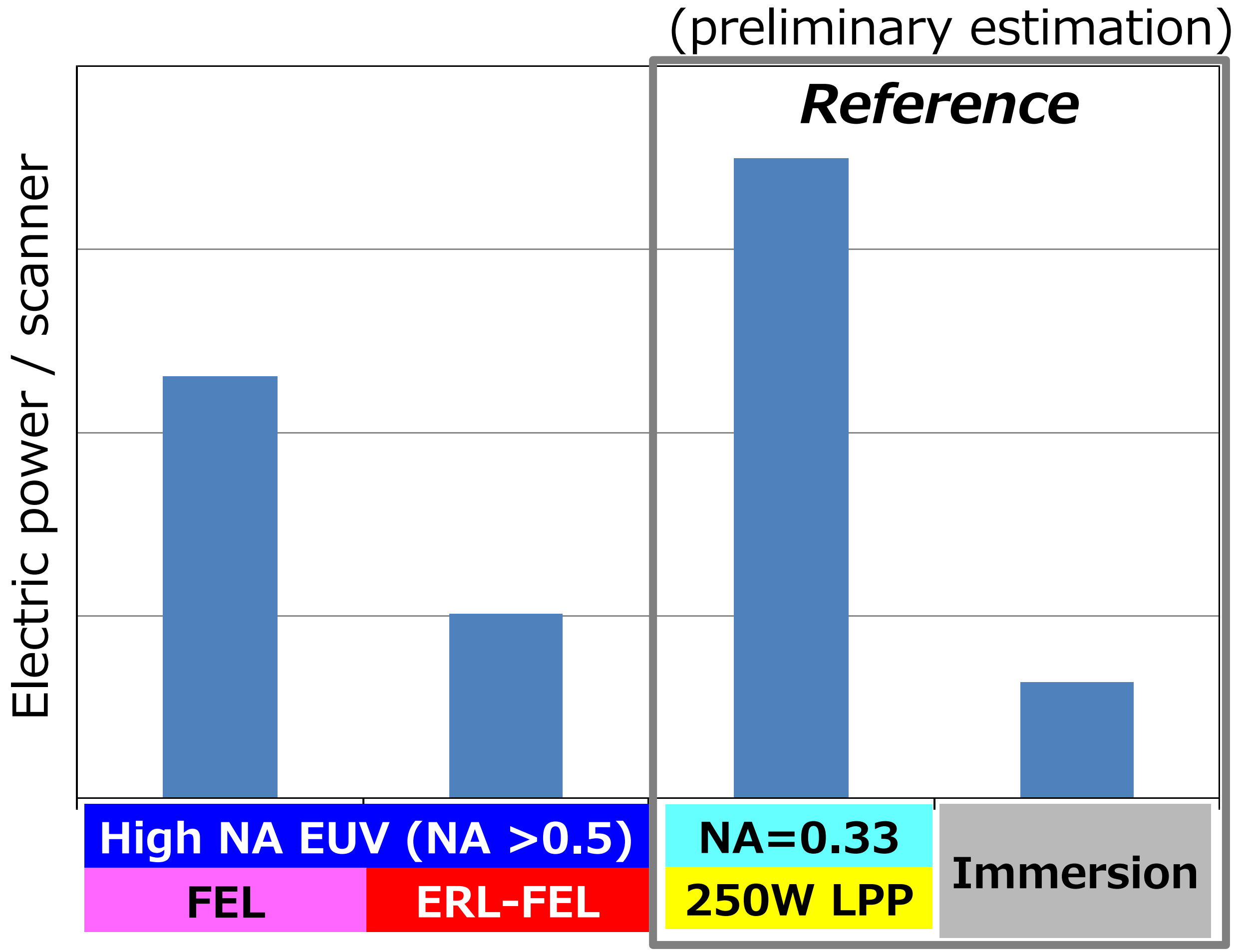
(preliminary estimation)



The sum of adding all of patterning cost for 1 layer

Wafer cost of FEL is expected to be lower than LPP.

Electric power consumption



ERL will reduce the electric power consumption of FEL.

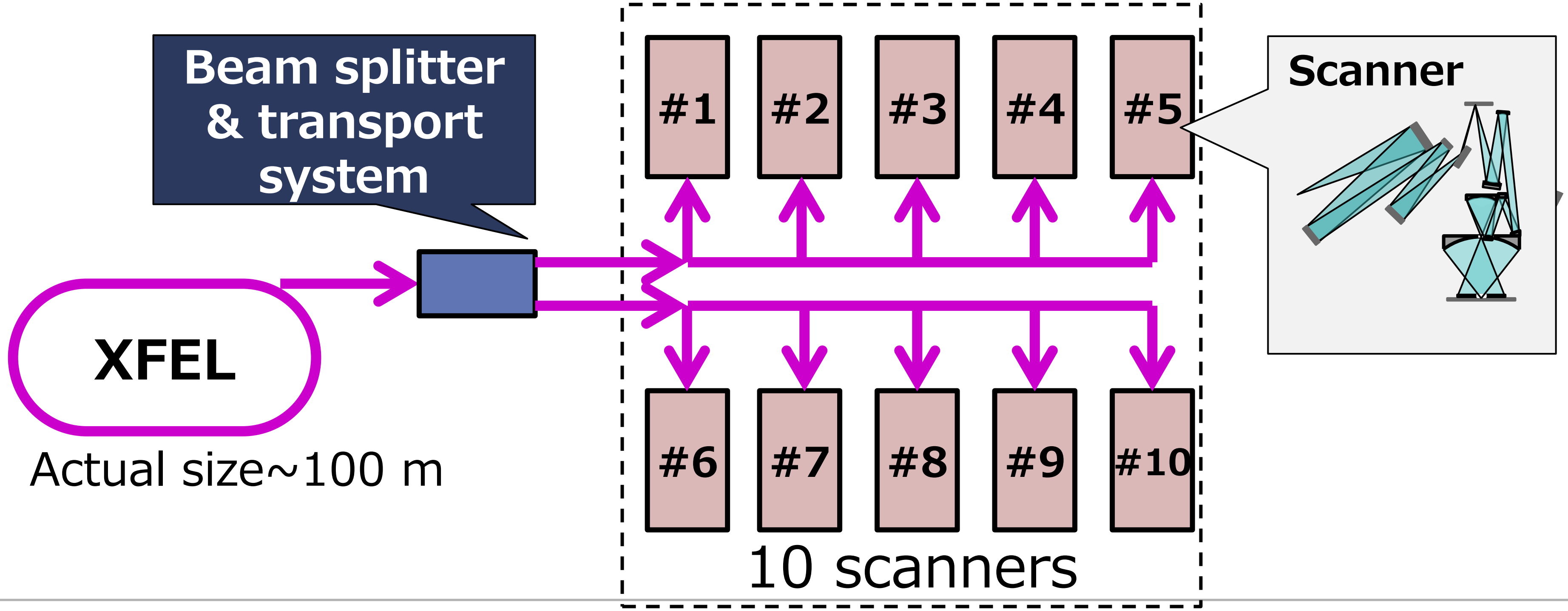
Concerns for FEL

- Proof of concept; λ=13.5 nm / > 10 kW
  - *?? Need research and development*
- Availability for 365D/24H
  - Redundancy system
- Impact for wafer cost
  - FEL cost is expected to be lower than LPP. Need detail estimation.
- Electrical power consumption
  - FEL will be better than LPP.
- Facility size
  - Very large underground facilities (~100 m)
- Timely readiness; long lead time items
  - Long term project management

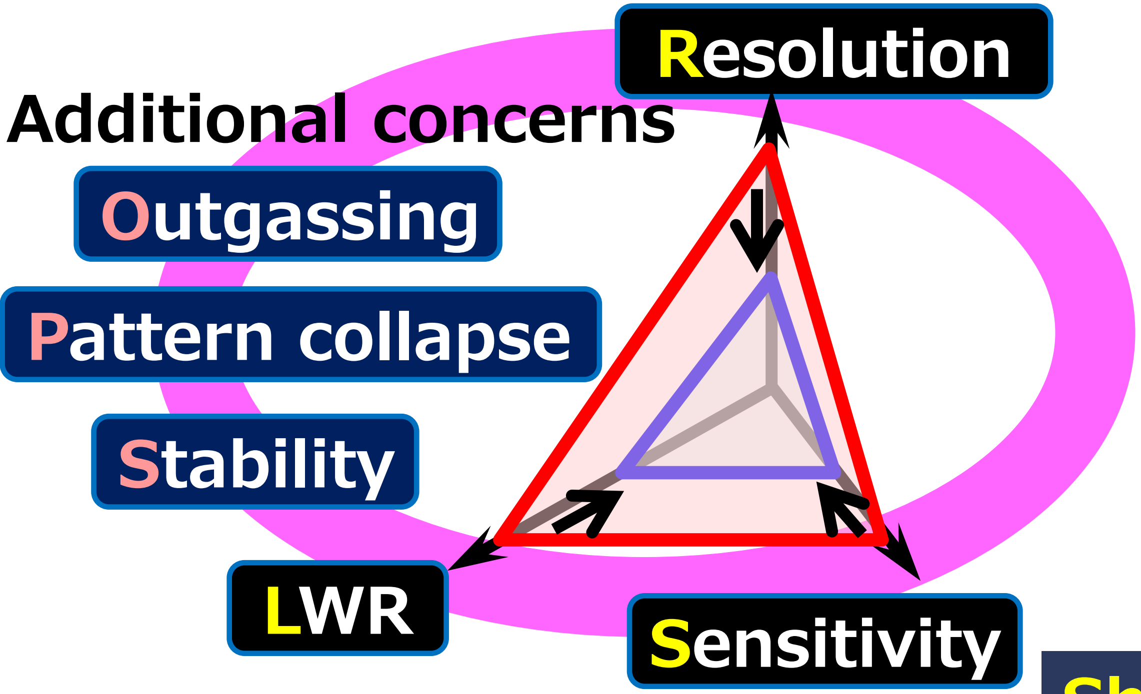
Optics for high NA and high power

- Increase in NA (≥ 0.6) leads the specification of mirror roughness and aberration tighter.
- Damage due to high power EUV light for all optics (e. g. beam splitter and transport system, ML mirror, mask and pellicle)

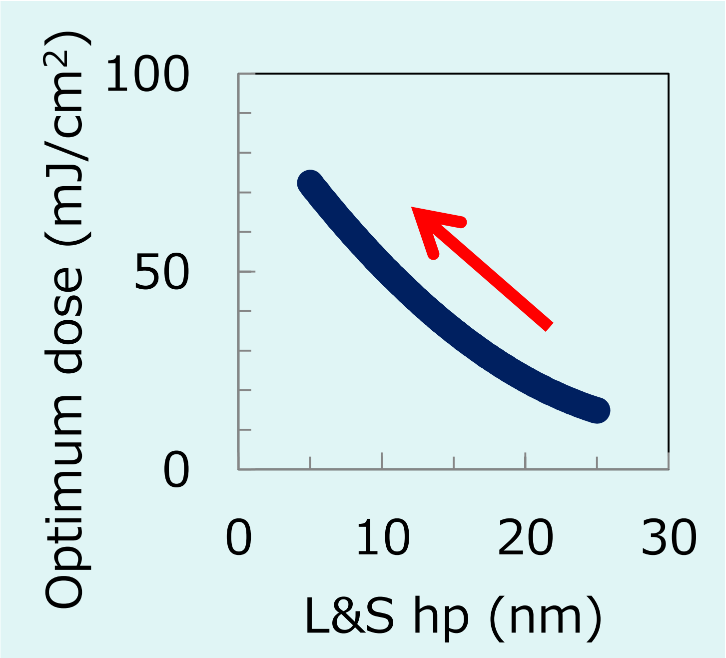
➔ Concern for durability



EUV resist tradeoff


Additional concerns

- Outgassing
- Pattern collapse
- Stability

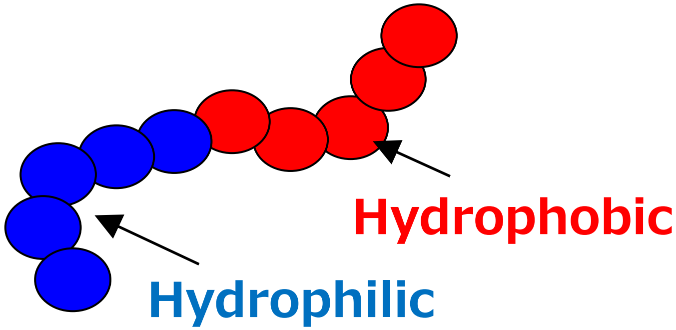


Shot noise!
➔ Higher dose for smaller hp

Difficult to overcome RLS tradeoff.
We need high resolution 1st for sub-10 nm.
Not only CAR but also alternative platform resist such as inorganic resist should be considered more.

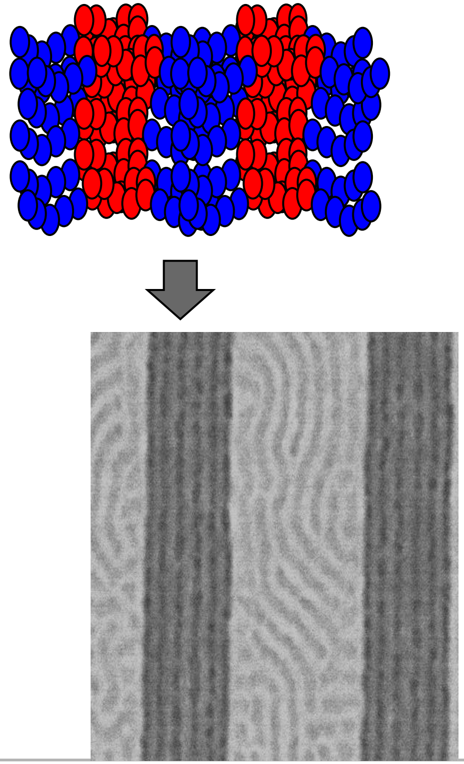
DSA has the potential of sub-10nm patterning.

DSA will be a complementary technology for all other lithography without expensive exposure tool. → potential of low cost lithography

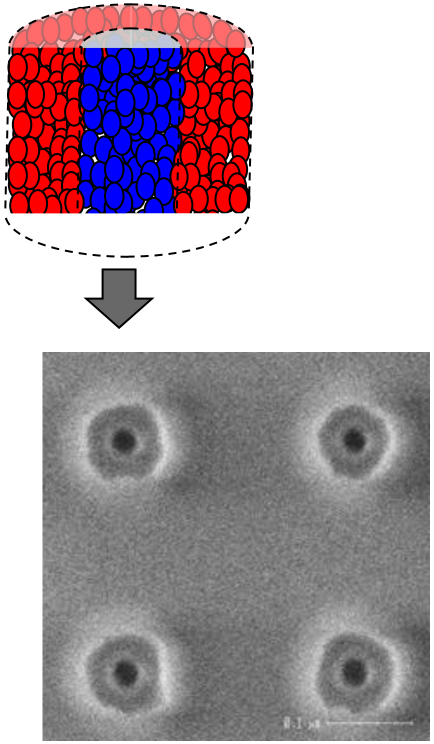


DSA polymer

L&S patterning



Hole shrinking

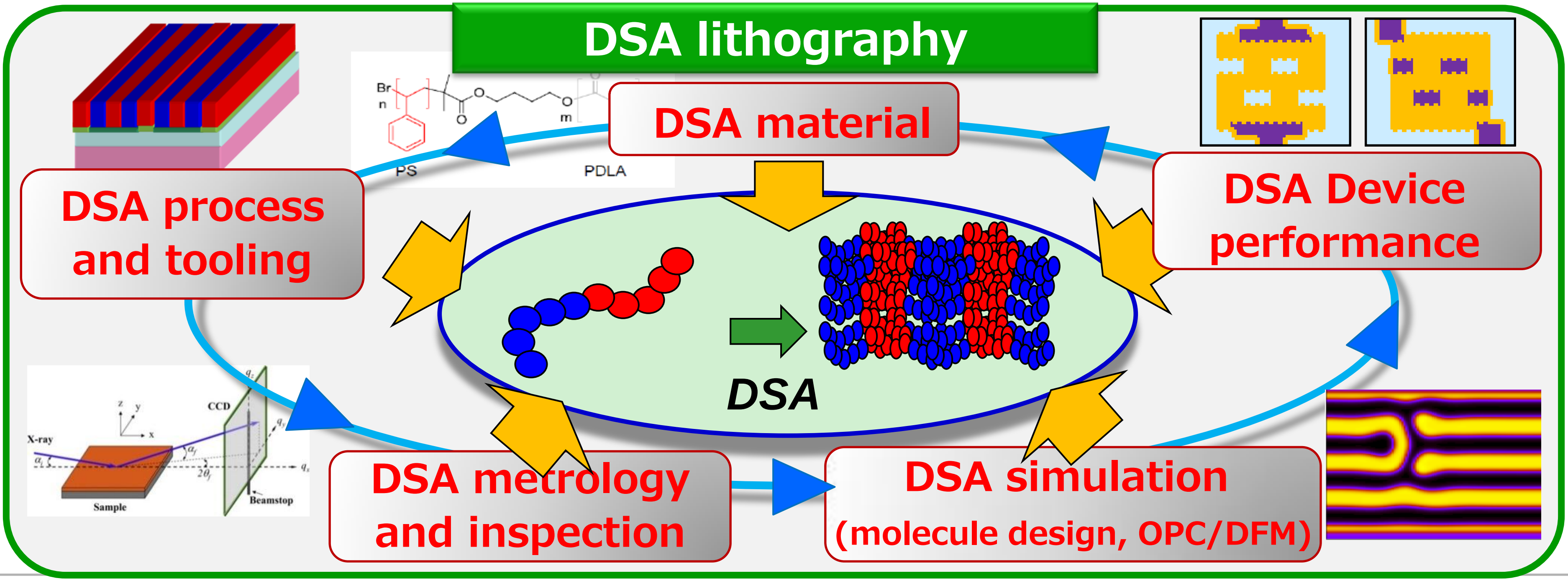


DSA collaboration

We hope DSA development for sub-10 nm patterning as complementary technology for NGL will be accelerated by collaboration.

Challenges

- Defectivity
- Pattern placement error
- Process stability
- Metrology and inspection
- Optimization of guide pattern design



DSA lithography

DSA material

DSA process and tooling

DSA Device performance

DSA

DSA metrology and inspection

DSA simulation (molecule design, OPC/DFM)

EIDEC activities

Blank Inspection technology

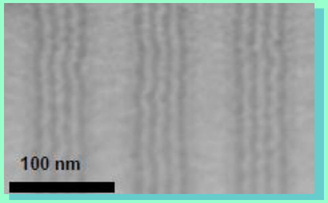
- Actinic BI tool technology
- Lithographic impact
- Defect characterization

EUV Resist out-gassing Control

- Criteria of resist out-gassing
- Quantitative analysis
- EB based method
- Correlation between EB & EUV

DSA research

- DSA standard process platform
- High χ material & process
- DSA simulation
- 3D nanostructure analysis

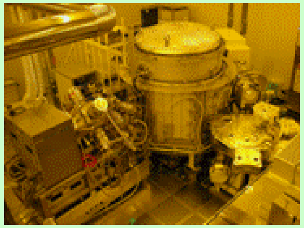


Patterned mask Inspection technology

- PMI tool technology with EB projection optics
- Defect characterization
- Lithographic impact

EUV Resist Material research

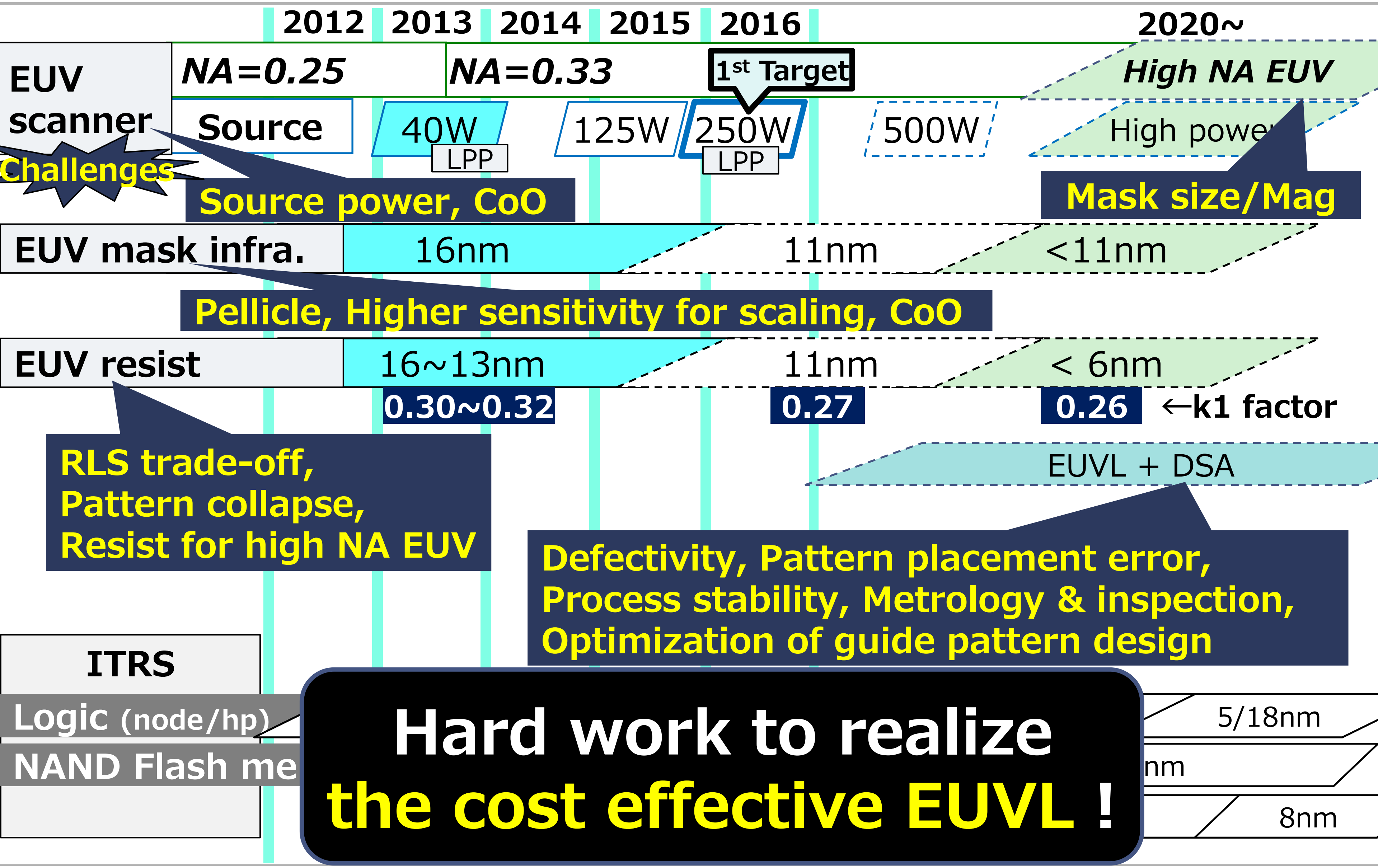
- SFET utilization
- Fundamental research
- New resist platform
- Alternative resist process



Courtesy of EIDEC

We hope to make full use of EIDEC results for implementation of NGL.

Trend of EUV lithography



Source power, CoO

Mask size/Mag

Pellicle, Higher sensitivity for scaling, CoO

RLS trade-off,
Pattern collapse,
Resist for high NA EUV

Defectivity, Pattern placement error,
Process stability, Metrology & inspection,
Optimization of guide pattern design

Hard work to realize
the cost effective EUVL !

Nano-particle management

- Nano-particle and -chemical contamination will be critical issues of manufacturing for future memory.
- There is a big gap between current level and future requirement, as follows.

	Current level	Req. in 2016	Req. in 2020
Min. defect size (nm)	25	12	5
Defect density (/cm2)	< 1	< 0.1	< 0.01

We need to establish nano-particle control & management techniques to close the gap.

Keeping cleanness, visualization of contamination, and cleaning technique are essential for mass production of future memory.

Lithography candidates for each device generation

(Table ORTC & Table PIDS7b of ITRS 2013)

LELE

EUV LELELELE・・・

High NA EUV / DSA

SADP/QP

	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
Logic node	16/ 14		10		7		5		3.5		2.5		1.8		1.3
Logic Metal hp	40	32	32	28	25	23	20	18	16	14.2	12.6	11.3	10.0	8.9	8.0
Logic Fin hp	30	24	24	21	19	17	15	13	12	10.6	9.5	8.4	7.5	6.7	6.0
NAND Flash 2D															
NAND Flash 3D															
DRAM															
PCRAM															7
ReRAM															4

Multiple patterning
or
Low power EUV
→ High NA EUV/DSA+EUV

We choose the lithography from the point of view of cost.

Summary

- **High NA EUVL** is the most promising candidate for sub-10 nm lithography, because of its patterning potential.
- We should take our best effort to establish **cost effective** high NA EUVL.
- There are many **concerns** for high NA EUVL.
  - Etched ML mask will enable **4X full-field 6 inch mask**.
  - **Higher power source** will be required for sub-10 nm. An FEL is one of the candidates for future high power source.
  - **Damage** due to high power EUV light for all optics is concern for durability.
  - Alternative platform **resist** should be considered more for sub-10 nm.
- DSA will be **complementary** technology to all other lithography for sub-10 nm.
- We need to establish **nano-particle** control & management techniques for future scaling.

TOSHIBA

Leading Innovation >>>