Advanced Mask Patterning & Wafer Level Defect Detection (P68)

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Outline

Advanced Mask Patterning

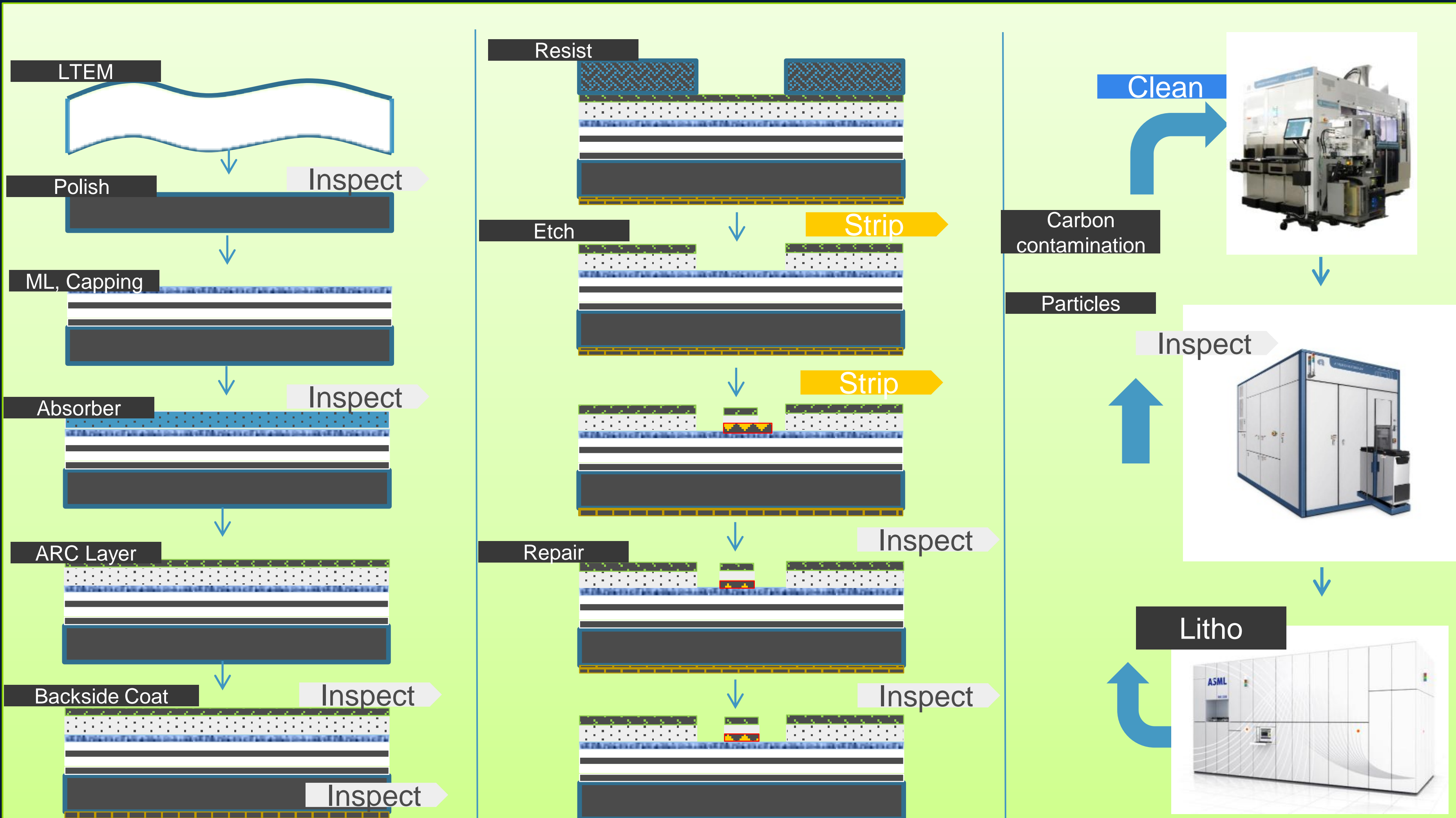
A. EUV Mask Cleans

B. EUV Mask Etch Requirements & Results

EUV SADP Programmed Defect Study

C. Defect Evolution Through SADP Flow.
Resolution Challenges and Approaches for 1xnm Defects

A) EUVL Reticle Cleans Space



Defect-Free Blank/Mask Interfaces Require Effective Damage Free Cleans

EUV Blanks/Mask Cleans Requirements

Prevent Ru Damage +/= Minimize R% Loss

Damage Free Features, Mask Back-side Cleans +/= No CD Loss, No Image Distortions

Carbon Contamination Removal + Particles removal

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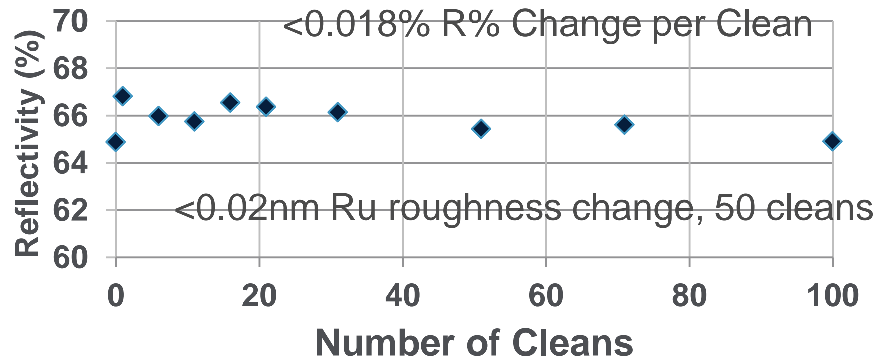
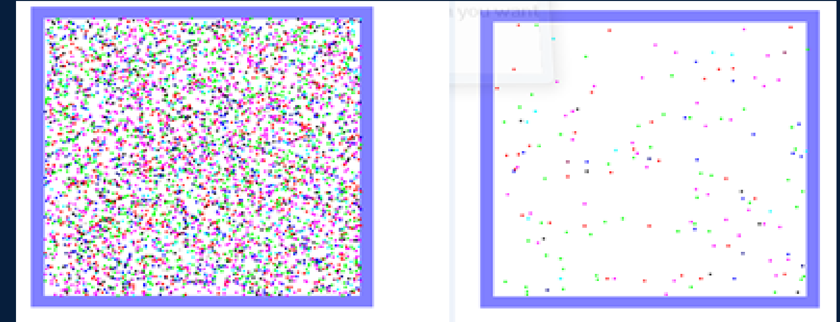
AMAT Reticlean Performance

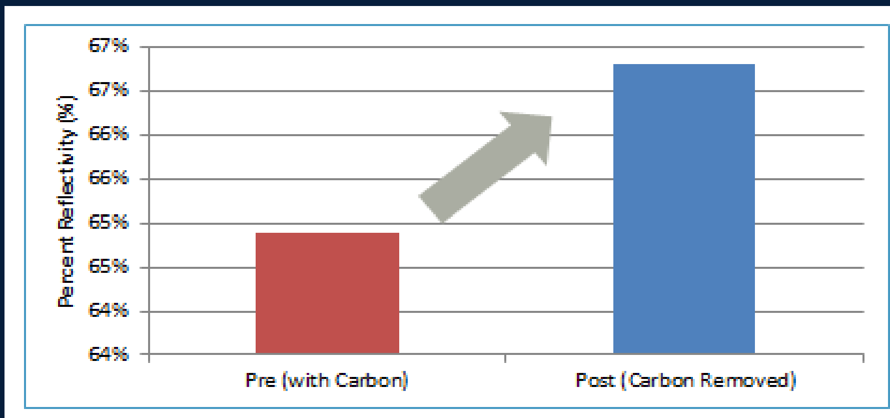


Effective EUV Mask Cleans Demonstrated Within Fab HVM Requirements.

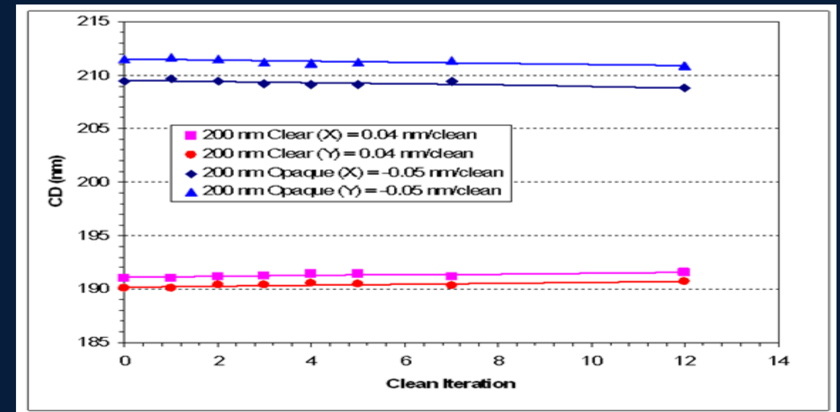


Programmed Defect Study

- Net Defects Reduction from ~5000 to <200 (10-50nm)



Increase in R% with Carbon Removal



<0.05nm/clean CD loss per clean)

Innovative "Wet + Dry" Based Approach to Ensure EUV Mask Spec Compliance.

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B) Tetra™ Mask Etch Capabilities

	Current performance		Under Development
Specification	**Tetra™ X**	**Tetra™ EUV**	**Tetra™ Z**
Node	**22/16nm**	**16/11 nm***	**11/8nm**
CDU (3σ)	**≤2nm**	**≤2nm**	**≤1.5nm**
Linearity	**≤5nm (70nm – 1μ)**	**≤5nm (60 nm - 1μ)**	**≤3 nm (50nm - 1μ)**
Iso-Dense Microloading	**≤1.5nm**	**≤1.5nm**	**≤1.5nm**
Resist Thickness **Cr:PR Selectivity**	**1500 Å** **0.7:1**	**1500 Å** **0.7:1**	**1000 Å** **1.5:1**

- ICP source
- Dynamic multi-port gas injection for uniformity control
- Advanced materials for defect control
- In-situ Quartz depth endpoint

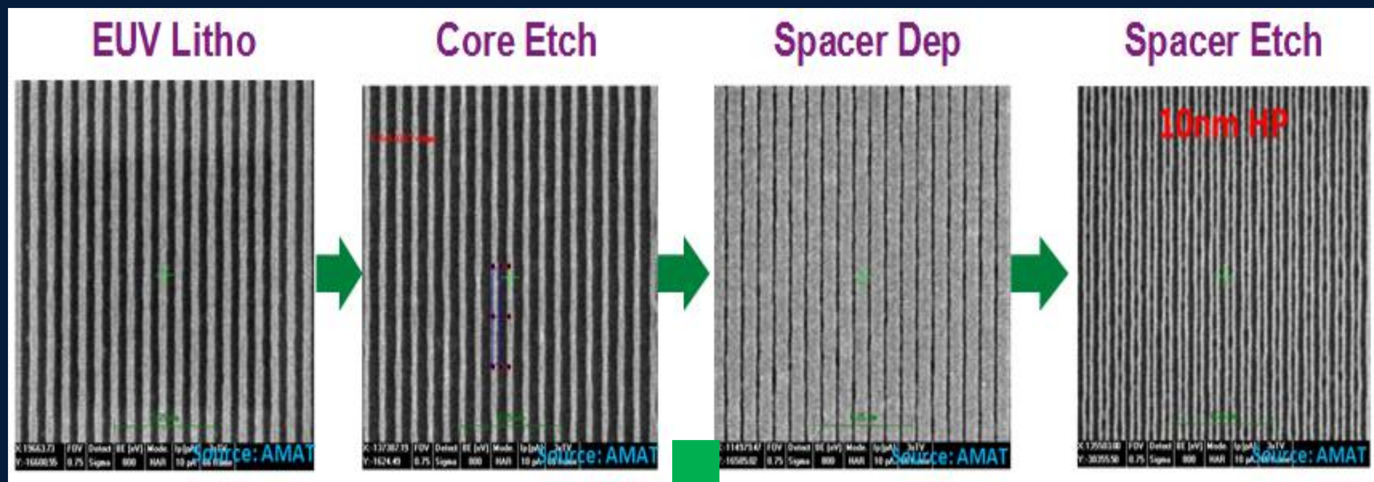
<2nm 3S EUV Mask Etch CDU Demonstrated: Ready to Intercept EUV HVM

C) 2013: 9/10nm HP EUV-SADP Demonstrations

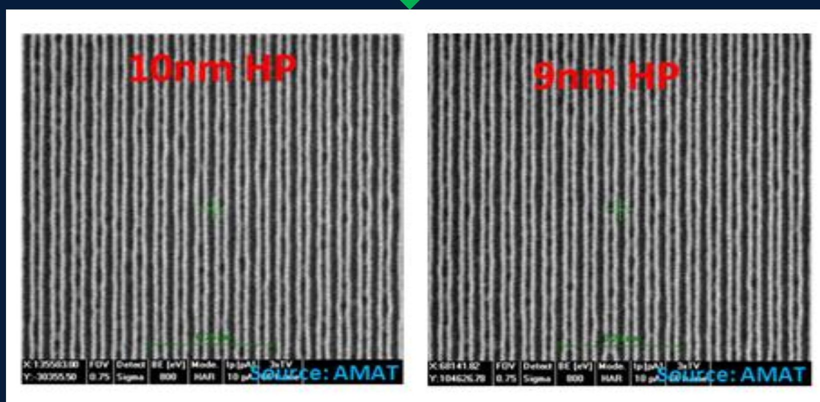
NXE 3300B
NA 0.33, Dipole
50nm Resist Thx
FIRM Rinse

Nitride
APF
Poly
Pad Oxide
Si

20nm 1:1 L/S Patterns



AMAT Producer PECVD



AMAT Mesa Etch

10nm L/S **9nm L/S**

Enabler for Low 1x,y,z nm Planar Flash Scaling and Gridded Logic Layouts

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Programmed Defect Mask

Print programmed defects using EUV lithography in a systematic grid of known size, shape, and location

- Pattern spacing: 30, 32, and 35 nm areas
- Defect sizes: 8 – 36 nm
- Defect shapes: Pindot or extension (1:1 1:2 2:1)

EUV lithography mask

L & S	Defect Size (nm) 8	10	12	14	16	18	20	22	24	26	28	30	32	36	Type
30 nm															A
															B
															C
															D
															E
															F
32 nm															A
															B
															C
															D
															E
															F
35 nm															A
															B
															C
															D
															E
															F

size as designed @ 1X		8	10	12	14	16	18	20	22	24	26	28	30	32
pindot	X/Y 1:1													
	X/Y 1:2	No pictures available												
	X/Y 2:1	No pictures available												
extension	X/Y 1:1													
	X/Y 1:2	No pictures available												
	X/Y 2:1	No pictures available												

Each square represents a defect location

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DUV Dual-channel Inspection Results

- Inspected 234 programmed defect locations after each process step
  - Smallest programmed size detected: **14nm**
    - Missed defects were typically small extensions, similar to line roughness

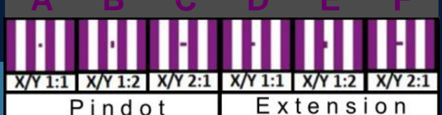
LITHO | ETCH | DEP | SADP

L & S: 30 nm, 32 nm, 35 nm

Defect Size (nm): 8 10 12 14 16 18 20 22 24 26 28 30 32 36

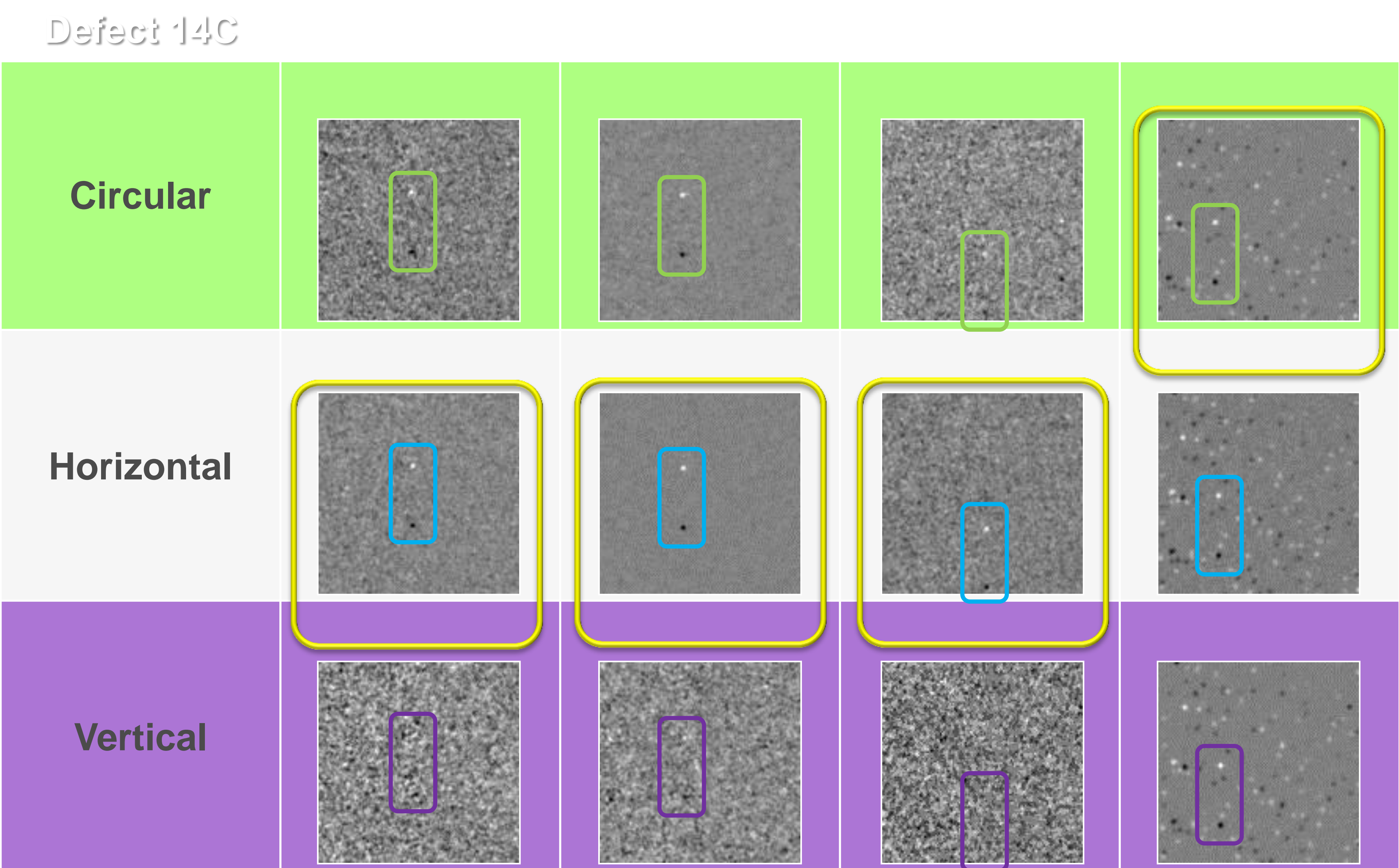
Type: A B C D E F

No Defect | NOT Detected | Detected | Size DNE



Difference Image & SNR Value: Defect 14C

- Polarization Dependence of SNR



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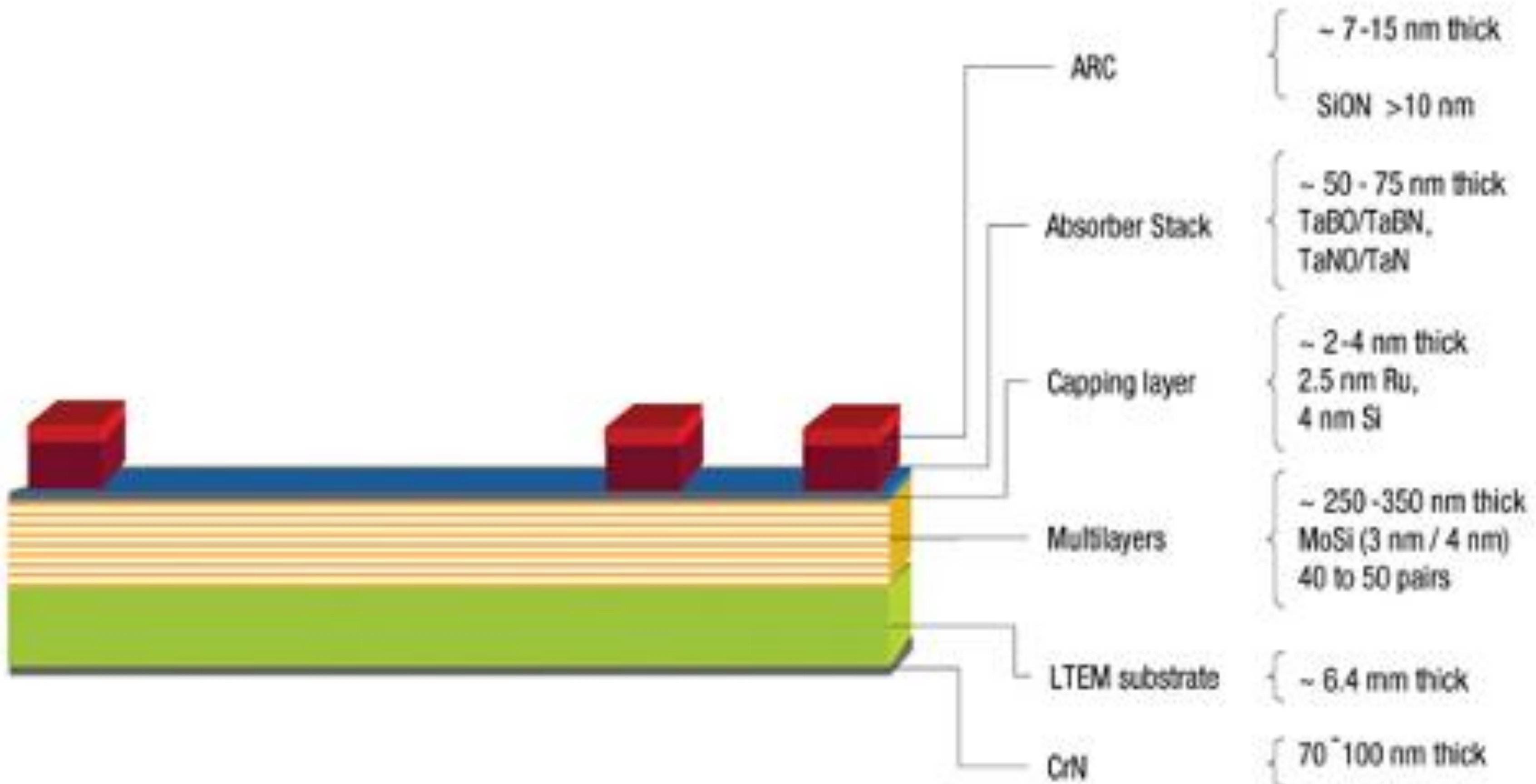
Conclusions

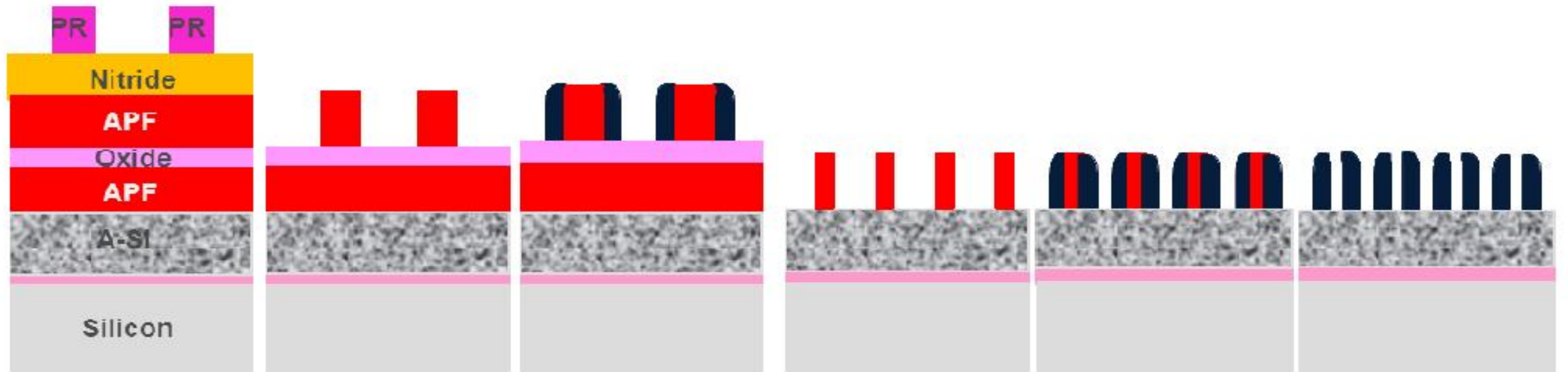
- EUV HVM for 7nm node likely will require double patterning @ K1< 0.28 (for aggressive layout needs).
  - Higher NA options or layout trade-offs might be required to allow single exposures at 7/5nm.
  - 8nm HP SADP wafer results demonstrated.
- EUV Mask Etch CDU and Mask Cleans Driven Defect Performance Successfully Demonstrated.
  - Minimal CD and R% loss shown through multiple cleans
- Wafer level inspection capability will be key as EUV likely will intercept sub10nm logic/foundry node HVM.
  - 14nm defects detected on EUV SADP processed wafers.
  - Defect resolution study indicates need for advanced optical platform features (polarization, improved optics, sources).

Dimensions and Critical Parameters

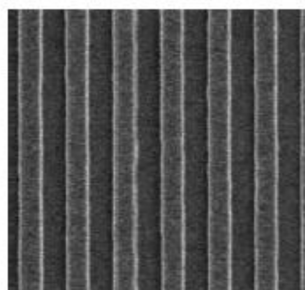


CTE(<5ppb/degc), HSFR, MSFR (<0.08nm RMS), Flatness (<25nm), Defects (0.03/cm2 at 20nm), Dep Temp (<150 deg),EUV Reflectivity (>70%)
➔ Image Plane Distortions, Power Degradation, LER, Defects.

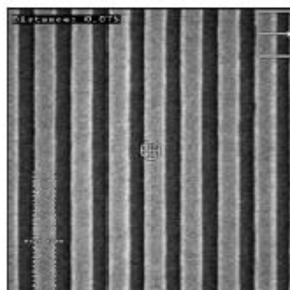
193i SAQP: The Other Alternative



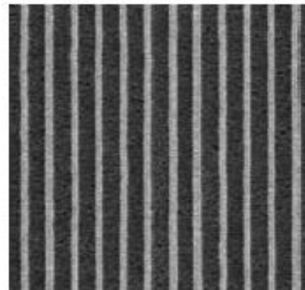
- Illustration of process flow of the SAQP scheme 1



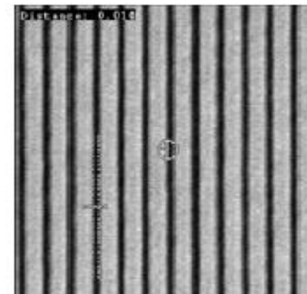
Top mandrel etch



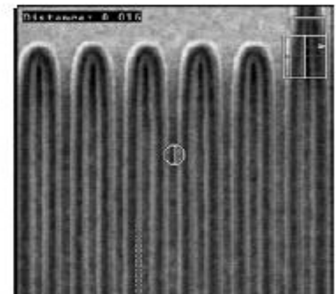
NIT Spacer1 Deposition



NIT Spacer1 etch, top mandrel strip & bottom mandrel etch



NIT Spacer2 Deposition



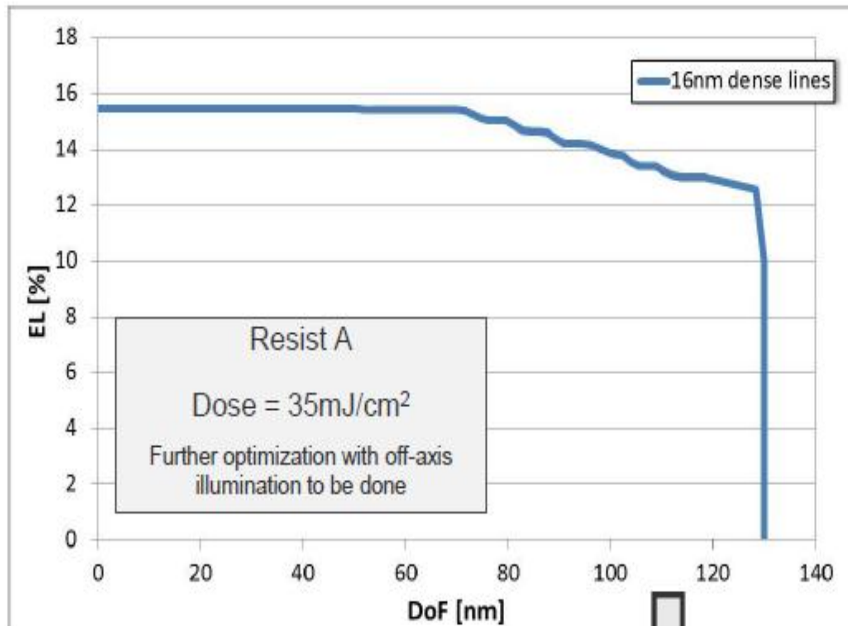
Bottom mandrel strip to form final pattern

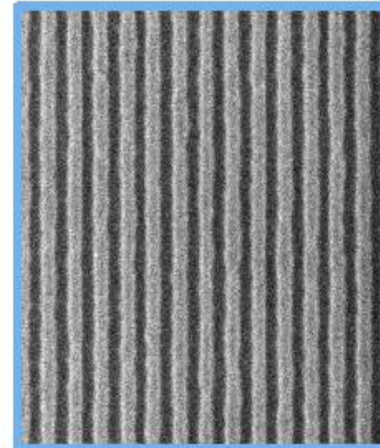
2x SADP with Increased Process Costs and CDU Challenges

EUV SADP Could Scale ~ 8nmHP(1:1) with Resist/Source Improvements

16nm dense lines with >15% exposure latitude and >120nm DoF on NXE:3300B (dipole-45 setting)

ASML





16nm L/S Dipole 45X
29.0mJ/cm2
Resist B