ASML

EUV Lithography Insertion in High-Volume Manufacturing

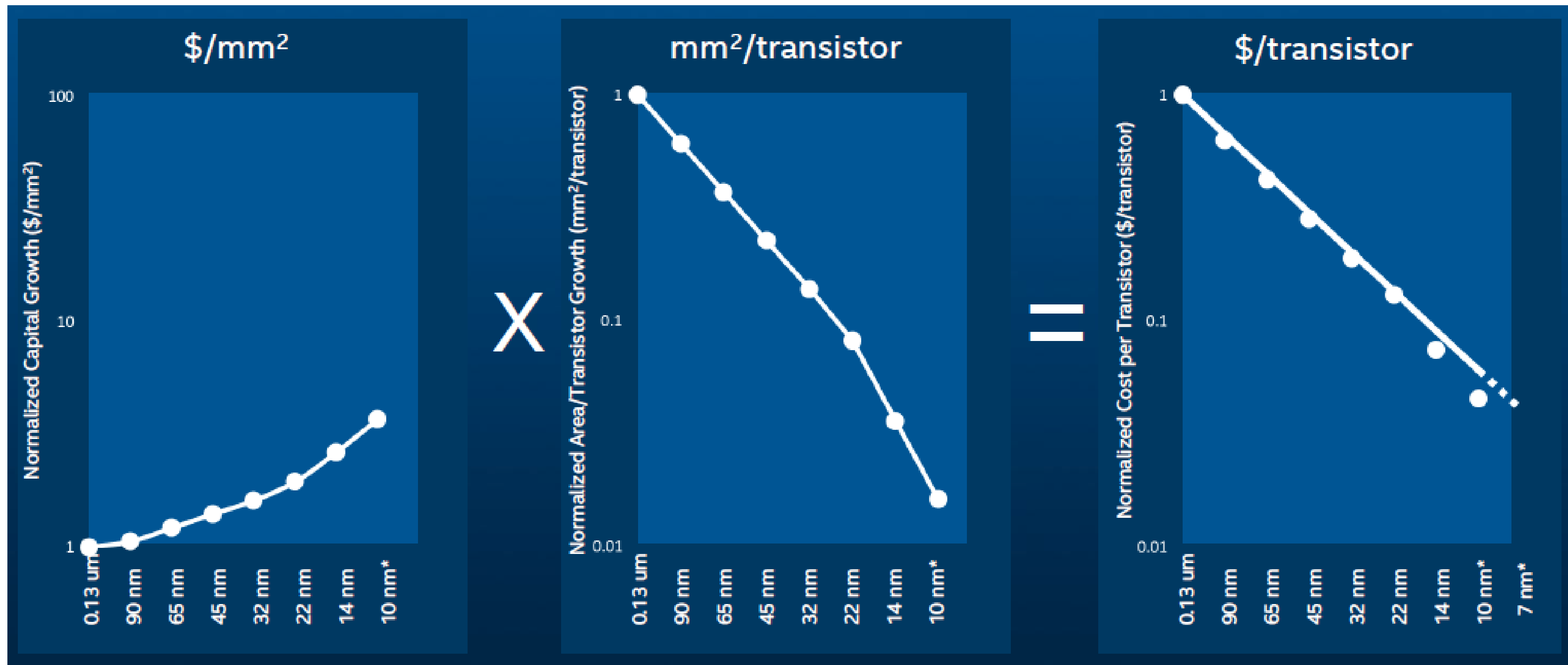
Our expanded EUV cleanroom

Agenda

- ***EUV Insertion***
- Source power and availability
- Imaging & Overlay
- Defectivity & Pellicle
- High NA
- Summary

The ambition: Continued cost per function reduction

Pace of feature shrink is even accelerating



Source: Bill Holt, Intel, “Investor Meeting 2014”, November 2014

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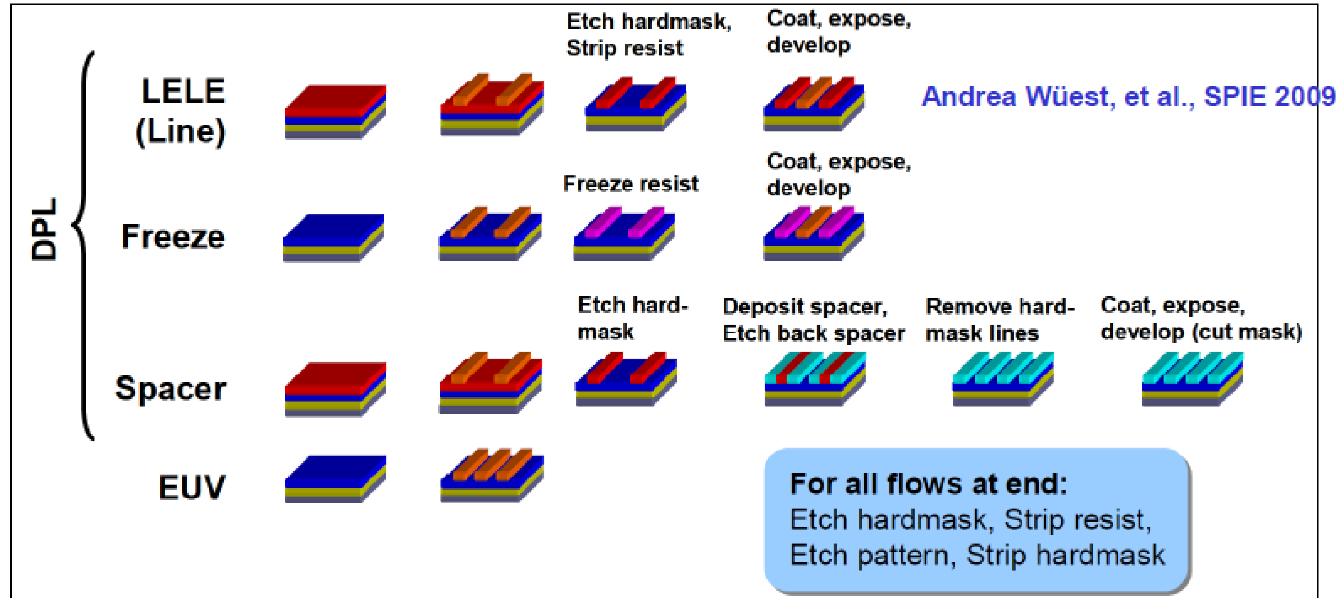
TSMC Property

EUVL simplifies patterning process!

Example for multi-patterning techniques:



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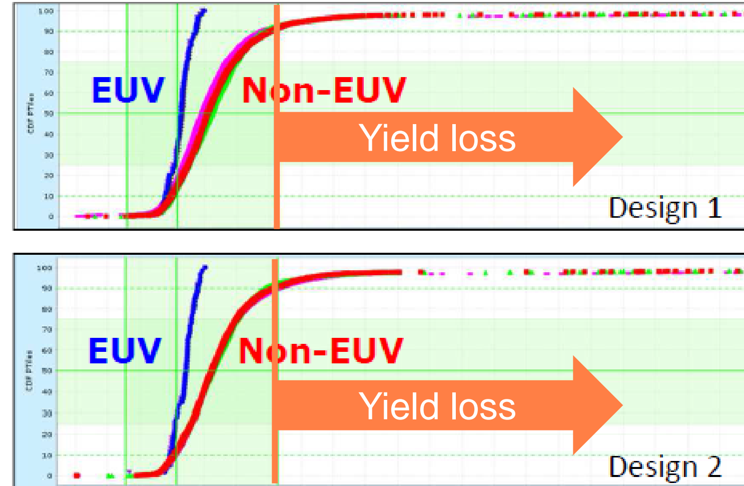
EUV insertion is focusing on the 7nm node

- EUV insertion is currently focusing on the 7nm node
  - *Production 2018, production system shipments 2017*
  - *Insertion is determined by the production readiness of EUV versus the complexity of multiple patterning*
- EUV initially will replace the most difficult multiple patterning layers
  - *Other layers will remain allocated to immersion for the foreseeable future*
- DUV and EUV will be available in parallel for many years to come
  - *ASML remains committed to advancing both technologies to provide the mix that best meets customers' performance and cost requirements*

EUV improves circuit performance, yield, design flexibility

Metal Line Wire Resistance distribution improved with EUV



"In this 10nm node demonstration, EUV wafers with single exposure have tighter distribution compared to optimized multi-patterned 193i lithography"

Source: Jeffrey Shearer et al, IBM, AVS, Nov 2014

7nm chip manufactured with EUV system

IBM: "Industry's first 7nm node test chips with functioning transistors"

- Close to 50 percent area scaling improvements over today's most advanced technology

- Scaling, materials and process improvements could result in *50 percent power/performance increase* for mainframes, servers

Source: IBM press release, 9 July 2015

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The path towards industrialization

Throughput

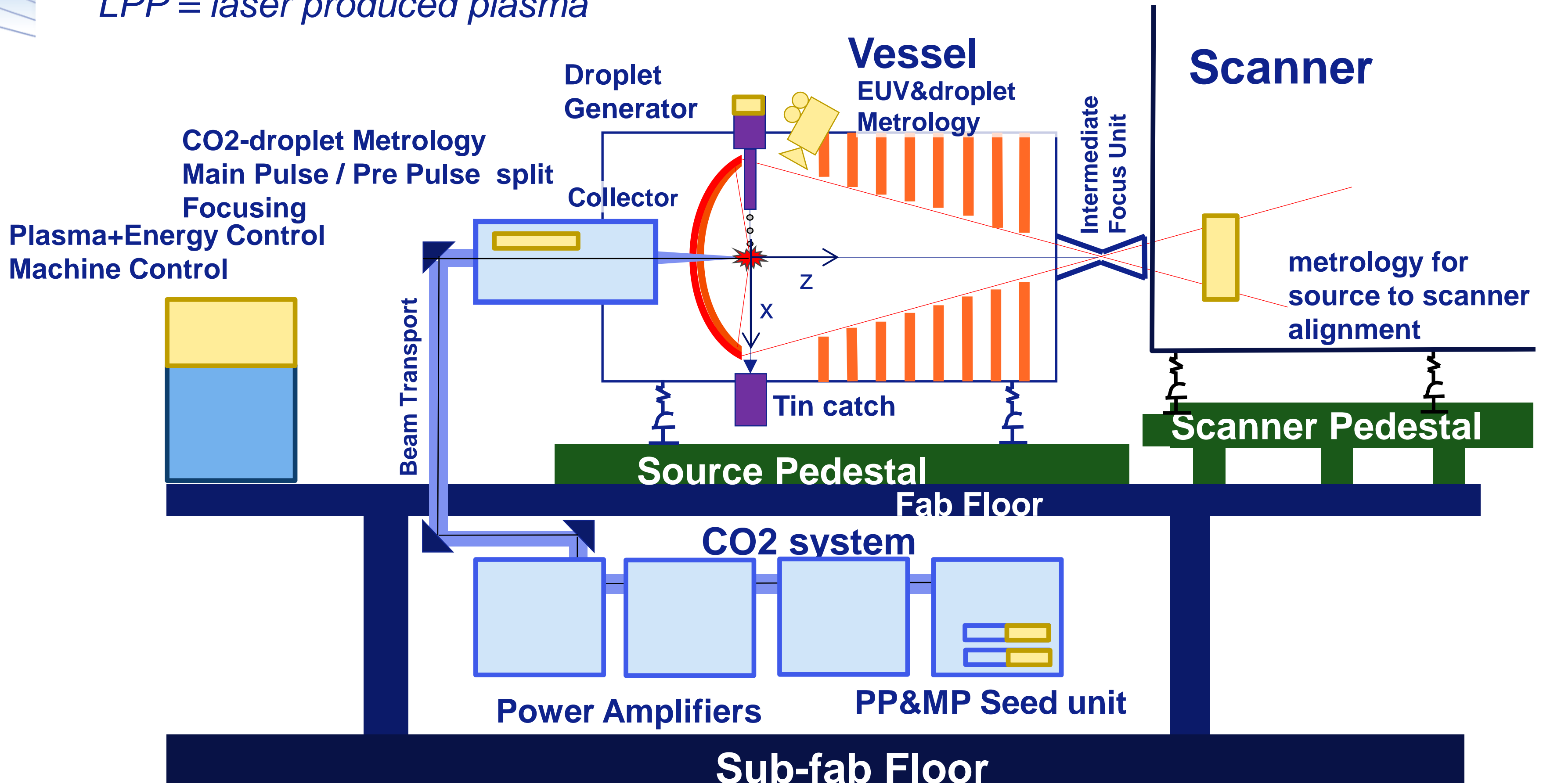
X

Availability

= Productivity

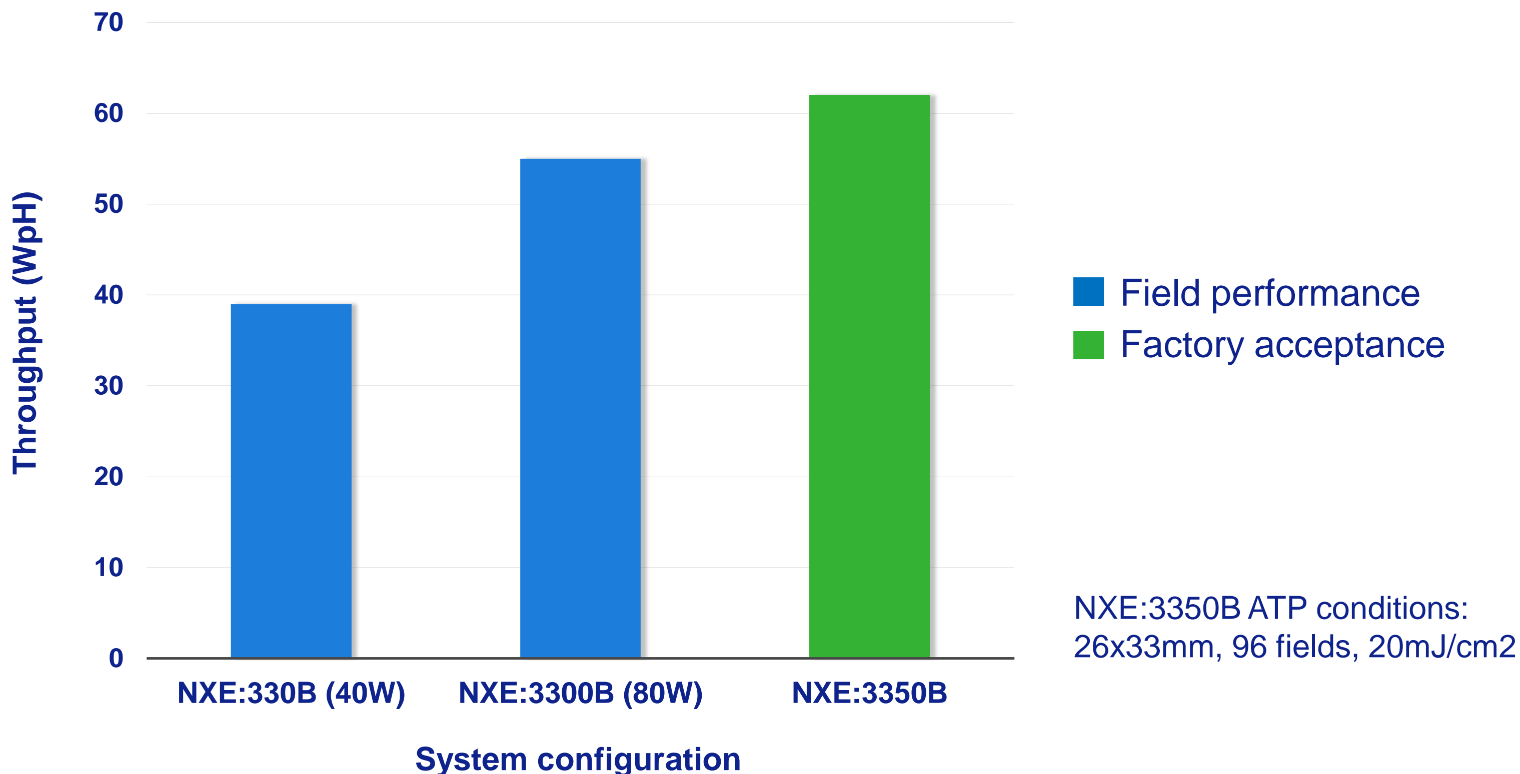
EUV source: LPP system architecture

LPP = laser produced plasma



X = droplet stream direction, z=CO2 light direction, y=orthogonal

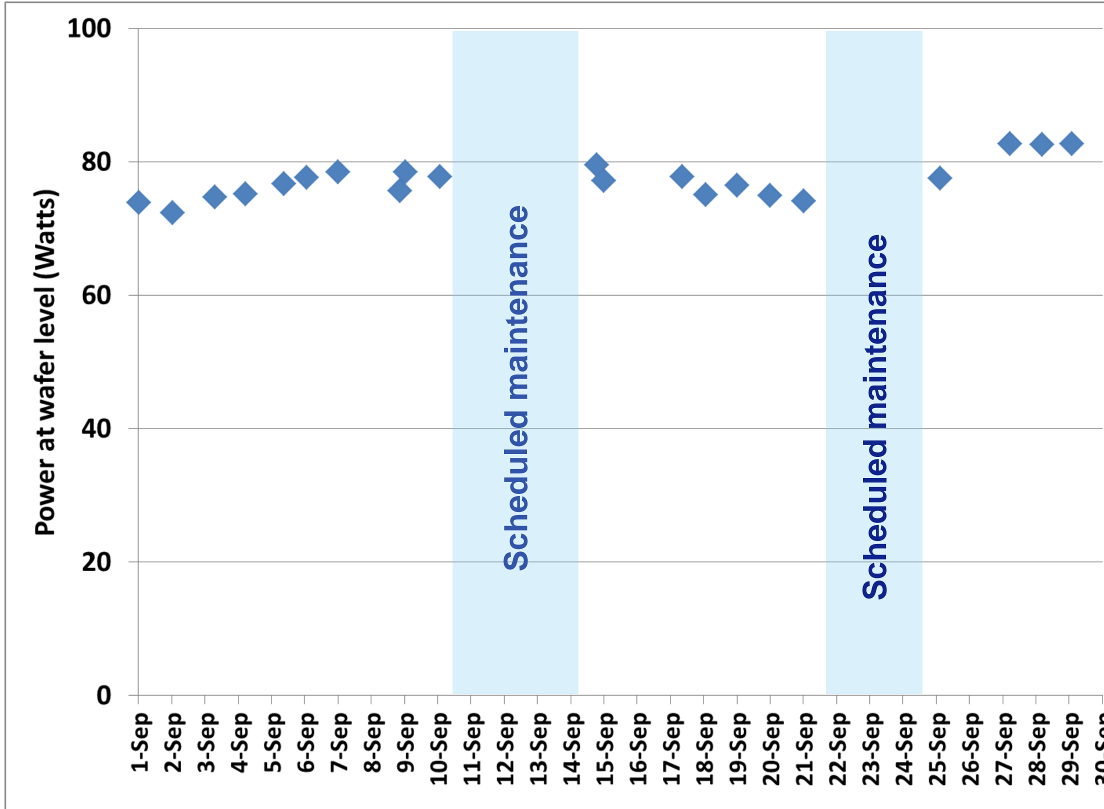
NXE:33X0B throughput performance at >60 wafers per hour



NXE:3350B ATP conditions:
26x33mm, 96 fields, 20mJ/cm2

NXE:3300B: stable 80W performance over one month

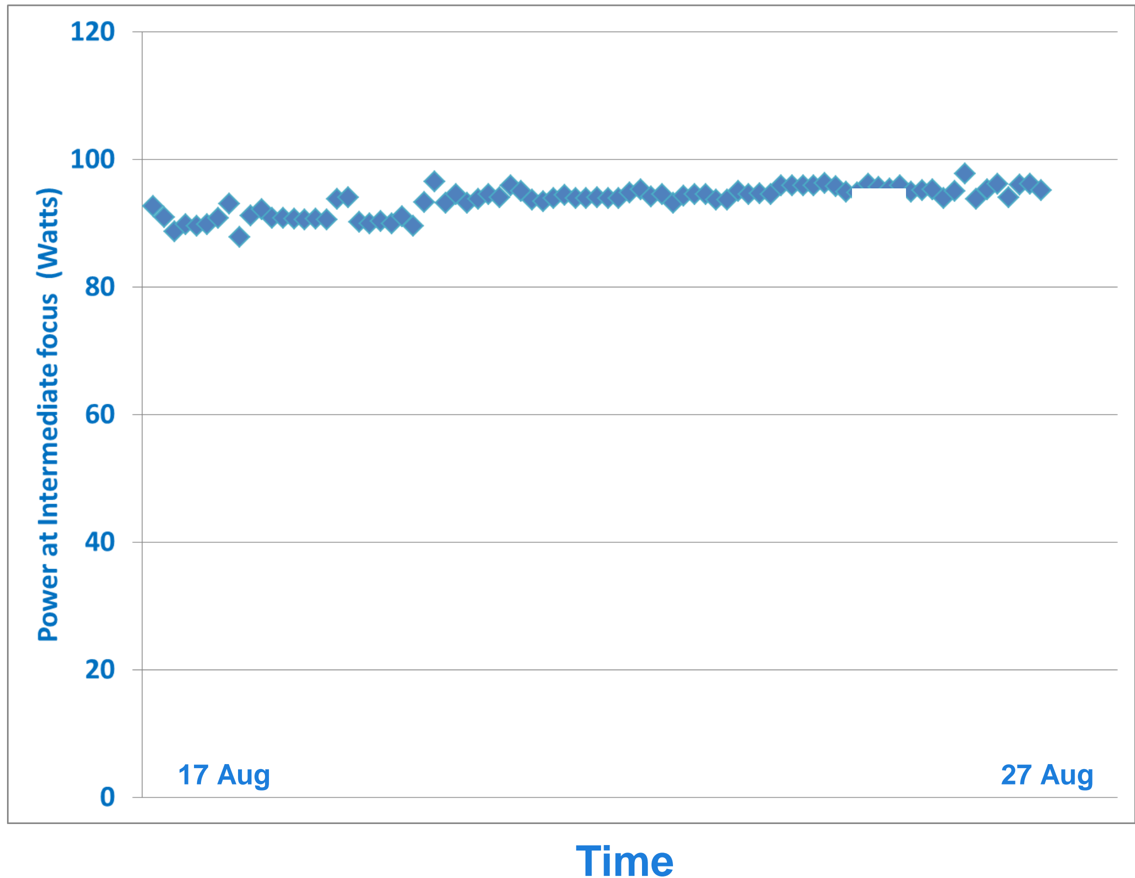
Customer system



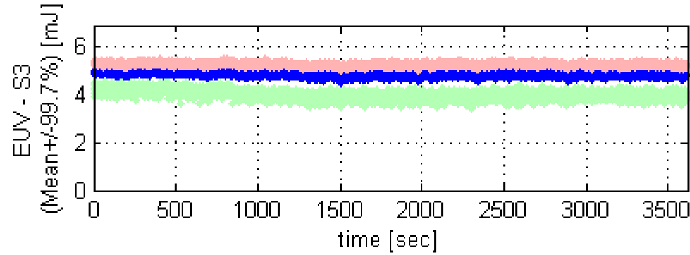
Power at IF(Watts)

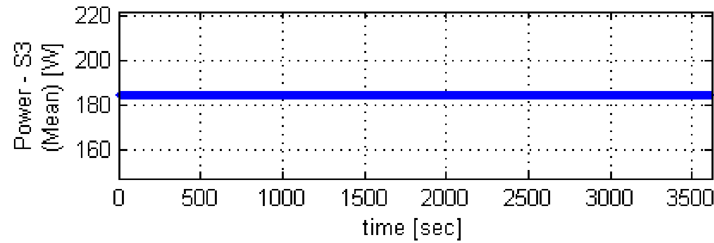
NXE:3350B: stable 95W performance over 10 days

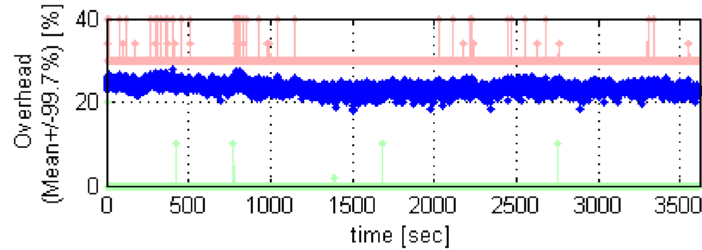
At ASML factory

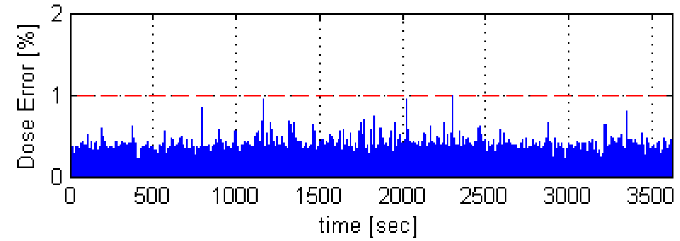


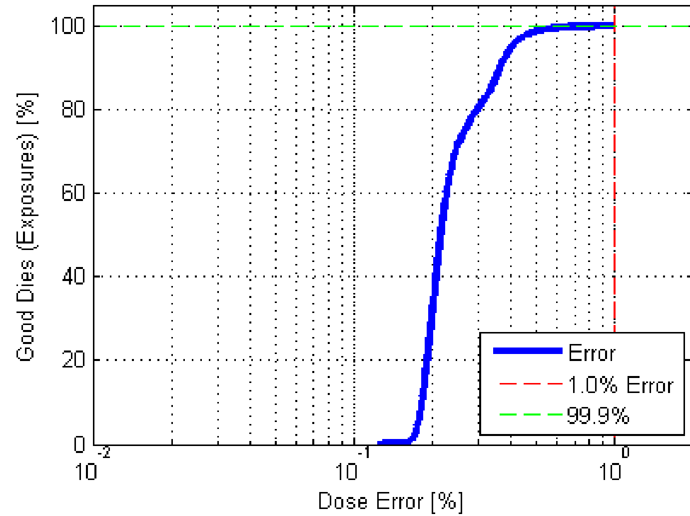
185W: New Record EUV Milestone on Source Stand Alone







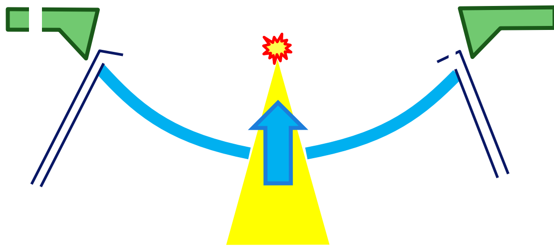




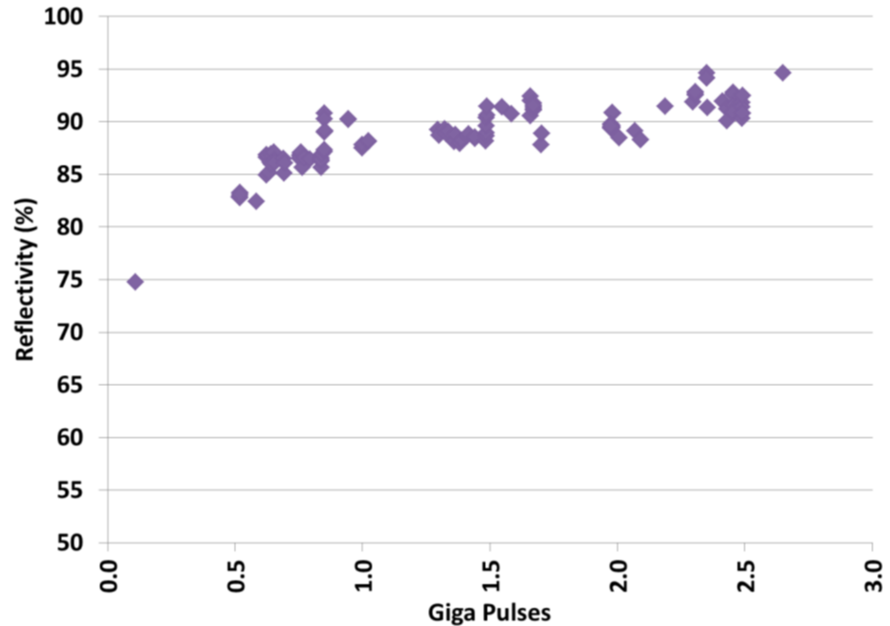
Focus 2015: improving source availability

Field upgrades executed/planned throughout 2015 to support >70% system availability

Collector: temperature optimization for power scaling

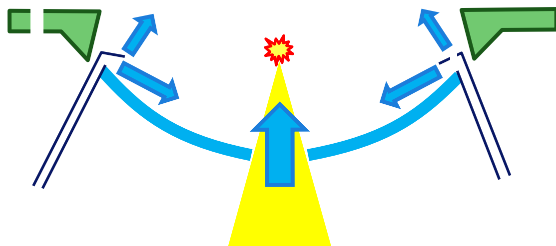


1. Decrease collector temperature to enhance EUV self cleaning effect

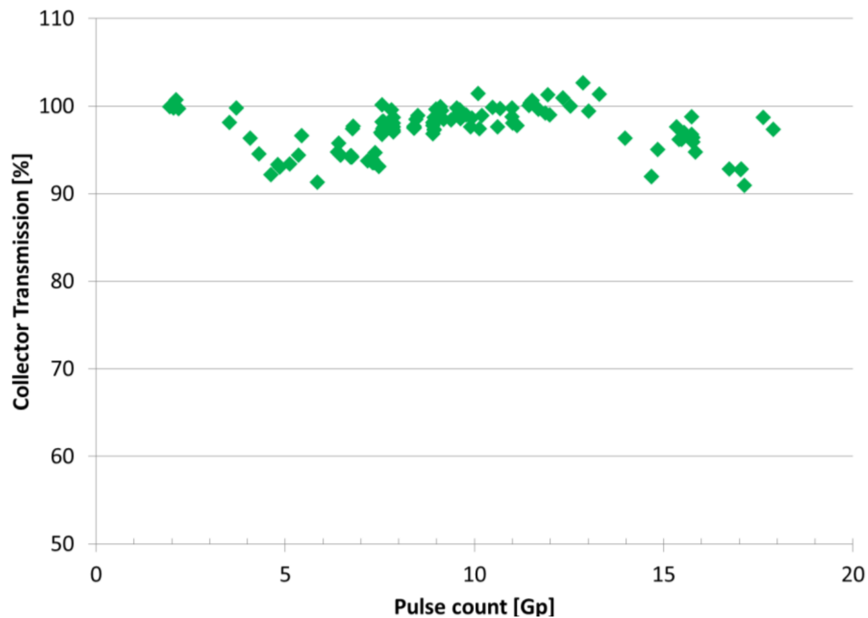


EUV induced etching effect restores collector reflectivity

Collector: flow optimization for power scaling



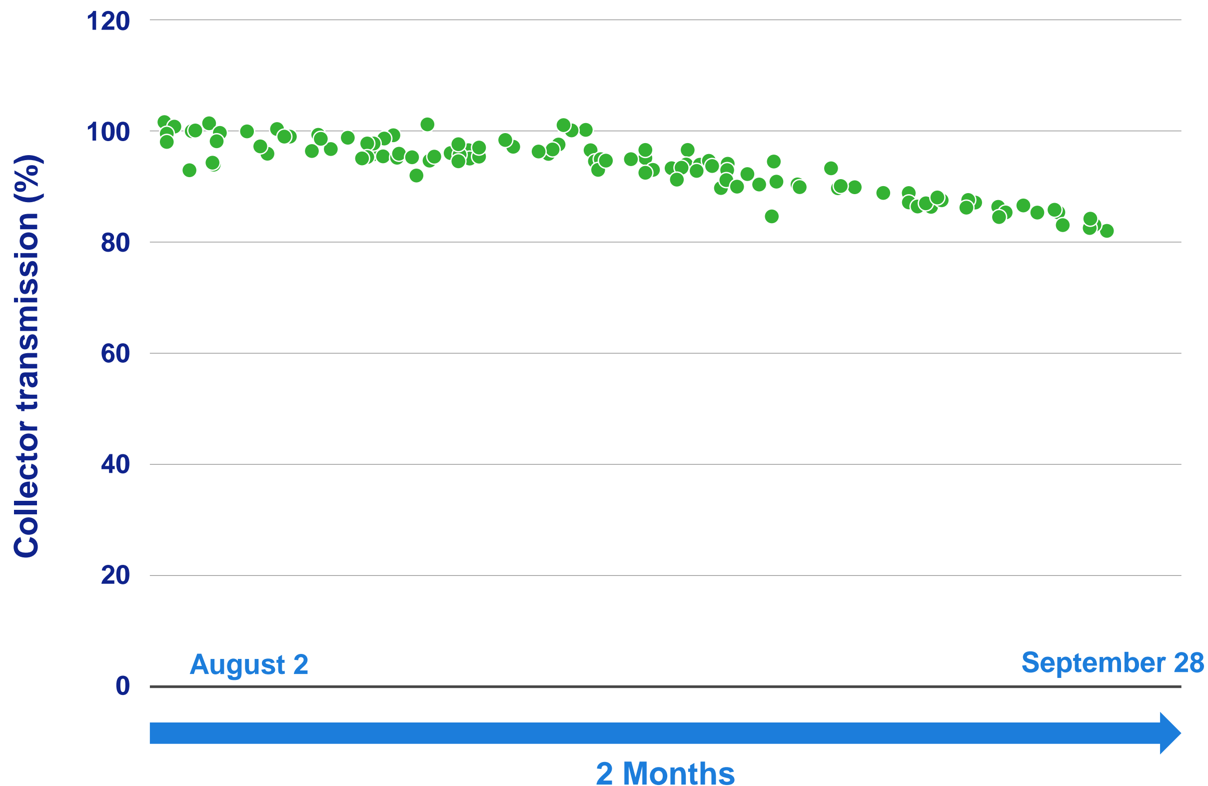
1. Collector protective flows, increase with source power



Test results on NXE:3350B source at 95W: estimated lifetime >6 months

Collector lifetime in 80W configuration towards ~6 months

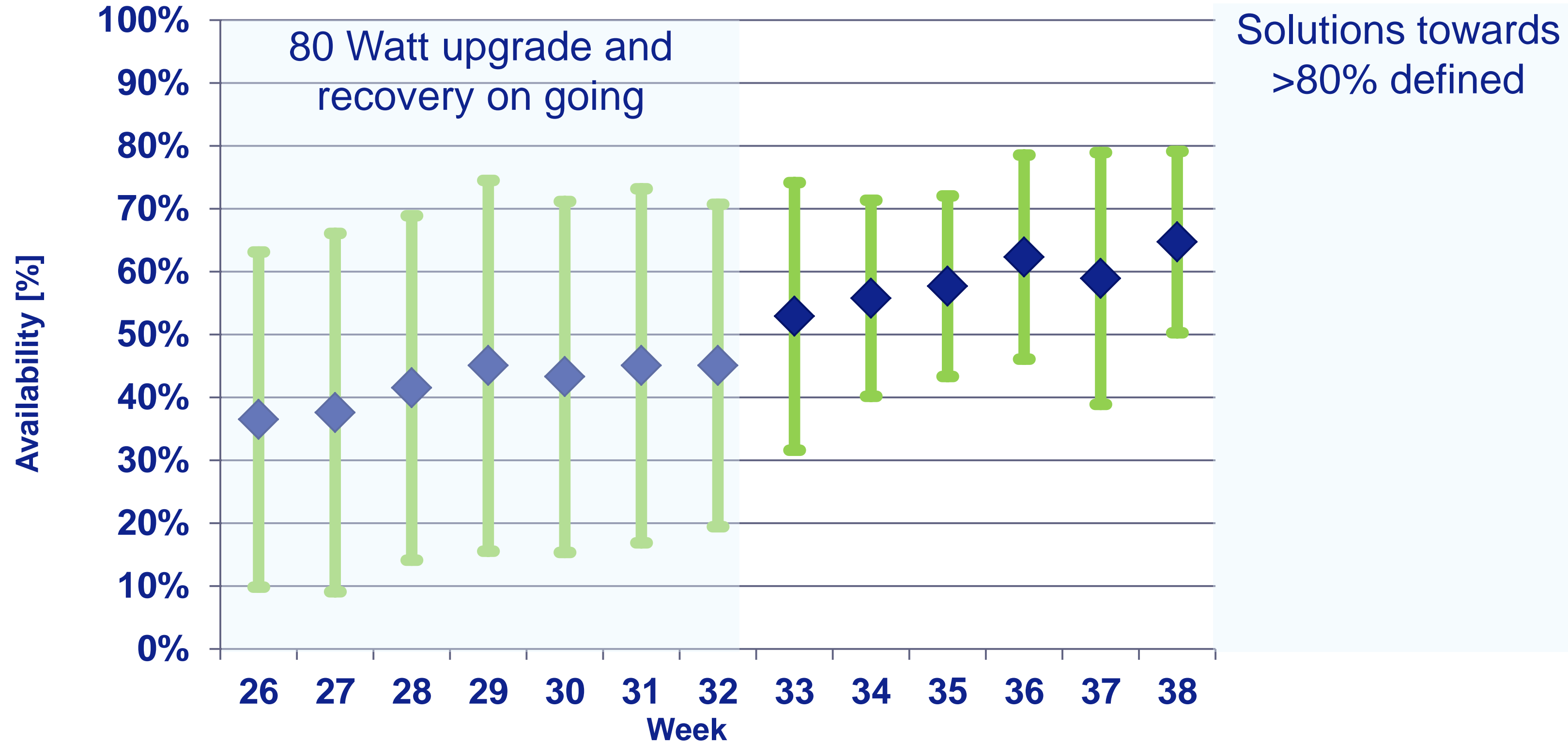
Estimated lifetime



Courtesy of IBM

EUV source availability improving towards 70%

Variability decreasing thanks to upgrades

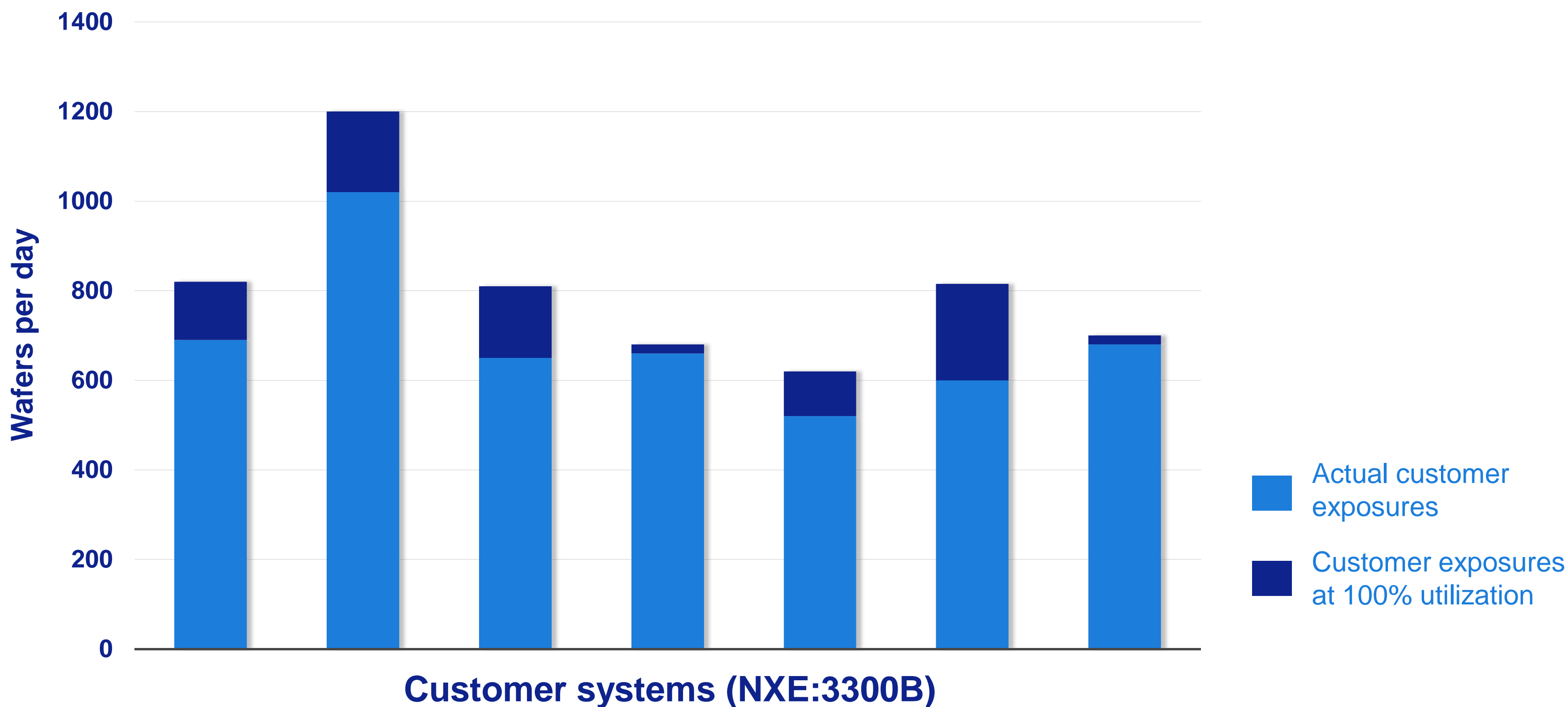


Availability = productive + stand-by + engineering time

Average +/- std. dev. of 5 sources, 4 weeks average

7 field NXE:3300B at 500 wafers per day

1,000 wafers per day capability demonstrated



Maximum number of customer wafer exposures in a 24 hour period

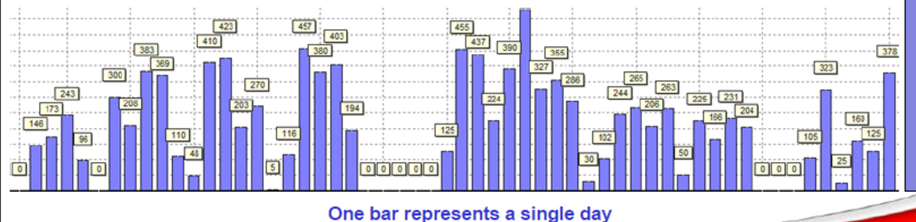
Availability improved from 55% to 70%

Q4 2014 data, as presented by Tony Yen at 2015 SPIE, San Jose

8 weeks of productivity on a NXE3300

- Process Conditions
  - Wafers of various lot sizes and required doses
- 8-week-average WPD: 203 wafers
  - Total wafers processed: 11375
- Average Tool Availability: 55%
- Data shown are prior to source upgrade to 80W

After 80W upgrade: 1022



9

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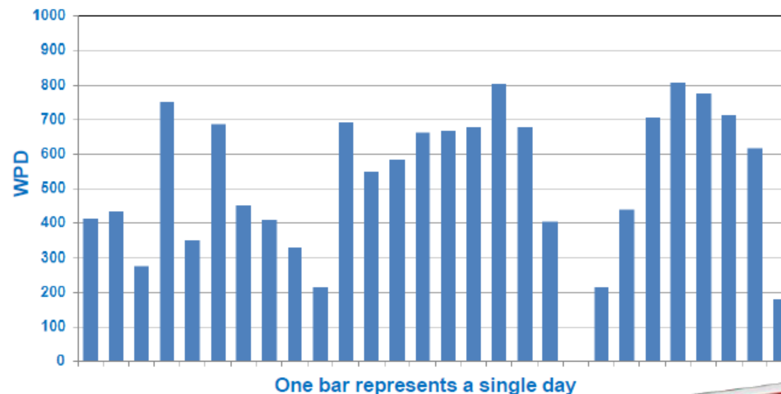
Open Innovation Platform®

Recent Productivity Improvement on NXE3300

- Process conditions
  - Wafers of various layers/lot sizes with required dose, CD, and overlay
- 4-week-averaged WPD: 518 wafers
  - Total wafers processed: 15040
- 4-week-averaged tool availability: 70.2 %



10

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EUV source supports NXE Industrialization Roadmap

Timing	Source power [W]	Throughput [Wafers/hr]	Source availability [%]	Productivity [Wafers/day]
Today	80	>55	>70%	>500
2015	125	>75	>80%	>1000
2016	250	>125	>90%	>1500

Done

Capability demonstrated

On track

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- EUV Insertion
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- ***Imaging & Overlay***
- Defectivity & Pellicle
- High NA
- Summary

Imaging, overlay, defectivity at a glance

Status September 2015

Imaging

- NXE:3300B imaging evaluation for 10 nm Logic: Dense and isolated lines, tip-to-tip CDU meets requirements
- Imaging evaluation for <15nm DRAM: Dense contact holes CDU meets requirements
- NXE:3350B imaging and overlay results for 7nm Logic are good

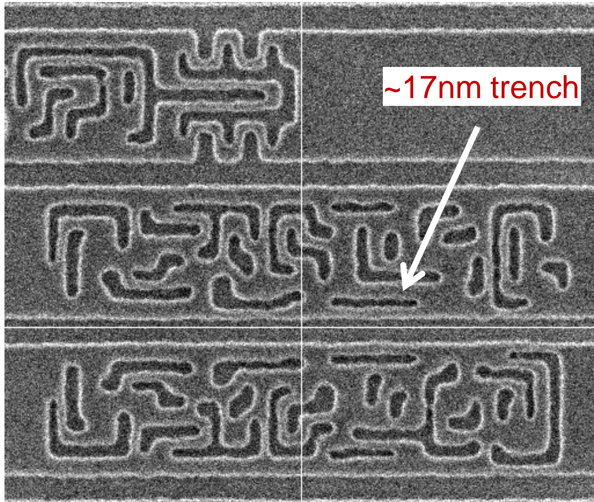
Overlay

- NXE:3300B: overlay in spec (tested at ~90 Watts source power)
- Good, stable mix-and-match overlay performance at customer site

Defectivity

- Front-side reticle defectivity: 10x reduction/year realized
- Full-size pellicle prototype available, no impact on imaging
- Removable pellicle concept enables mask pattern inspection with existing equipment

NXE:3300B meets 7 nm Logic node performance requirements

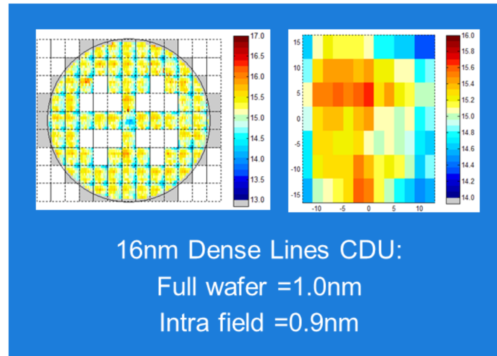


Routed 2D semi-gridded Metal 1

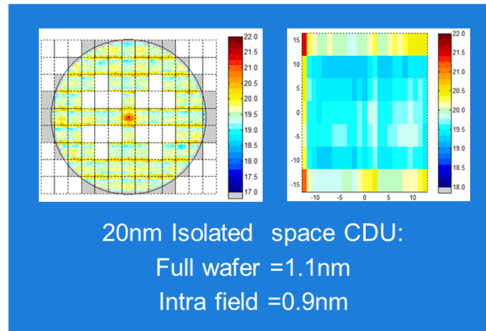
36x38nm (PV x PH)

This example would require 4 exposures with 193 immersion – or one with 0.33NA EUVL

Conditions: NXE:3300B, annular illumination, 60nm resist, 40mJ/cm2 dose

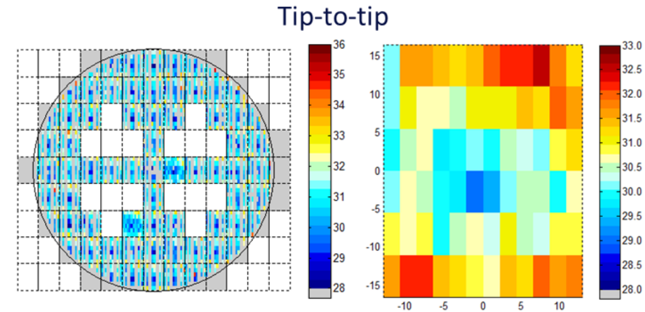


16nm Dense Lines CDU:
Full wafer =1.0nm
Intra field =0.9nm

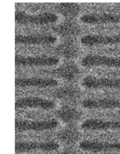


20nm Isolated space CDU:
Full wafer =1.1nm
Intra field =0.9nm

Tip-to-tip



16nm dense L/S with 12nm gap (1x) @ 40mJ/cm²
Including reticle and shadowing fingerprint



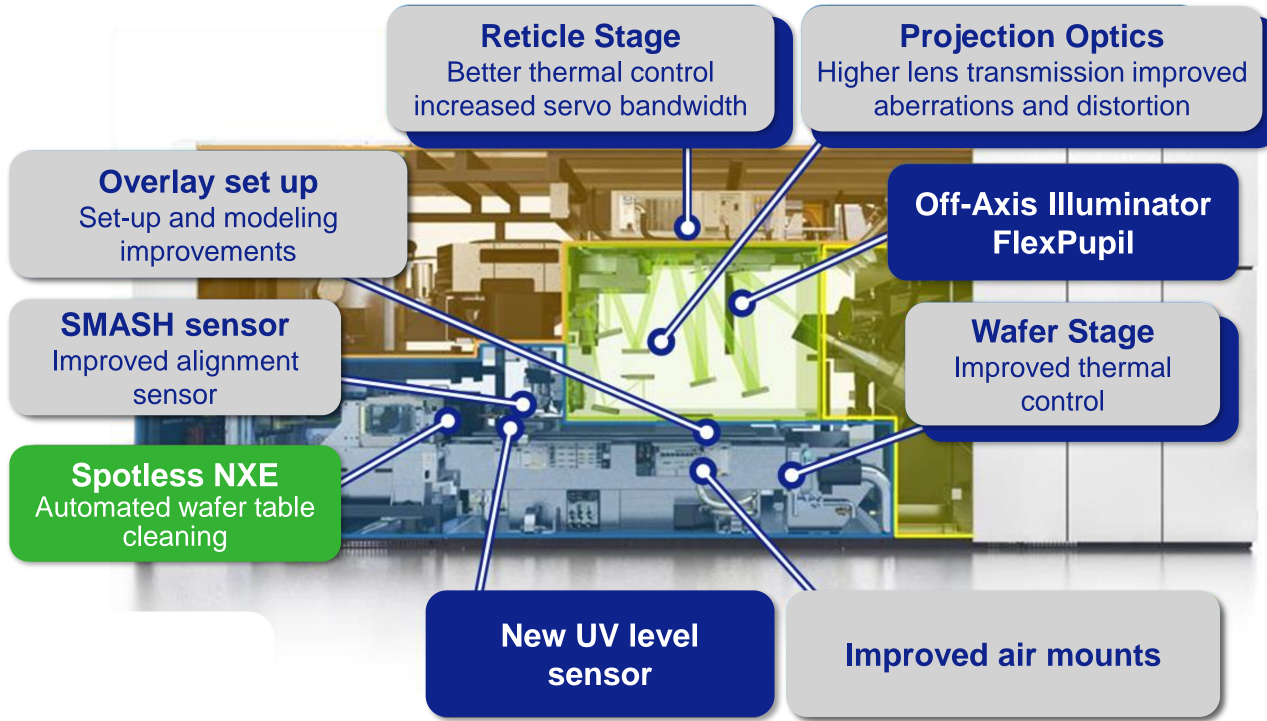
CDU	CD	FW CDU	IF CDU
V T2T gap	30.9nm	2.9nm	2.2nm
H trench	18.4nm	1.1nm	1.0nm

Experimental conditions

NA=0.33, sigma inner/outer=0.2/0.9 Dipole-90-Y

NXE:3350B Supports 7nm logic insertion

by strongly improved overlay and resolution



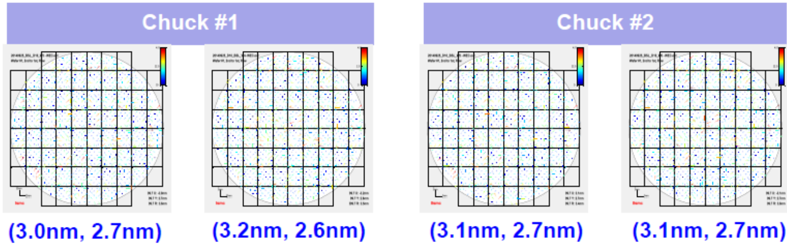
Resolution	16nm
Full wafer CDU	≤ 1.3nm
DCO	≤ 1.5nm
MMO	≤ 2.5nm
Focus control	≤ 70nm
Productivity	≥ 125 WPH

Overlay
Imaging/Focus
Productivity

Stable mix-and-match <3.2 nm overlay performance

At customer site between immersion and EUV (NXE:3300B)

Mix-and-match overlay performance



Measurement on 68 fields; 25 points per field

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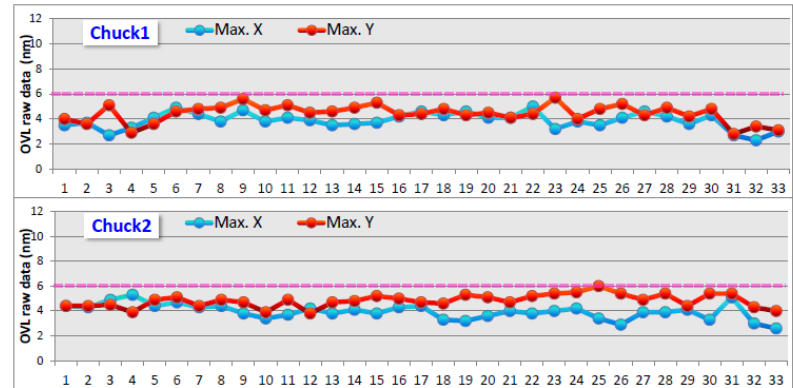
Mix-and-match overlay performance



EUV-to-immersion mix-and-match overlay on multiple lots with >200 points per wafer

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Immersion 4 masks vs EUVL 1 mask

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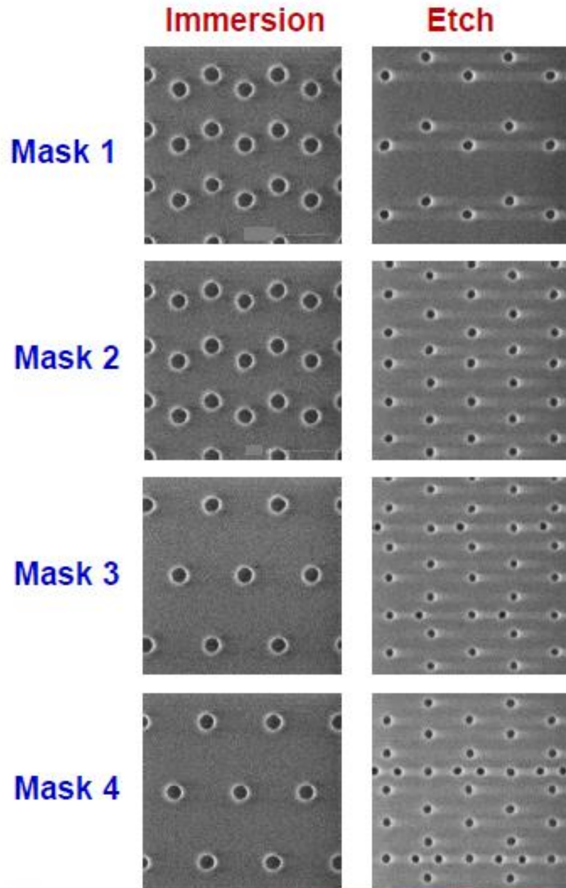
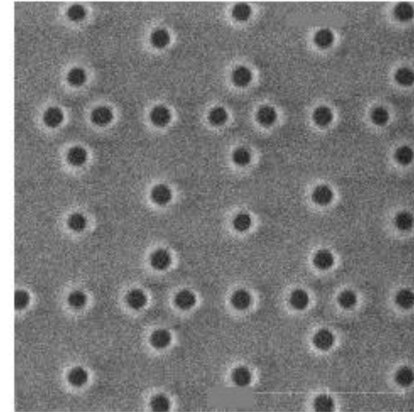


EUV single patterning



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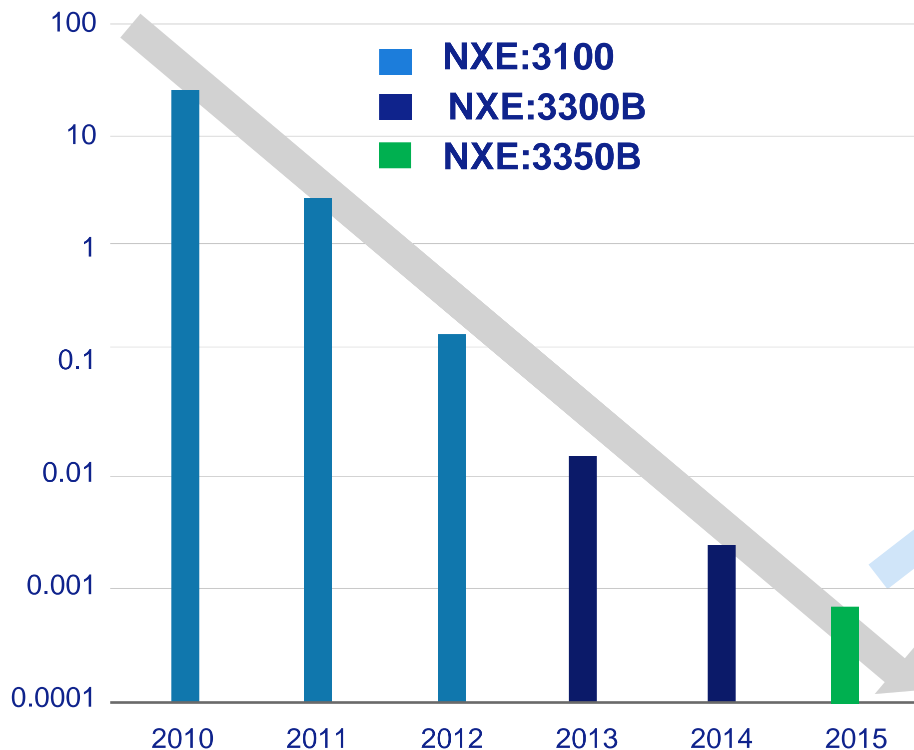
Front-side reticle defectivity: 10x reduction/year realized



Test	# Cycles	# Added Particles	PRP Value
A	228	0	< 0.004
B	140	0	< 0.007
C	450	0	< 0.002
D	222	1	0.0045
E	133	0	< 0.007
Cumulative	**1173**	**1**	**0.0008**

EUV pellicle development progress

ASML

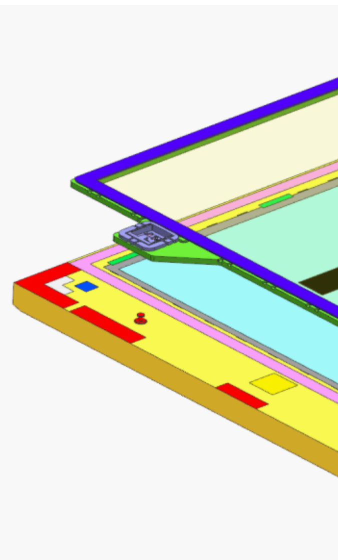
	Oct'12	May'13	Nov'13	Feb'14	Jun'14	Dec'14	Feb'15
Film testing	11mm x 11mm	50mm x 50mm	Half size proto	Full size proto (attached to wafer)	Full size proto		Removable
Machine testing		11mm x 11mm		50mm x 50mm	Half size proto	Full size proto	Removable
Imaging testing		11mm x 11mm			Half size proto	Full size proto	

Imaging achieved in cooperation between ASML and NXE:3100 customers

Repeated same imaging testing on full size proto pellicle on NXE:3100

NXE Pellicle concept: particle free mounting/ de-mounting

Allowing multiple inspection schemes



Fully integrated
EUV pellicle

Key features

t-free solution

side from fall-on defects

combination and mounting
t particle generation

ppression towards pattern area

KE scanner

les compatible

ronment compatible

quirements

stortion-free mounting

ard EUV mask flow

y type of pattern mask
-beam, and actinic; both at

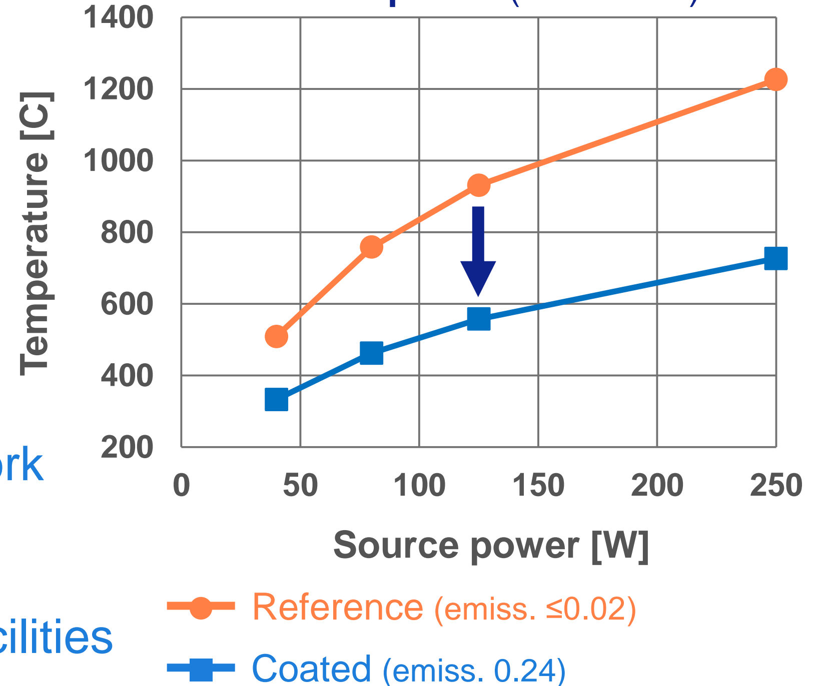
el cycle (repel=repeat pellicle)

Pellicle durability proven at least to 125 W
using coated pellicles, to be integrated at ASML work center

Heat load test* results

Film stack	Eq. source power	Sample survivability
Uncoated	40 W	9/9
Uncoated	125 W	3/5
Coated	125 W	32/32

ASML pellicle integration work center at our Veldhoven production facilities



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Summary

- *Progress in EUV in the past year in all key area's*
  - Productivity >10x, Consistency 2x. *Significantly more progress is needed*
  - EUV Infrastructure (resist, mask, and inspection) improved
  - Litho-performance compatible with 7 nm Node use
- EUV moves from "**If**" to "**When**" it will be introduced in production.
- Expectation: (a) exercise of EUV at the 10 nm Logic in order to qualify EUV and shorten cycles of learning. (b) high volume production of EUV at the 7 nm Logic node. (DRAM will follow Logic closely).
- EUV is a new extendable litho-technology allowing customers to continue cost effective shrink and up to 5-10x simpler and faster manufacturing cycles for at least the next 10 years

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