EUV Lithography: Present and Future

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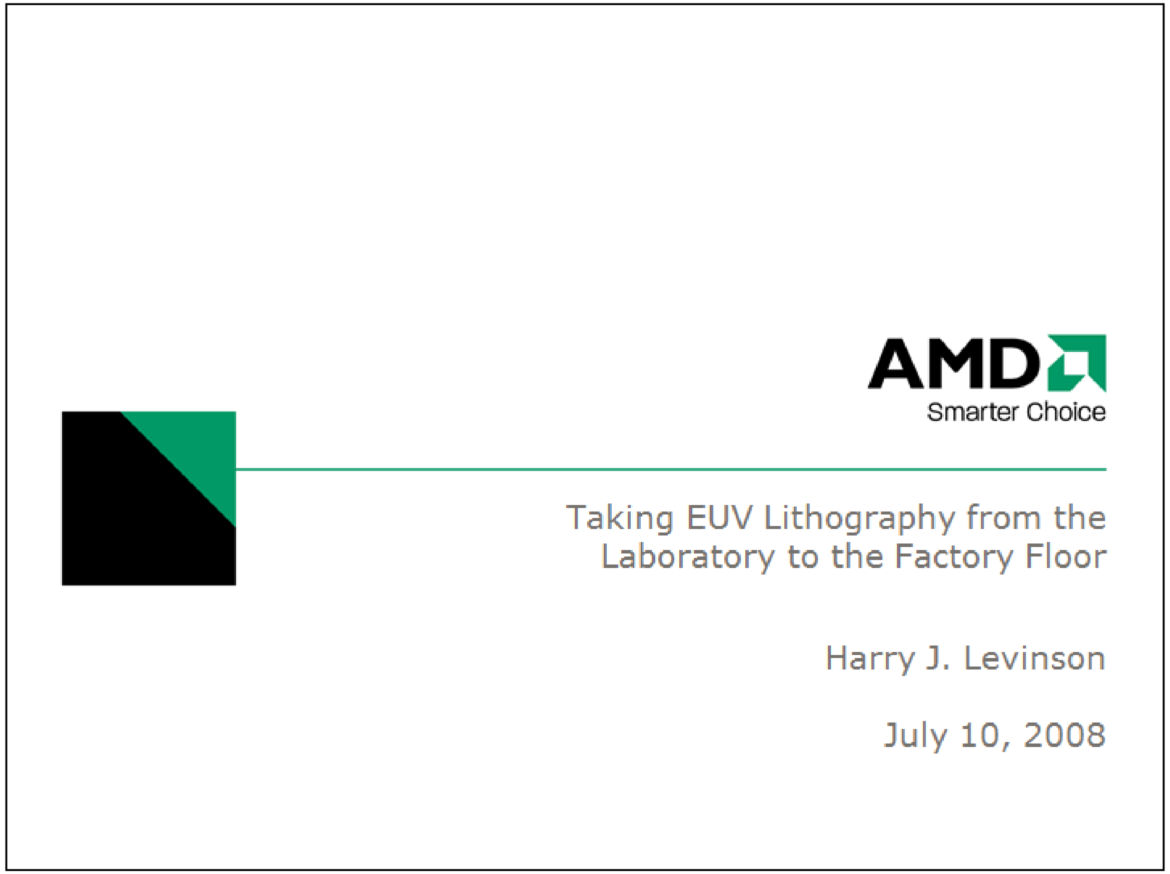
June 2016

GLOBALFOUNDRIES®

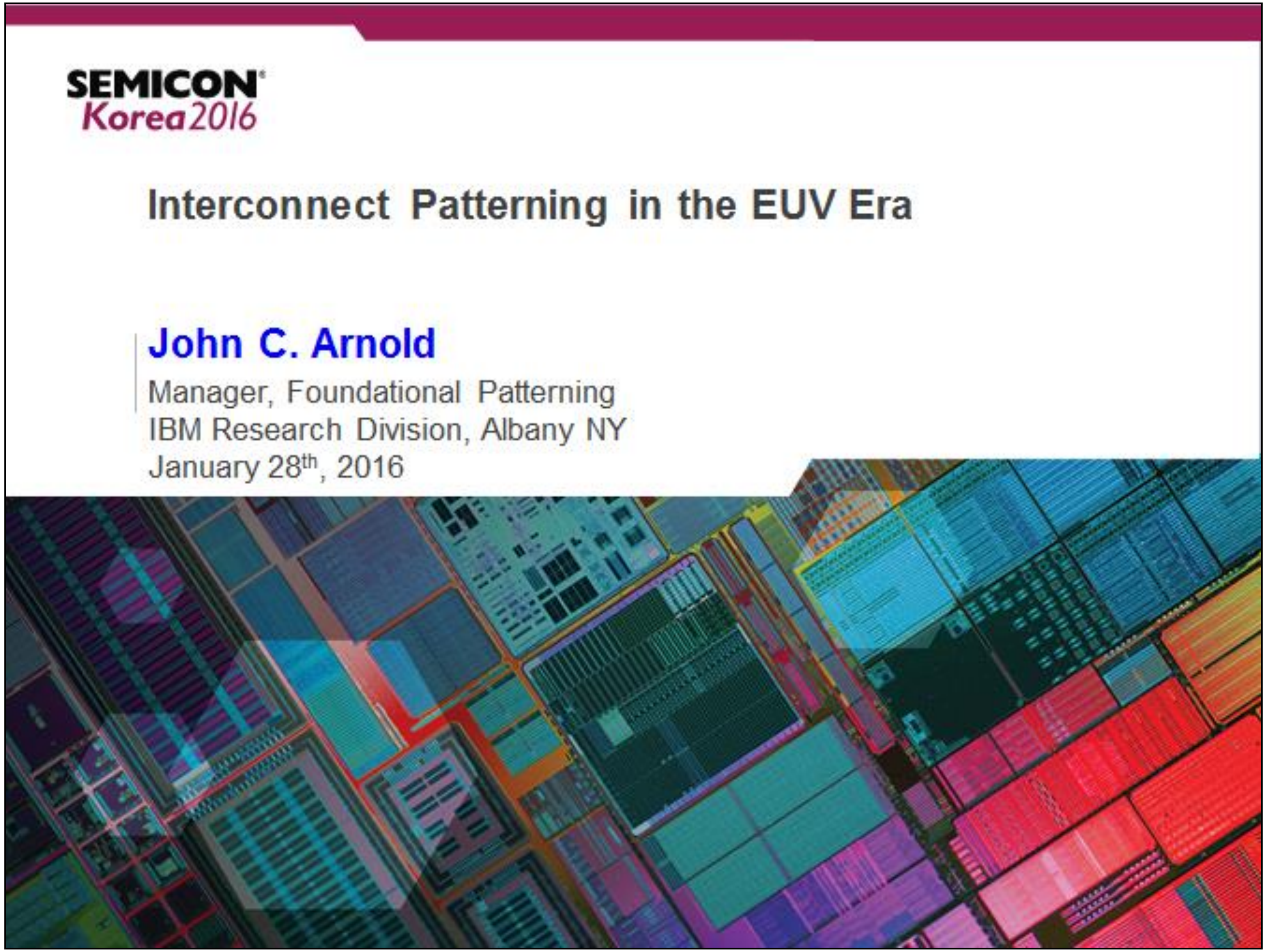
Presentations in Korea on EUV lithography

Semicon Korea February, 2014

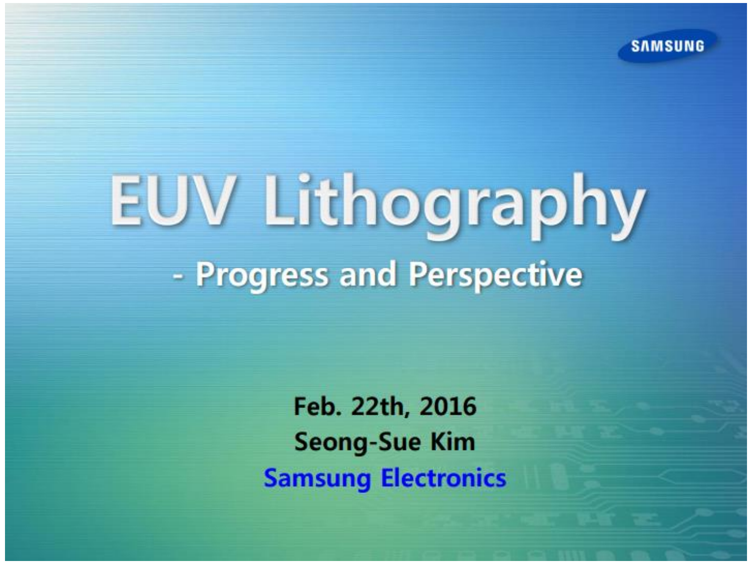
Optical Society of Korea 2008

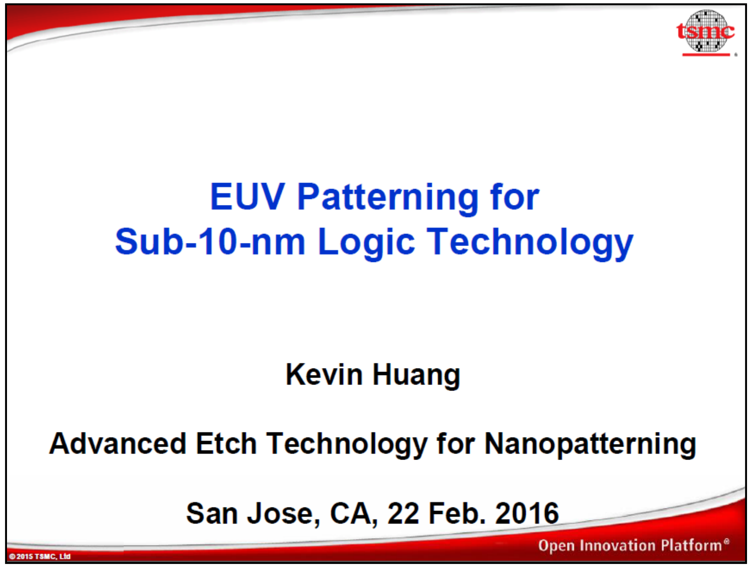


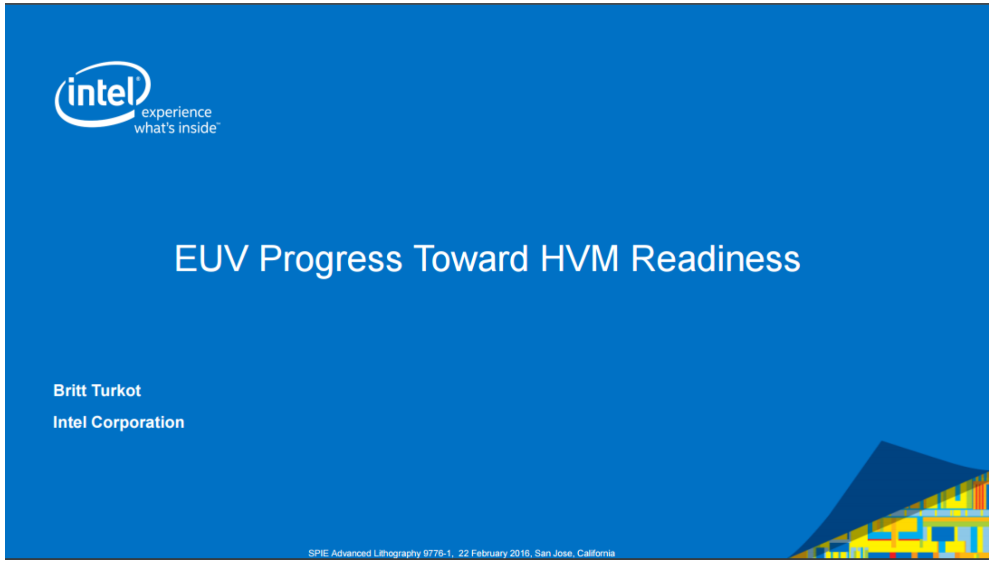
Presentation in Korea on EUV lithography – this year



Presentations on EUV lithography, SPIE Advanced Lithography 2016





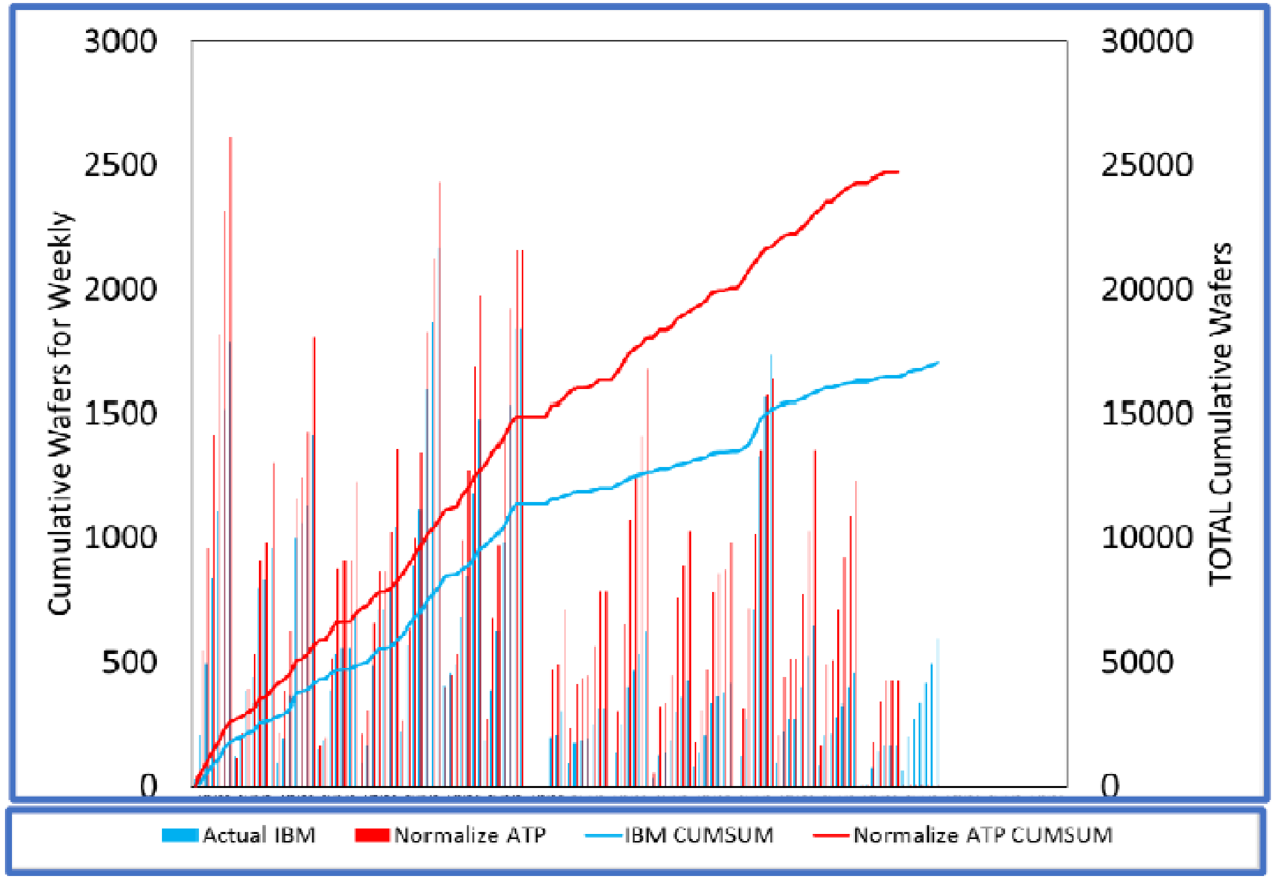


What changed?

EUV sources

	Availability	Power
January, 2014	<< 50%	<< 60 W
Today	~75%	60-80 W

13 week cluster productivity (IBM)



- ~200 wafers per day
- Difference between being able to make progress and not.

What can be done with 200 exposures/day/tool?

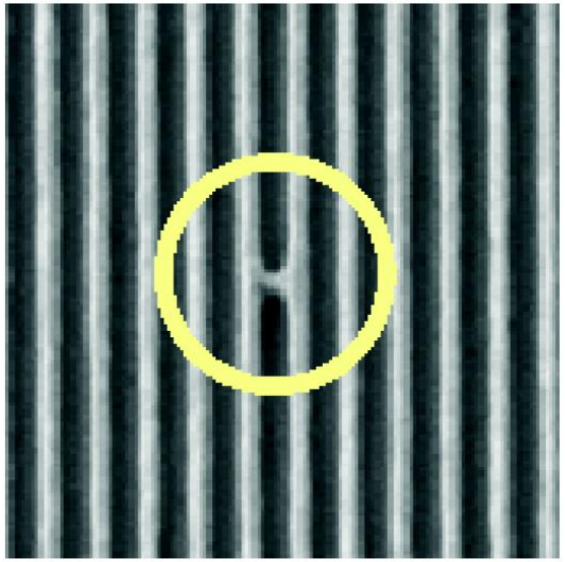
- A pilot line with two exposure tools, each capable of 200 exposures/day:
  - Can sustain 50 wafer starts per day of integrated lots with 6 EUV levels.
  - Can support additional assessments of EUV lithography.
    - Resist testing.
    - Wafer prints of EUV masks.
    - Exposure tool testing.

- While not HVM-level, this is also beyond the laboratory.

Learning during development is different than during research

- Yield
- Mask contamination
- Equipment reliability
- Process control
  - Overlay
  - Critical dimension uniformity (CDU)

Example: Defect reduction specific to compatibility of resists and filter materials



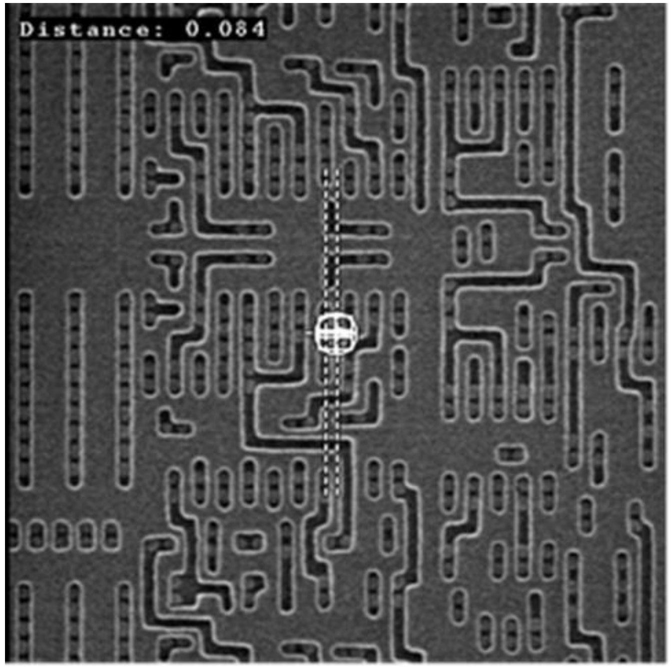
"Defect reduction by using point-of-use filtration in a new coater/developer."

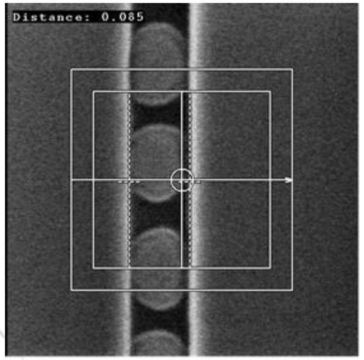
Toru Umeda, Shuichi Tsuzuki, and Toru Numaguchi,

SPIE Advanced Lithography, pp. 72734B-72734B (2009)

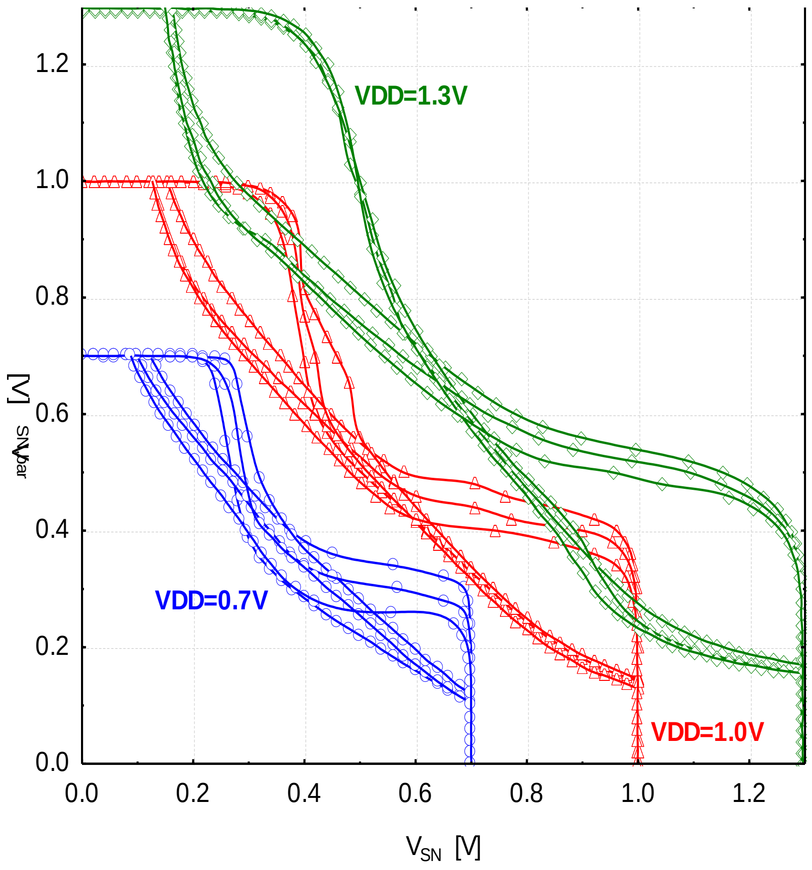
	1	2	3	4
Membrane material	Nylon 6,6	Nylon 6,6	HDPE	HDPE
Filter rating	10 nm	20 nm	10 nm	30 nm
Polarity	Polar	Polar	Non-polar	Non-polar
Product name	PhotoKleen™ EZD-2	PhotoKleen EZD-2	PhotoKleen EZD-2	PhotoKleen EZD-2
Part number	PHD11AN01EH11	PHD11ANMEH11	PHD11UG001EH11	PHD11UG003EH11

Early device demonstration with EUV lithography





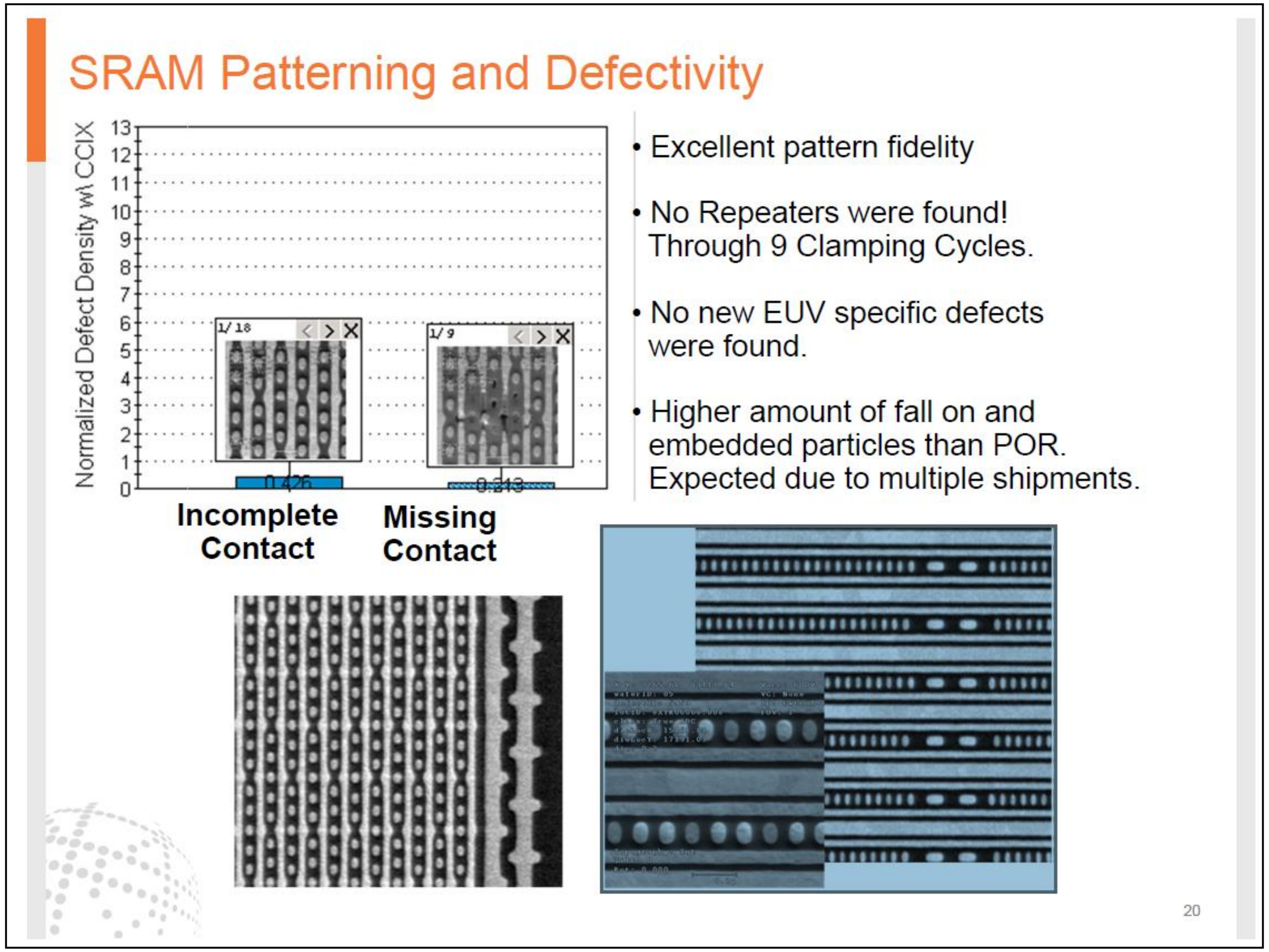
SRAM Butterfly Curves



LaFontaine, et al., “The use of EUV lithography to produce demonstration devices” SPIE Emerging Lithographic Technologies (2008)

Application to devices

- With improved reliability, multiple tools in the field, and motivation, EUV lithography is being used to pattern complex circuits.

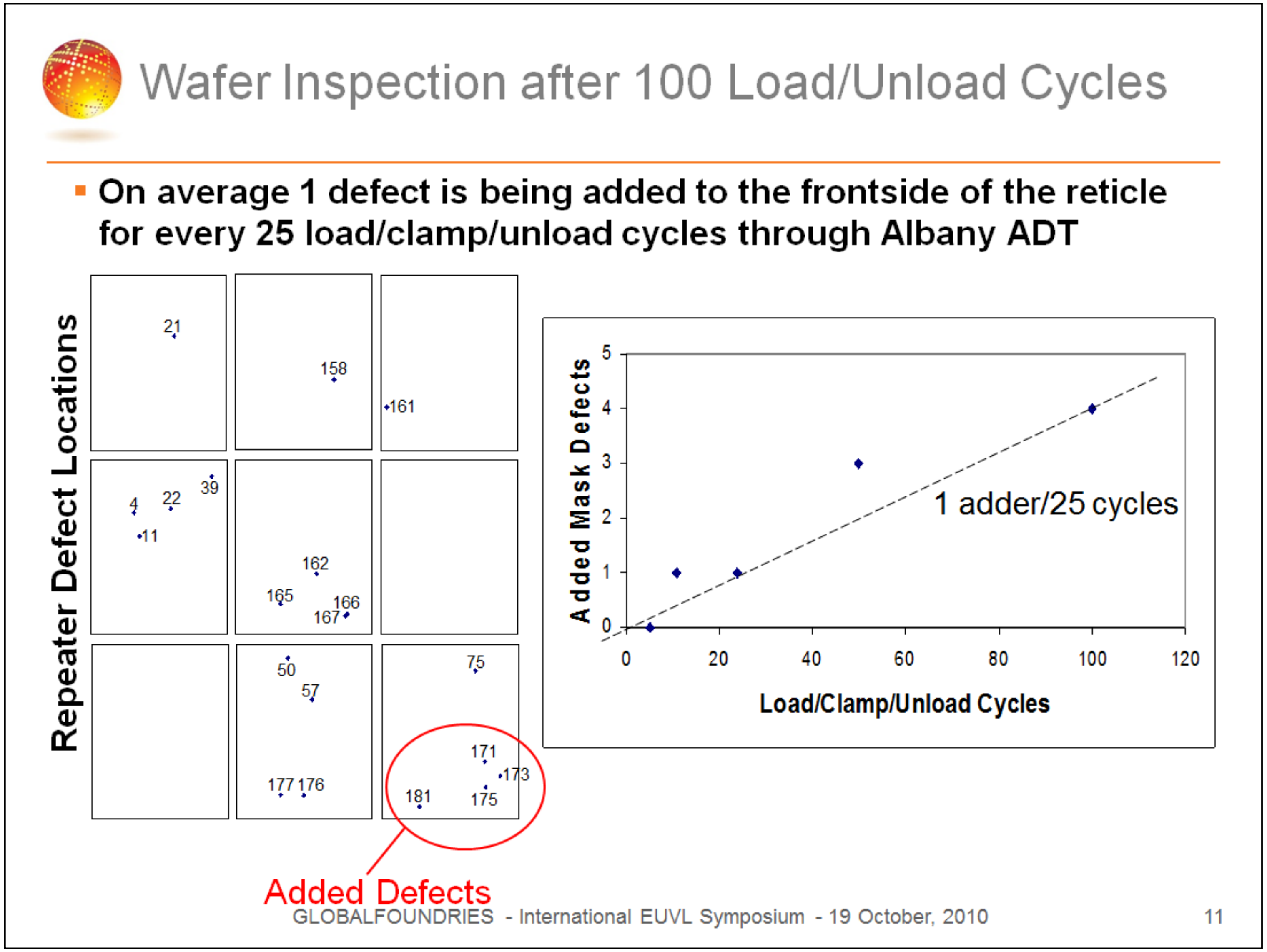


"Integration of an EUV Metal Layer: A 20/14nm Demo,"

Craig Higgins, et al.,

SPIE Advanced Lithography Symposium (2014)

Reticle contamination

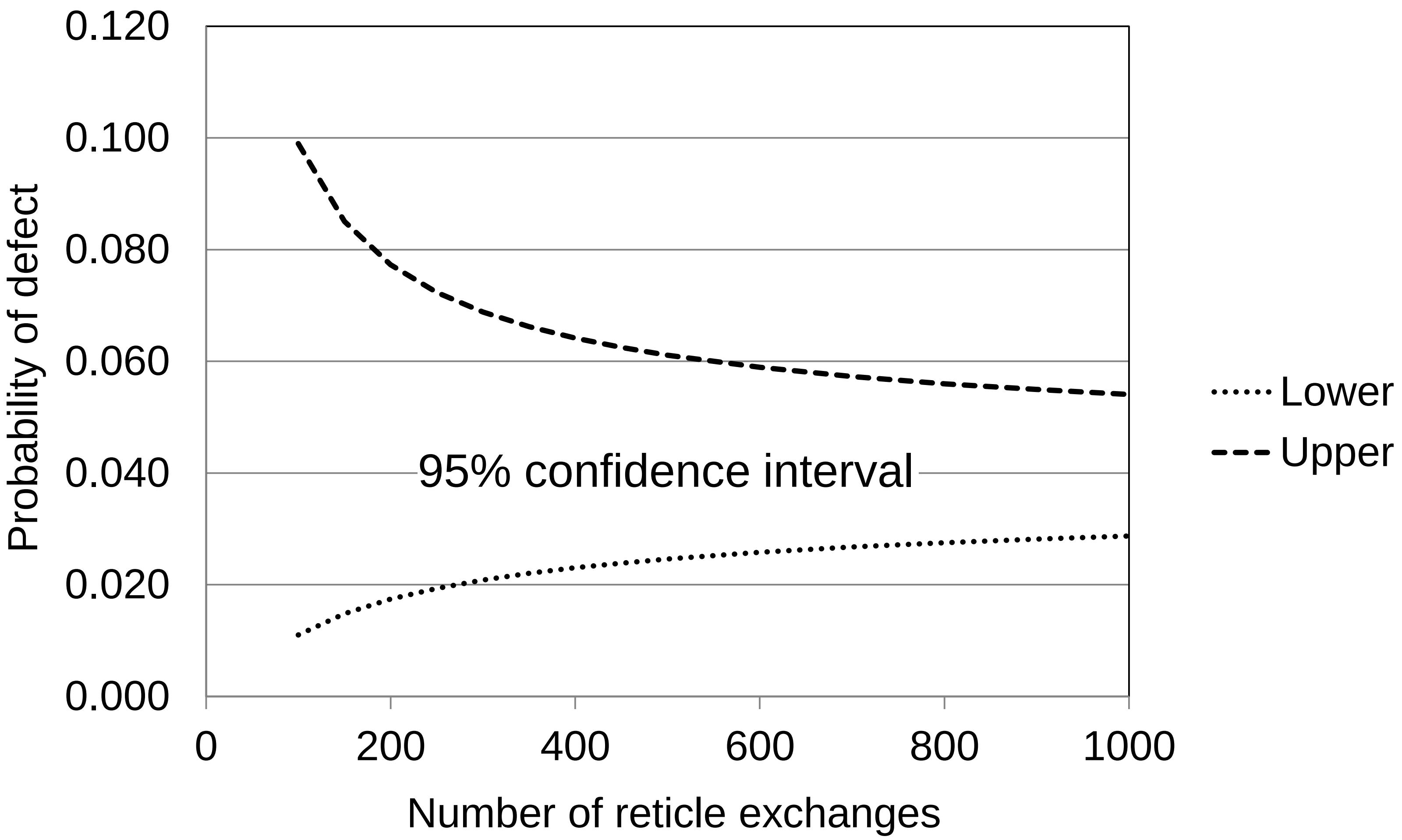


"Impact of frequent particle removal on EUV mask lifetime,"

Obert Wood, et al,

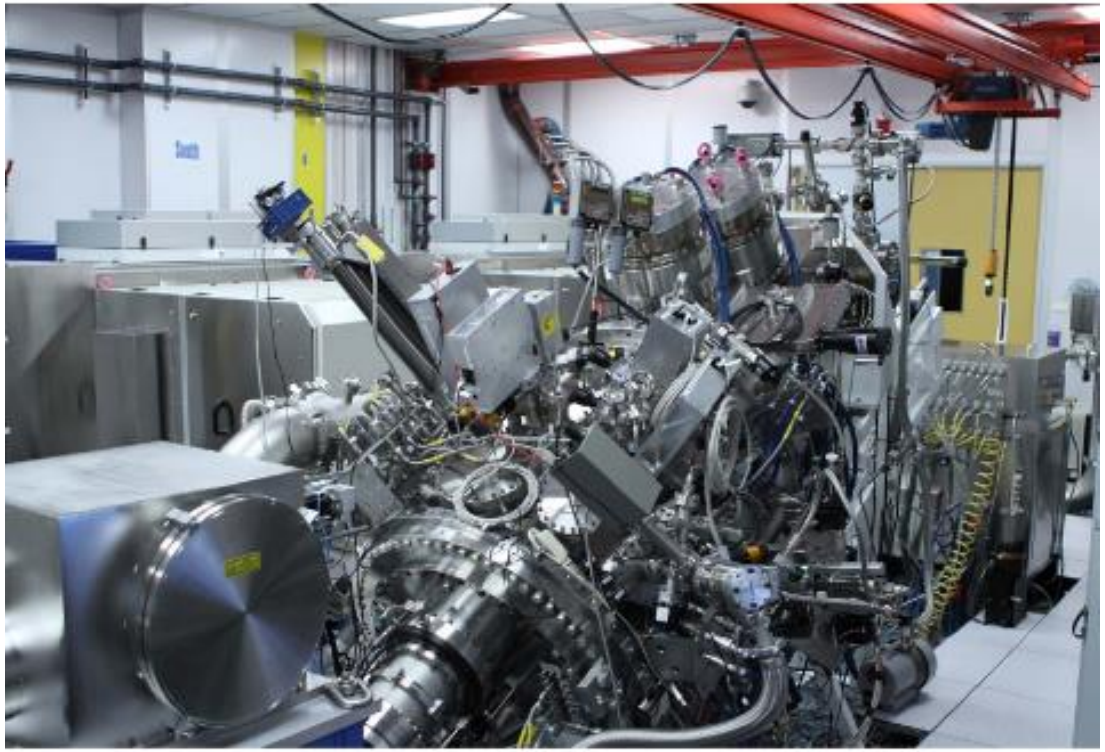
EUV Lithography Symposium, 2010

Reticle contamination



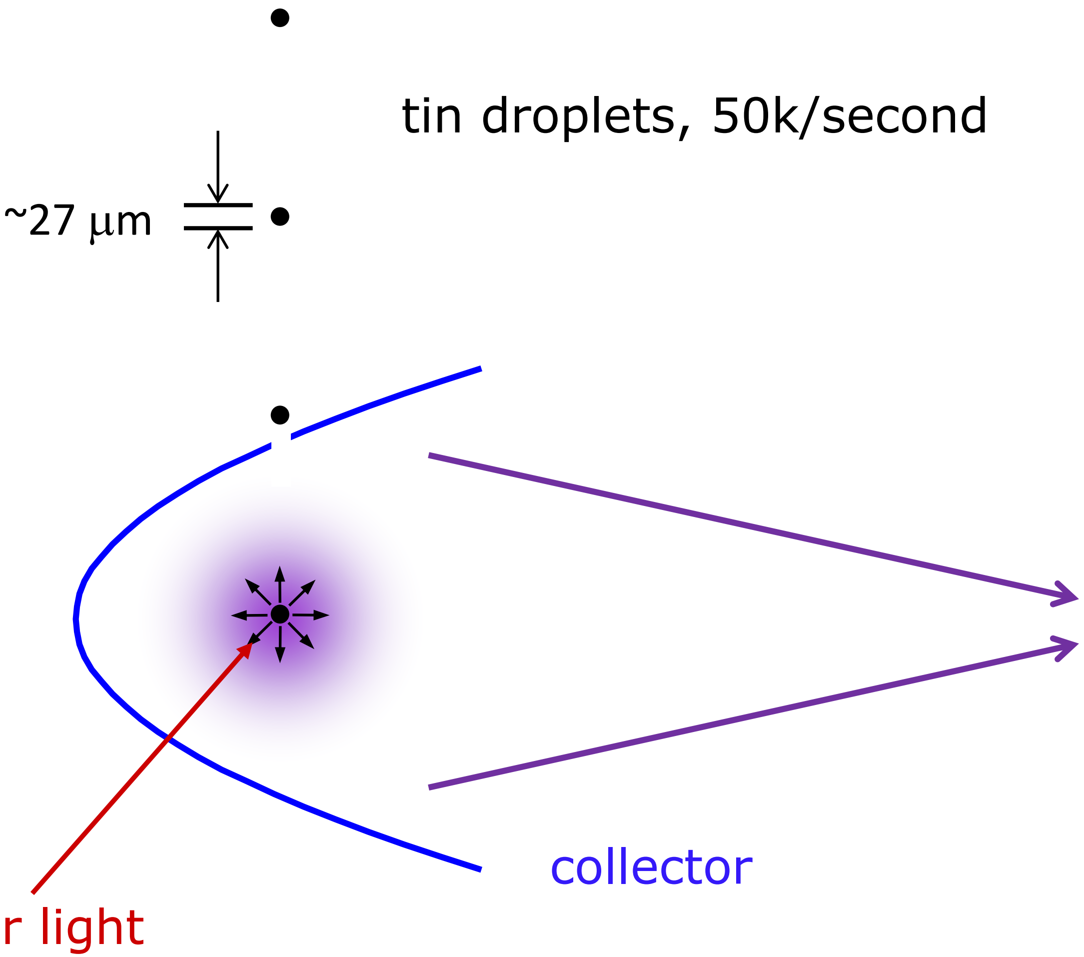
Reliability

Early EUV light source



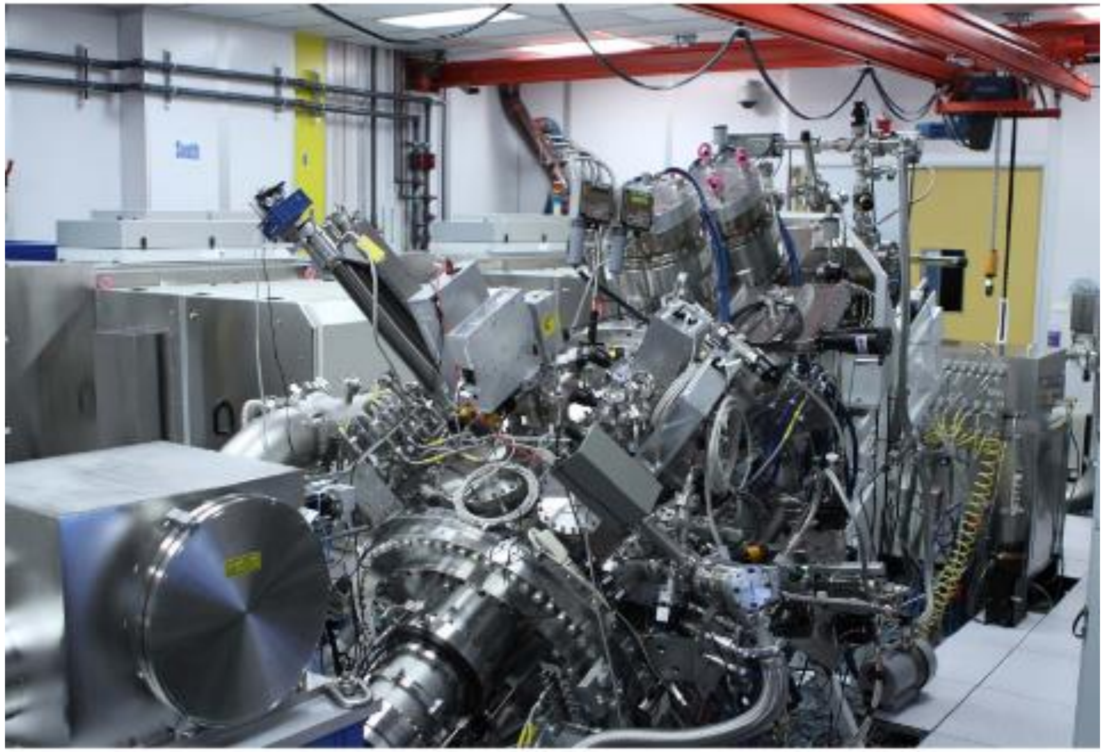
- System complexity is self-evident
  - Intrinsic to laser-produced plasma sources

Laser-produced plasma EUV light source



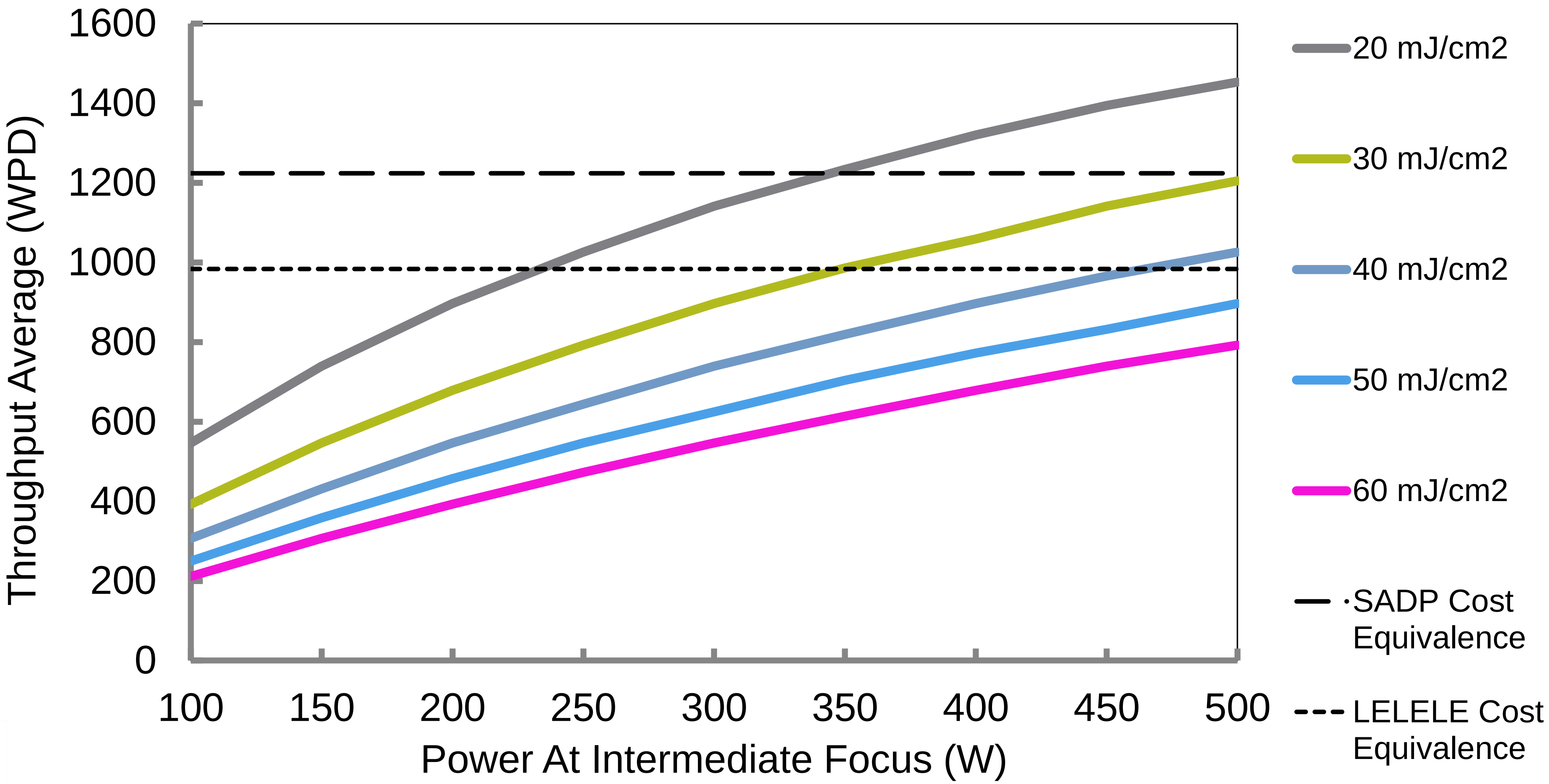
Reliability

Early EUV light source

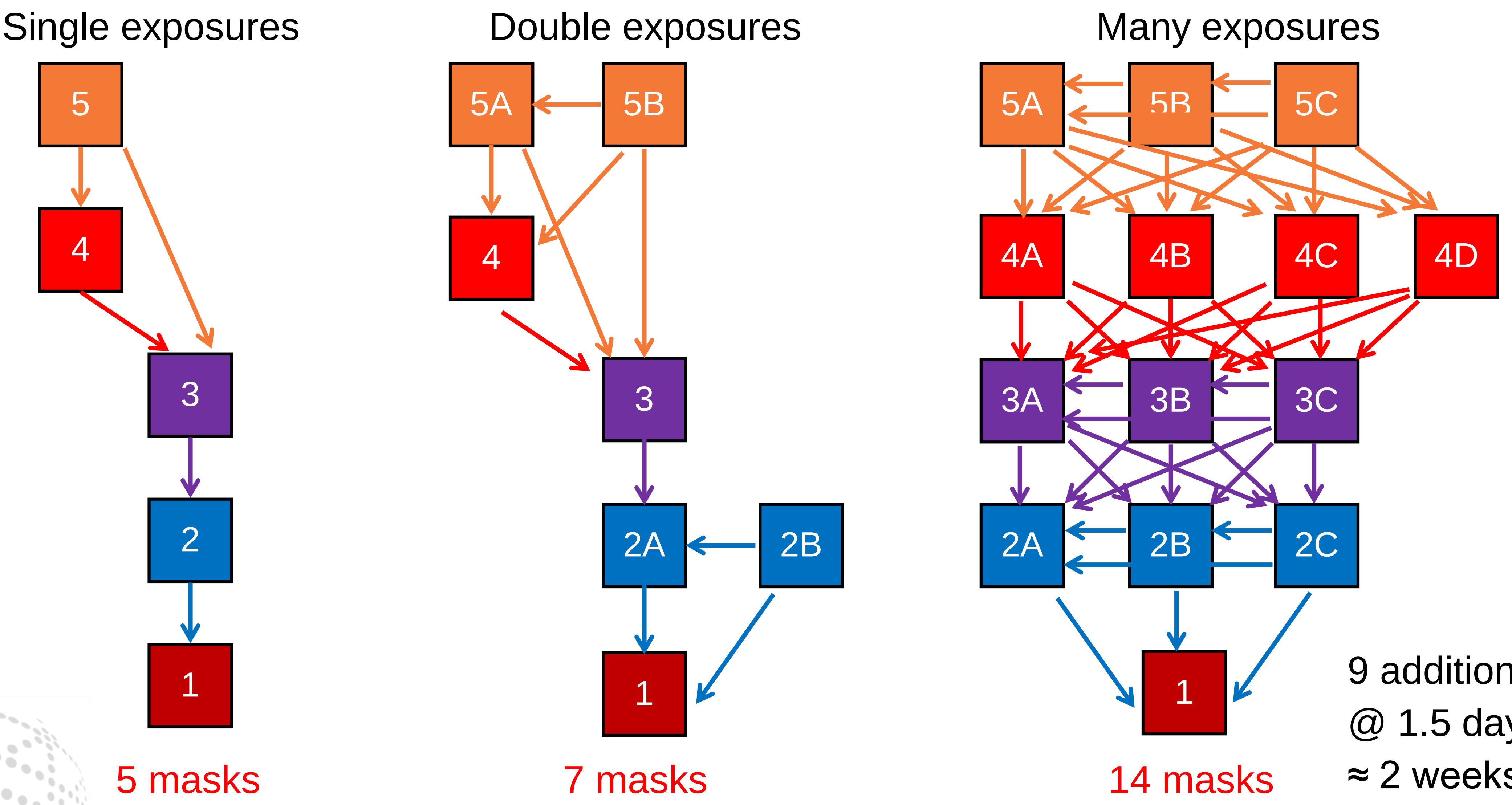


- When reliability is extremely poor, it is difficult to make progress.
  - Example: Improving collector lifetime to many Gpulses.
- A threshold appears to be crossed, and reliability improvement at higher powers is moving forward.
- In spite of the intrinsic challenges, it is not unreasonable to expect ~250 W sources with > 90% availability.
- With such sources, cost parity with immersion triple patterning can be approached.

Scanner throughput versus source power for different resist sensitivities



New motivation for using EUV lithography



9 additional masks
@ 1.5 days per mask
≈ 2 weeks

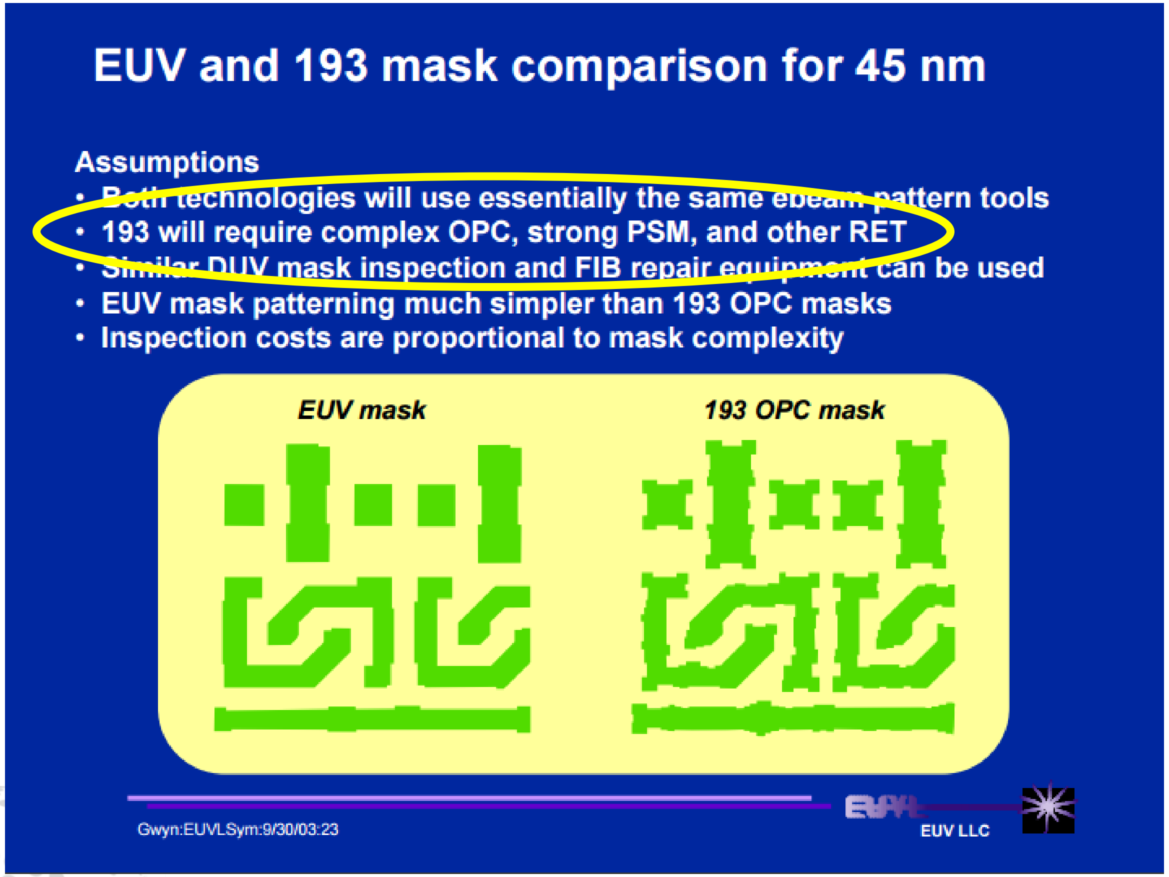
Current activities

- We are motivated
  - Simpler processes
  - Reduced cycle time
- Line-of-sight to HVM capability

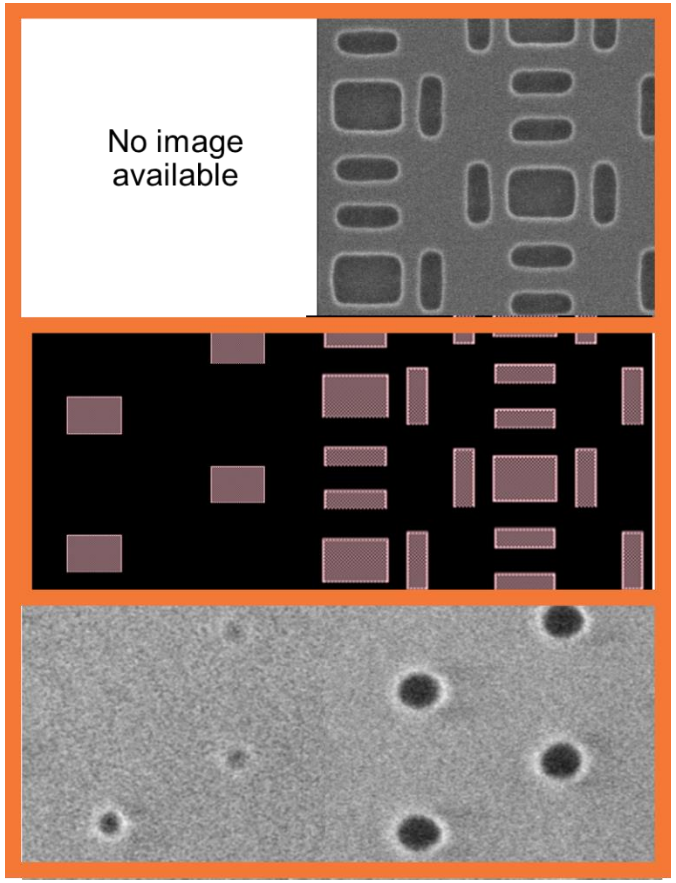
What is left to be done?

OPC for EUV

Chuck Gwyn, “EUV Lithography in Perspective,” 2003 EUV Symposium,



Deniz Civay, et al., “Subresolution assist features in extreme ultraviolet lithography,” JM3 (2015)

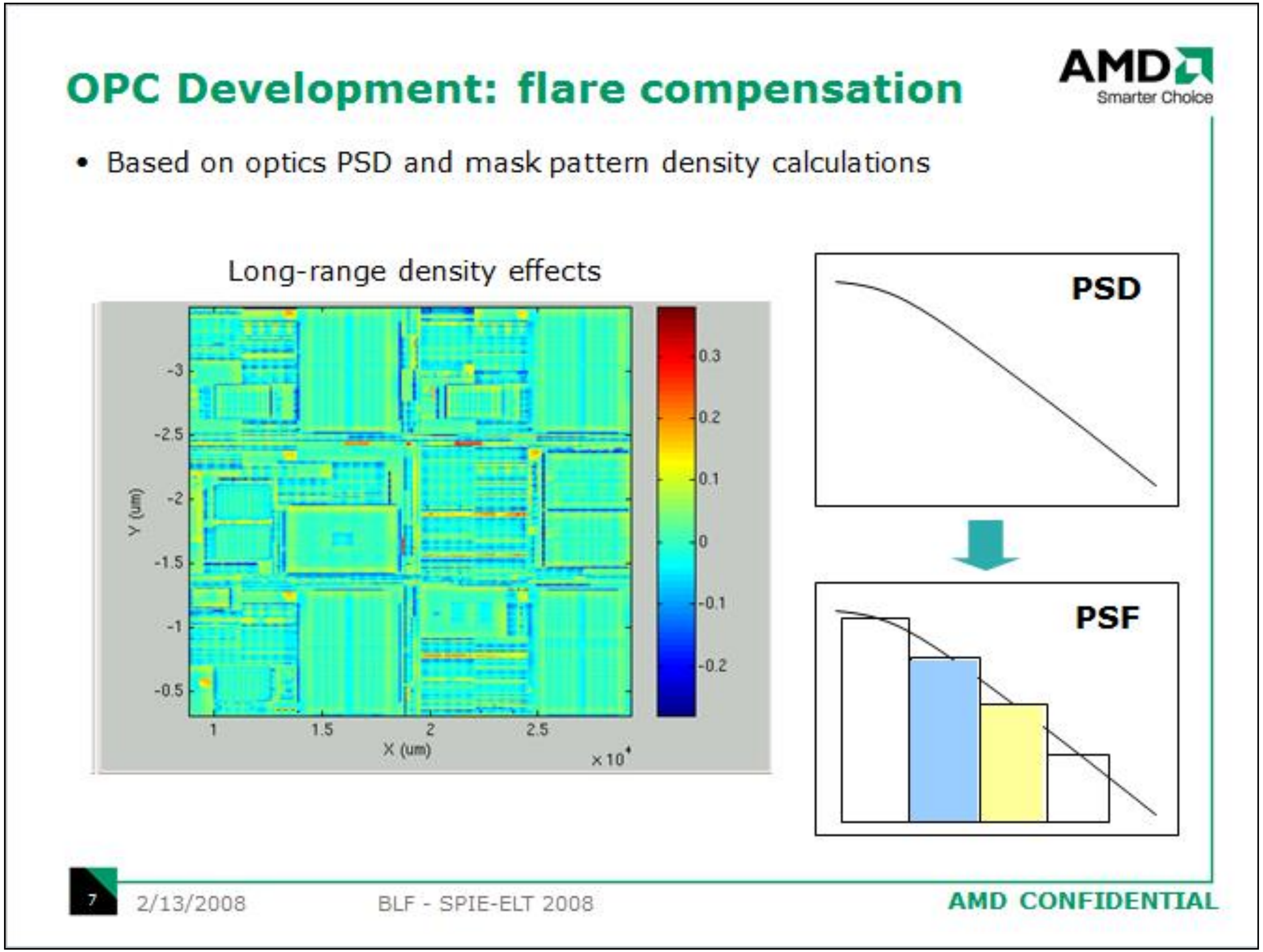


Mask SEM image

Design layout

Developed resist on-wafer SEM image

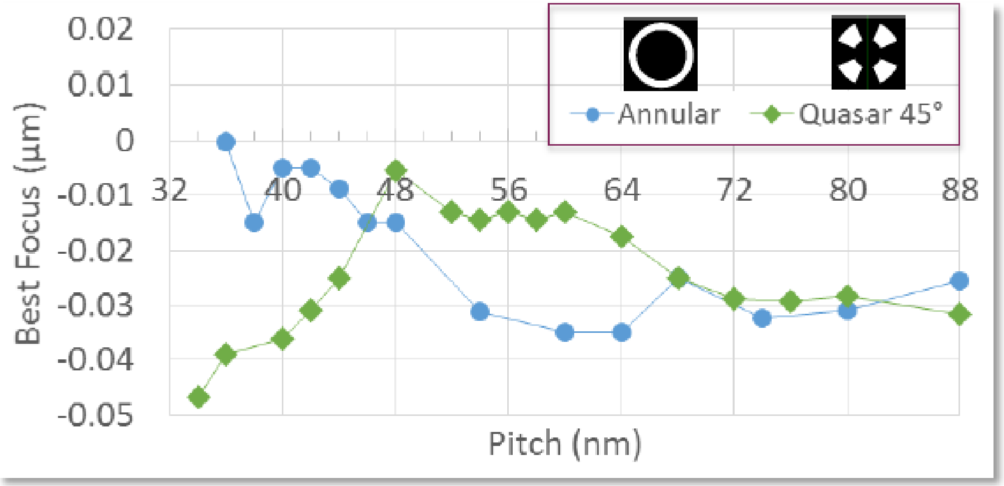
OPC for EUV

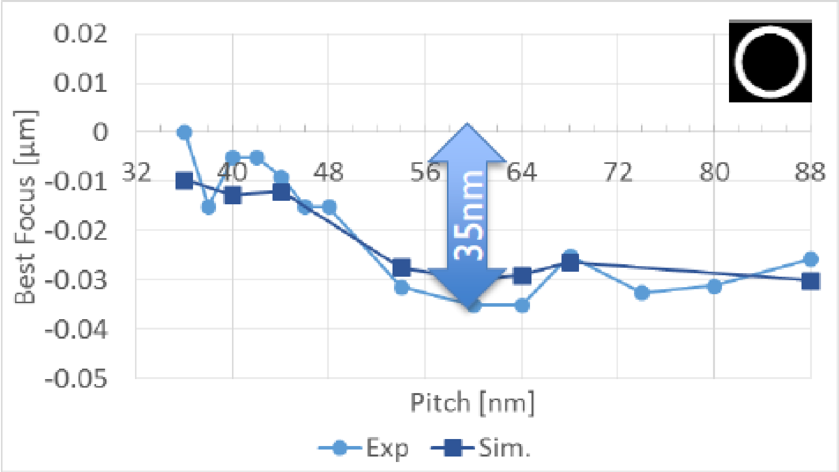

OPC Development: flare compensation
AMD
Smarter Choice
• Based on optics PSD and mask pattern density calculations
Long-range density effects
Y (um)
-3
-2.5
-2
-1.5
-1
-0.5
1
1.5
2
2.5
X (um)
× 10⁴
0.3
0.2
0.1
0
-0.1
-0.2
PSD
PSF
7
2/13/2008
BLF - SPIE-ELT 2008
AMD CONFIDENTIAL

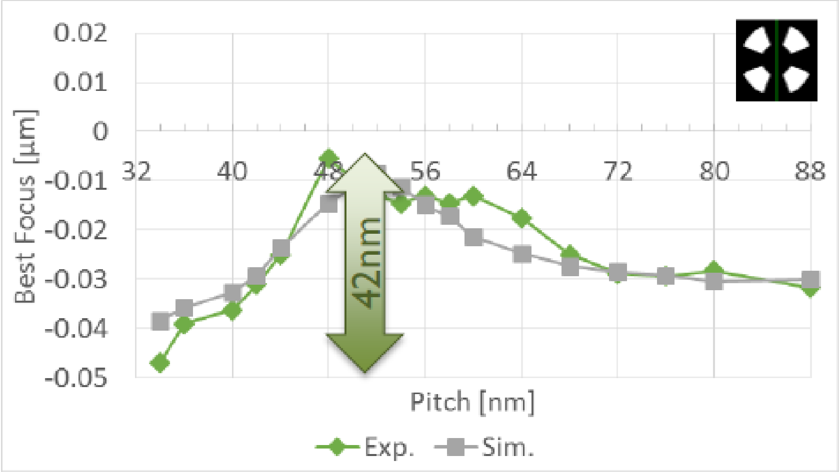
OPC and RET for EUV

BEST FOCUS THROUGH PITCH

Vertical trenches through pitch (34nm to 88nm)







Experimentally determined Best Focus through pitch are

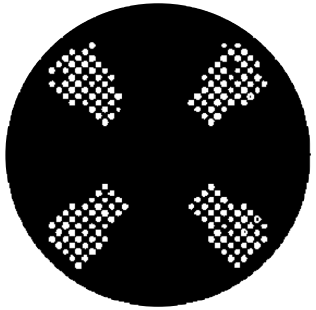
- illumination dependent
- strongest at the smaller pitches (≤ 48nm)
- predicted by rigorous mask 3D simulation

“NXE:3300 Insertion for N7 : Status and Challenges,” Vicky Philipsen, et al., 2015 International Symposium on EUV Lithography

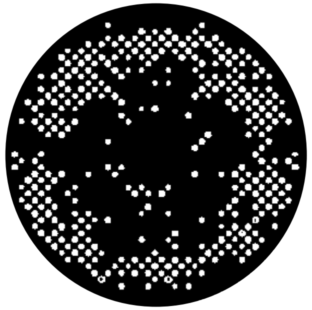
- experimental manifestation of Mask 3D effect predicted by rigorous simulations

imec ASML 14 2015 International Symposium on Extreme Ultraviolet Lithography, Maastricht

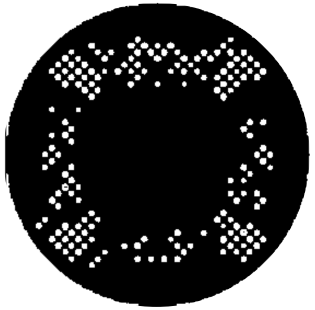
Source-mask optimization (SMO) for EUV



Quadrupole illumination

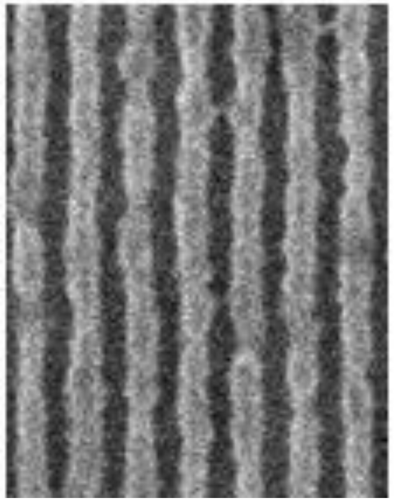


SMO standard solution



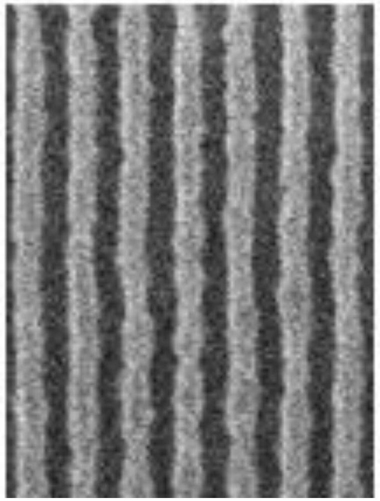
SMO NILS optimized

32 nm lines/spaces



NILS = 1.61
LER = 3.6nm

NILS = 1.57
LER = 3.7nm



NILS = 2.05
LER = 2.6nm

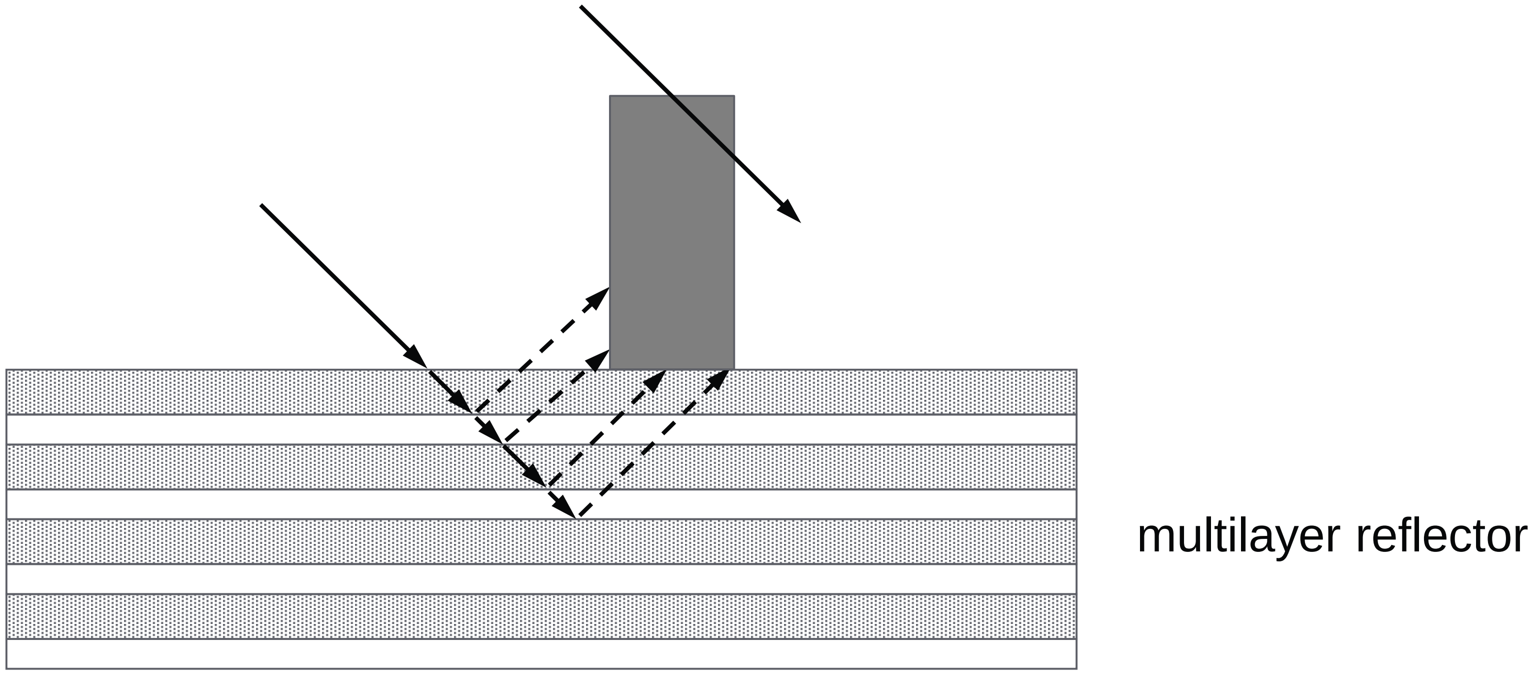
"Application of EUV resolution enhancement techniques (RET) to optimize and extend single exposure bi-directional patterning for 7nm and beyond logic designs"

Ryoung-Han Kim et. al.,

SPIE Advanced Lithography Symposium (2016)

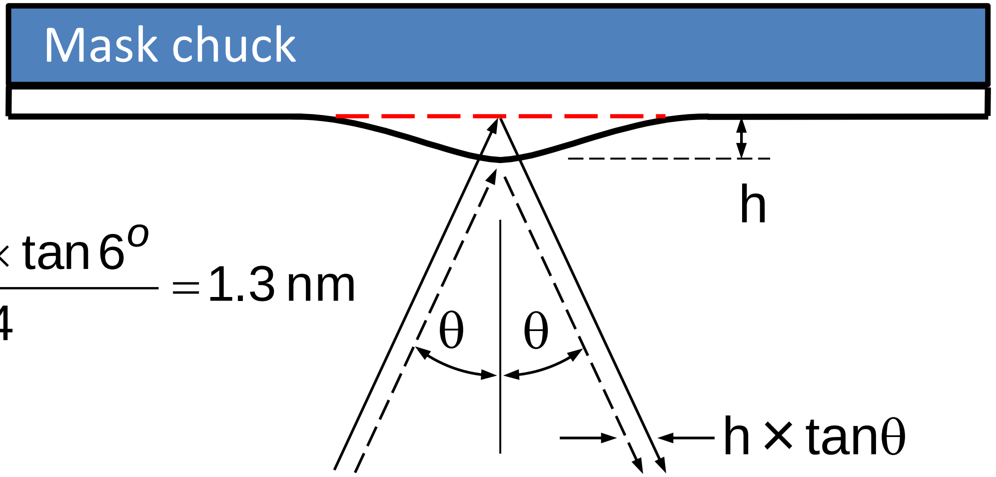
OPC for EUV

- The EDA infrastructure for EUV lithography is maturing.
  - SRAFs
  - Flare
  - Compensation for pitch-dependent focus resulting from oblique illumination geometry.
  - Maximizing NILS for better LER.



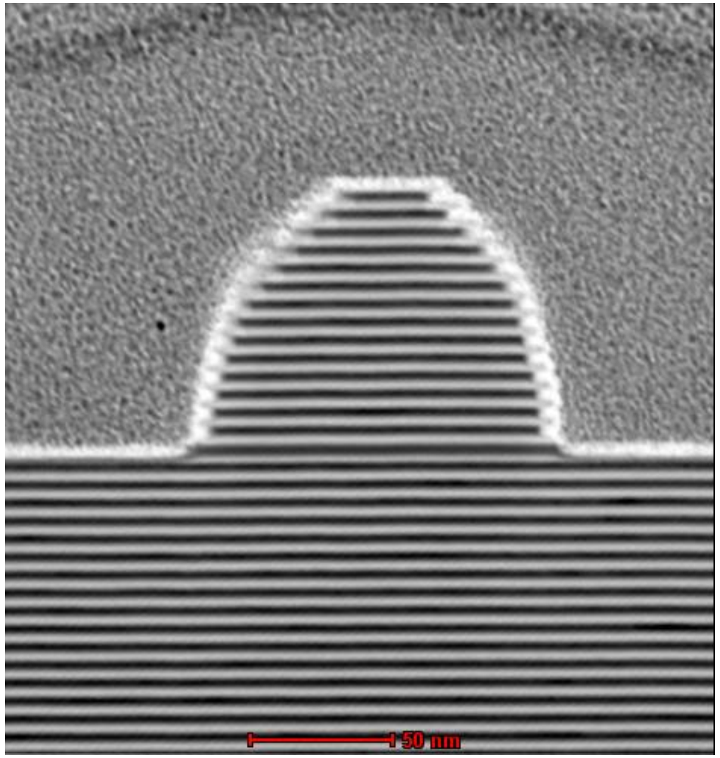
Process control for EUV

New physics: Mask non-flatness → overlay errors

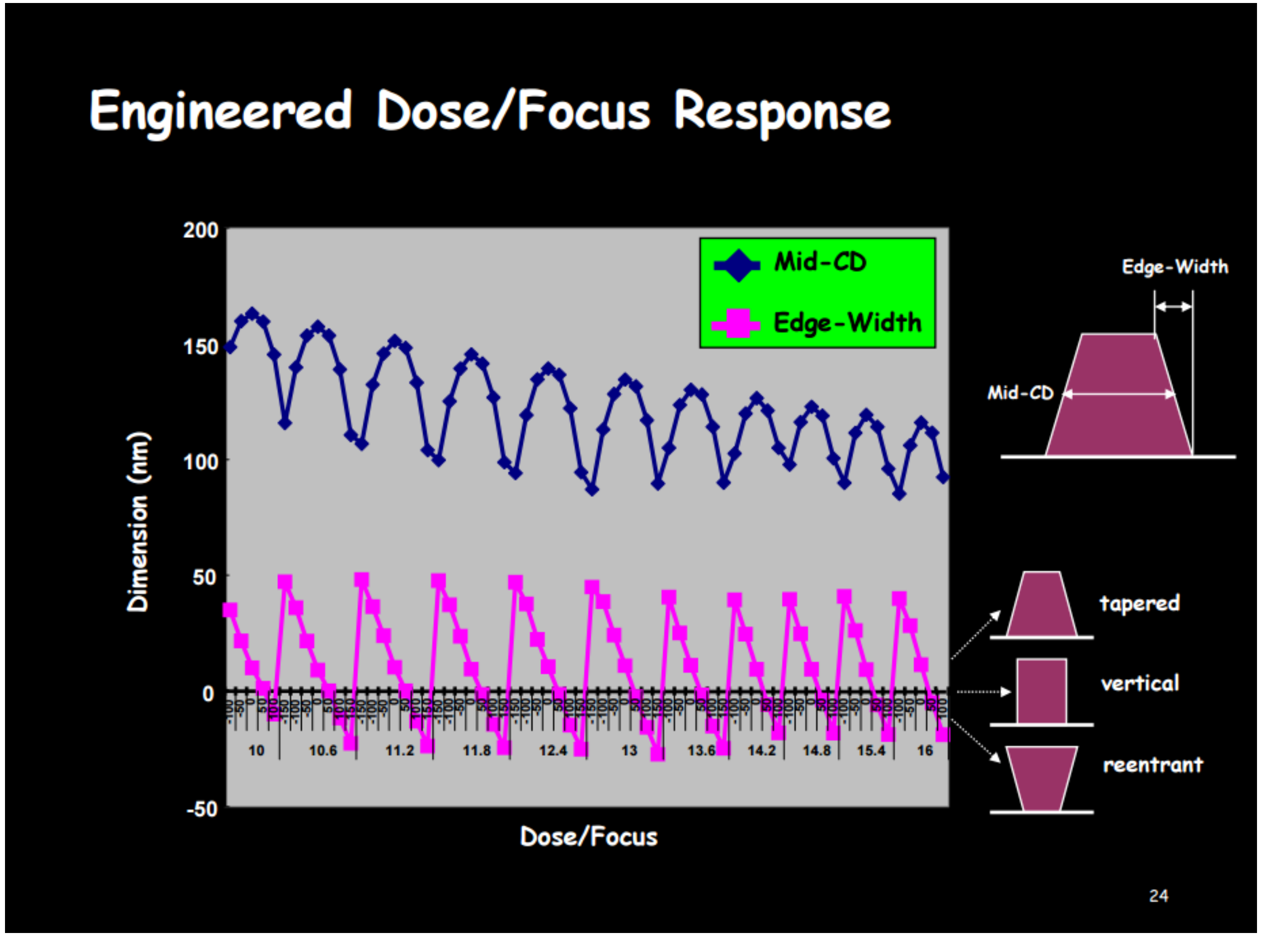


$$\frac{50\,\text{nm} \times \tan 6^{o}}{4} = 1.3\,\text{nm}$$

Early EUV phase-shifting mask

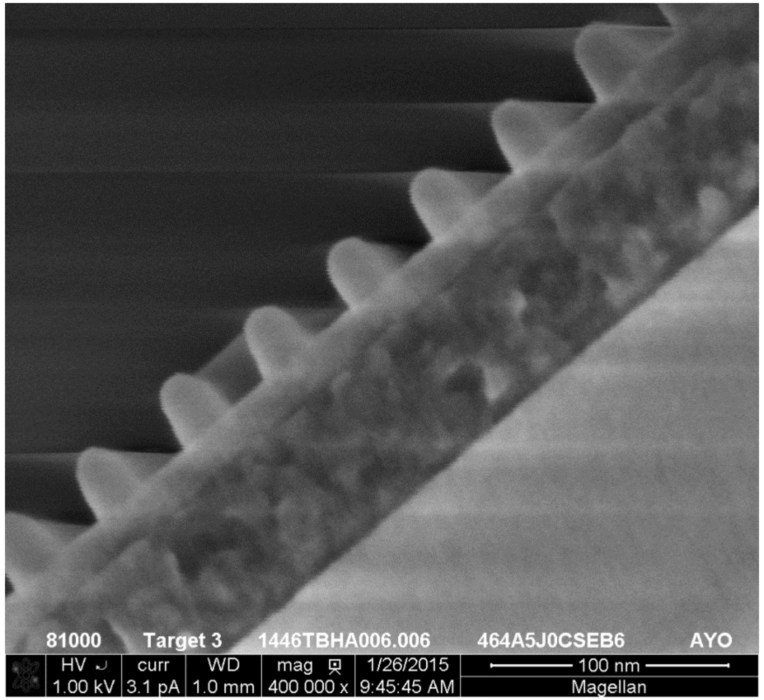


Process control for EUV



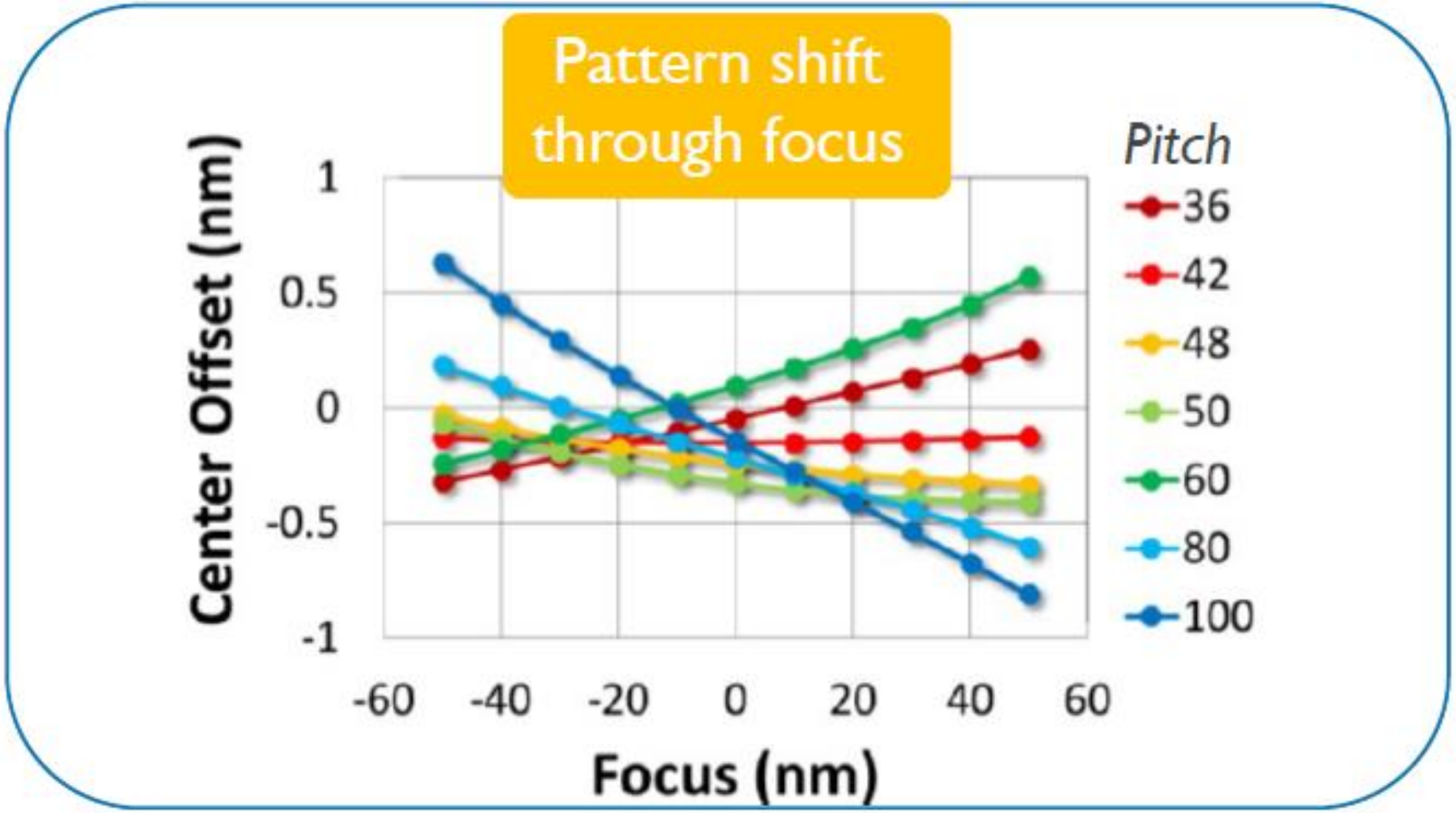
From “Patterning at the Precipice,” Kit Auschnitt, 5th International Symposium on Immersion Lithography Extensions, The Hague, Netherlands, Sept. 2008

50 nm thick EUVJ2121 resist



This SEM is from work performed by the Research Alliance Teams at various IBM research and development facilities

Process control for EUV

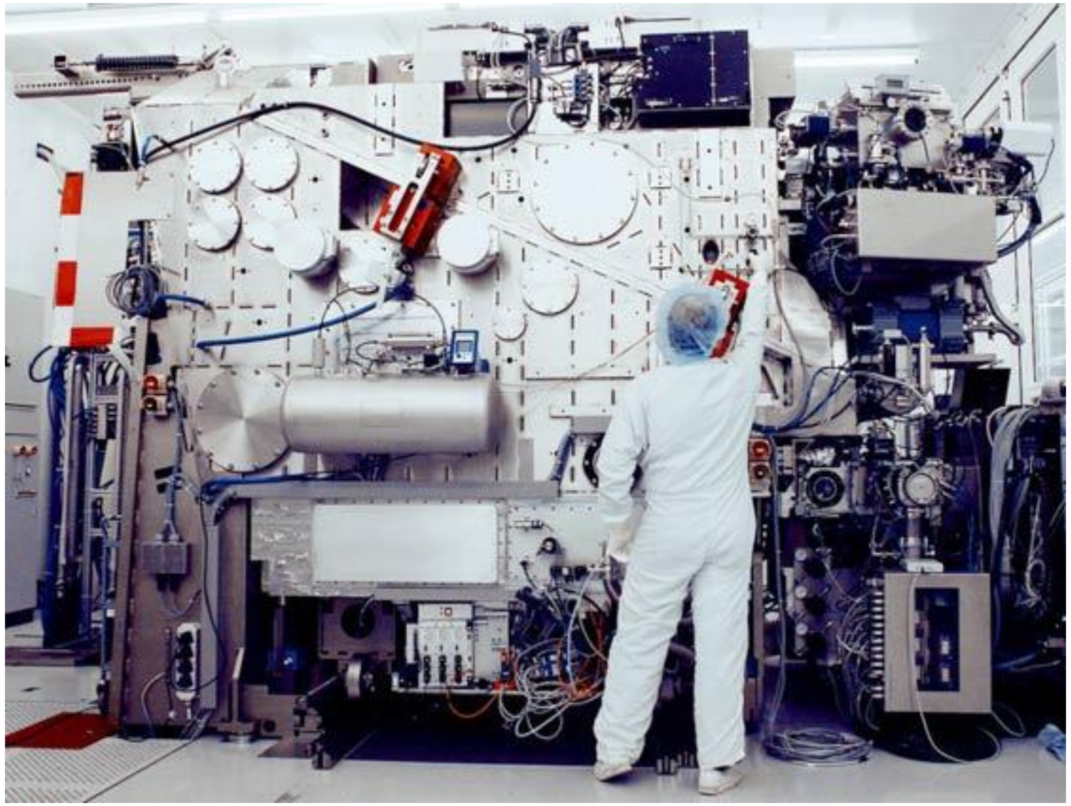


Lieve Van Look, Iacopo Mochi, Vicky Philipsen, Vu Luong, Emily Gallagher, Eric Hendrickx, et al.,
"EUV mask 3D Effects and Possible Mitigation Strategies"

Process control for EUV

Optics, mask and wafers are in vacuum

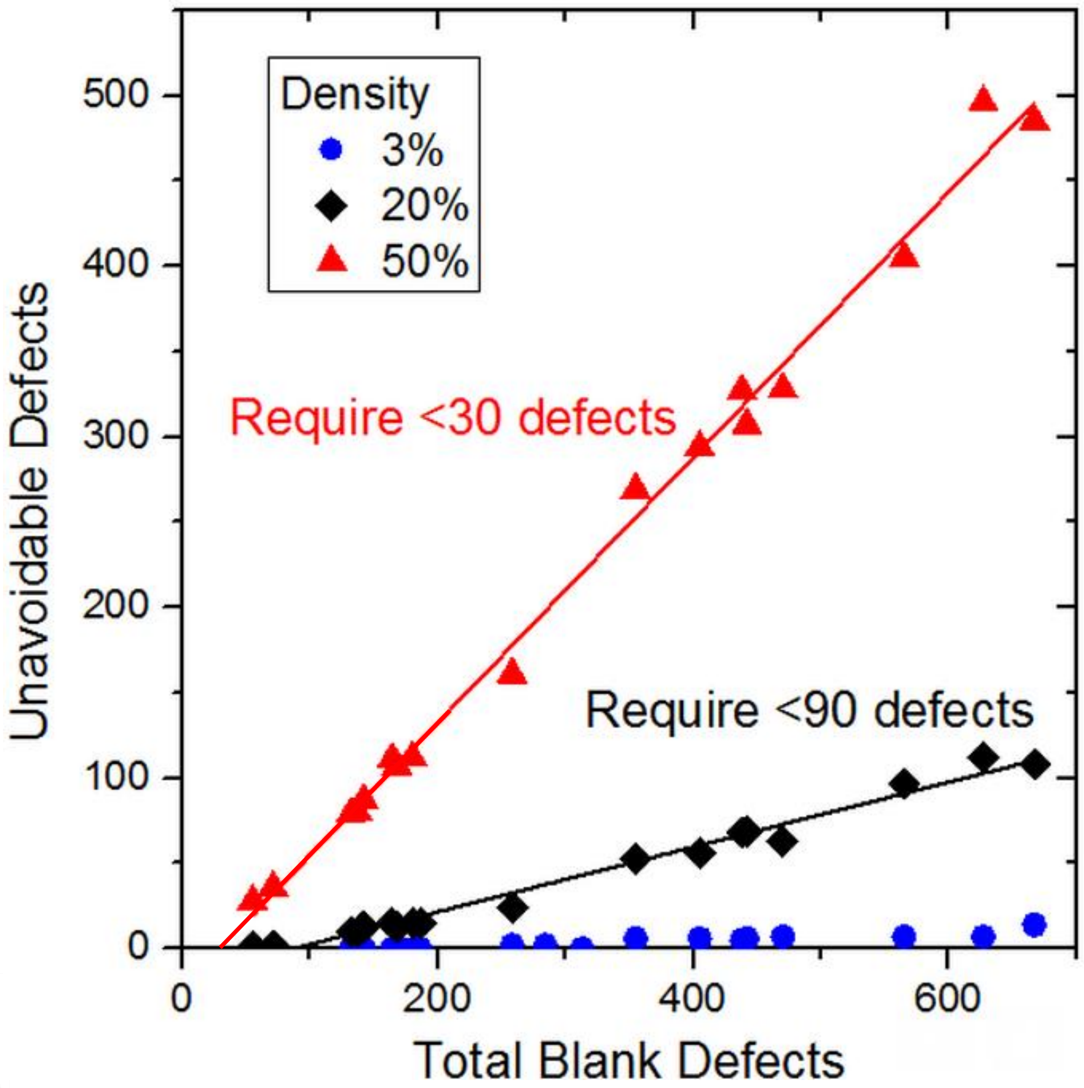
$$k_1 \frac{\lambda}{NA} = 0.32 \frac{13.5}{0.33} = 13\,\text{nm}$$



CD control = ±0.12×13 nm = ±1.6 nm

Overlay control ≤ ±2.5 nm

EUV mask blank defects



- For defectivity, mask blank infrastructure can support contact/via masks.
- Low-defect blanks need to become more readily available for supporting high-density line/space patterns.
  - Increasing challenge as feature sizes shrink.

"Defect Avoidance for EUV Photomask Readiness at the 7 nm Node,"

Dr. John Qi, et al.,

Photomask Japan 2016

Status and future

- Lithographers are working through the issues for moving EUV lithography forward to initial insertion into HVM.
  - OPC
  - Process control
  - Mask-making and mask defects
  - Productivity.

- Although 7-nm node can be done with optical lithography, the use of EUV has advantages
  - Cycle time
  - Process complexity

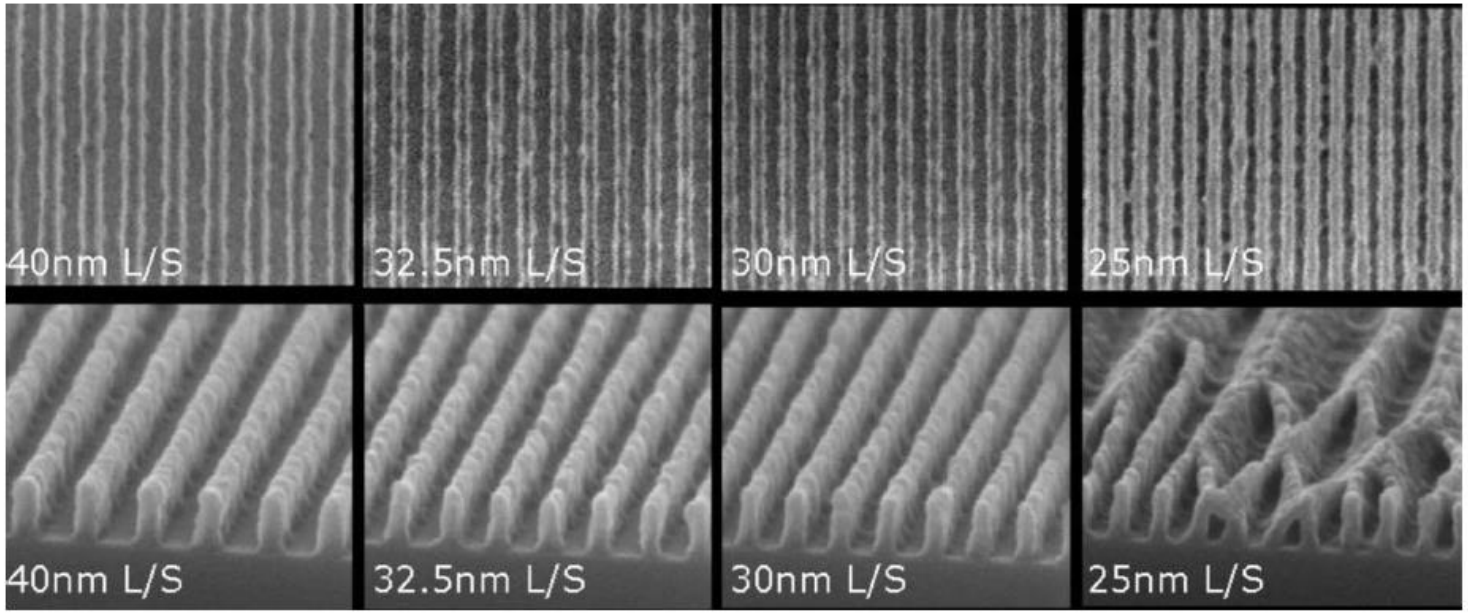
- What will next node with EUV lithography look like?

Next node EUV lithography

- Next node EUV lithography will have the complexities of low k_1.
  - Limit of immersion double patterning is 38-nm pitch.
  - EUV at this next node will have a minimum pitch is 0.7 × 38 nm = 26 nm.

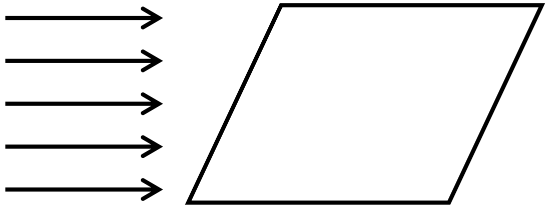
$$13\,\text{nm} = 0.32\,\frac{13.5}{0.33}\,\text{nm}$$

Resist capability



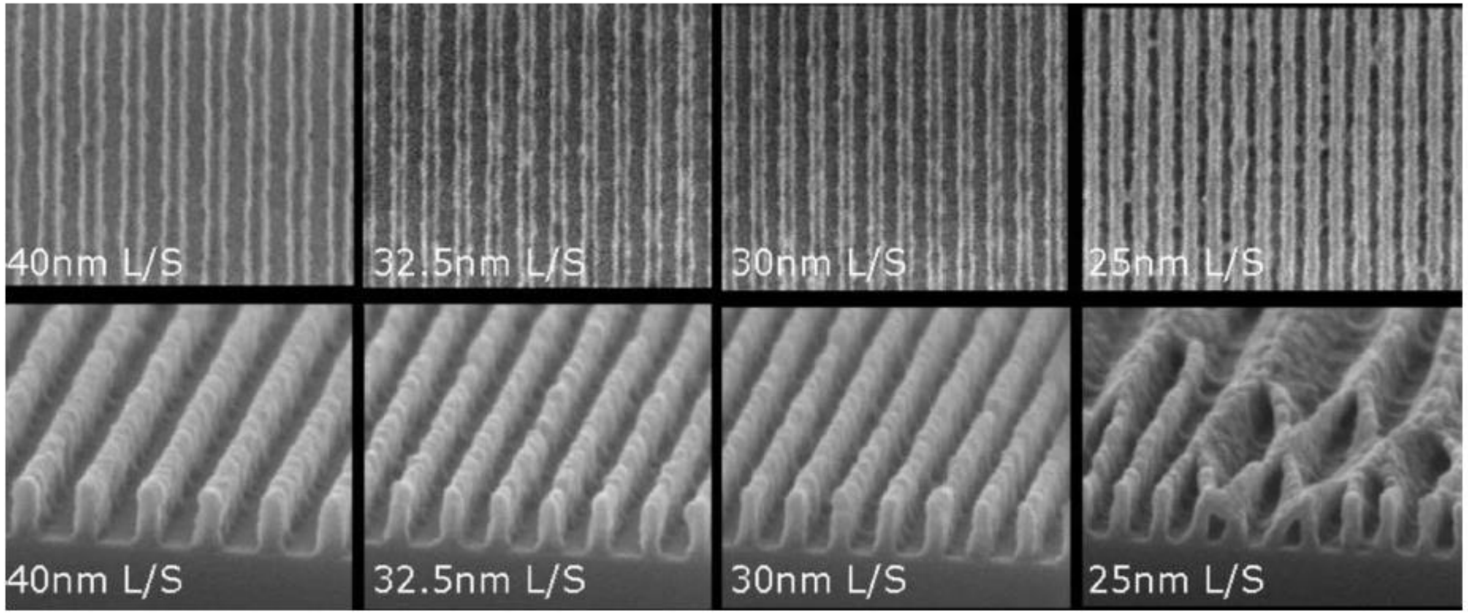
- Issues for imaging <30 nm pitch in resist.
  - LER
    - Stochastic effects.
      - Photon shot noise.
      - Molecular inhomogeneity.
      - Molecular sizes.
  - Pattern collapse

$\langle n \rangle$



$$\sigma \sim \frac{1}{\sqrt{\langle n \rangle}}$$

Resist capability



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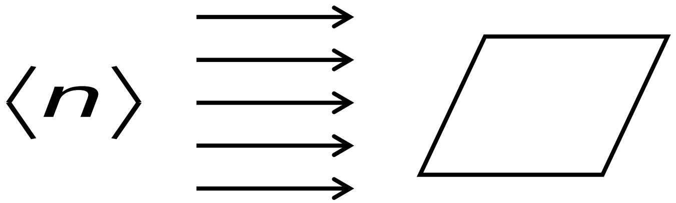
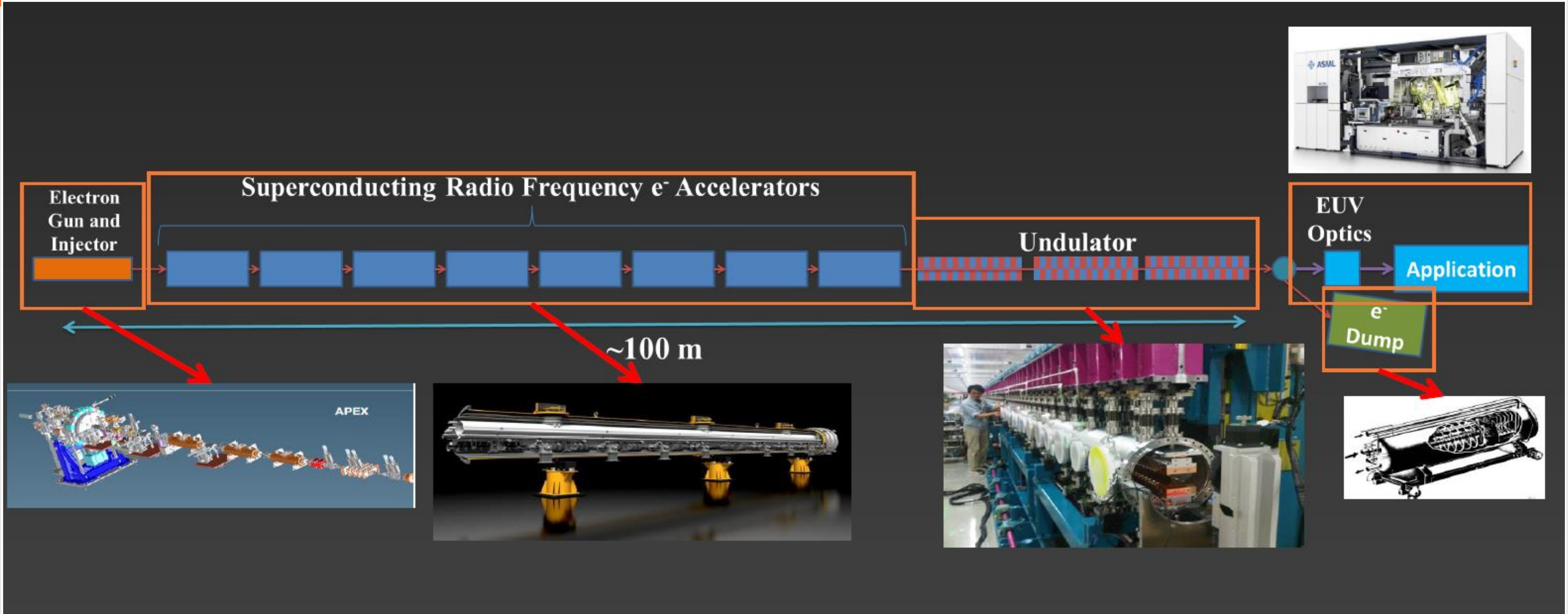


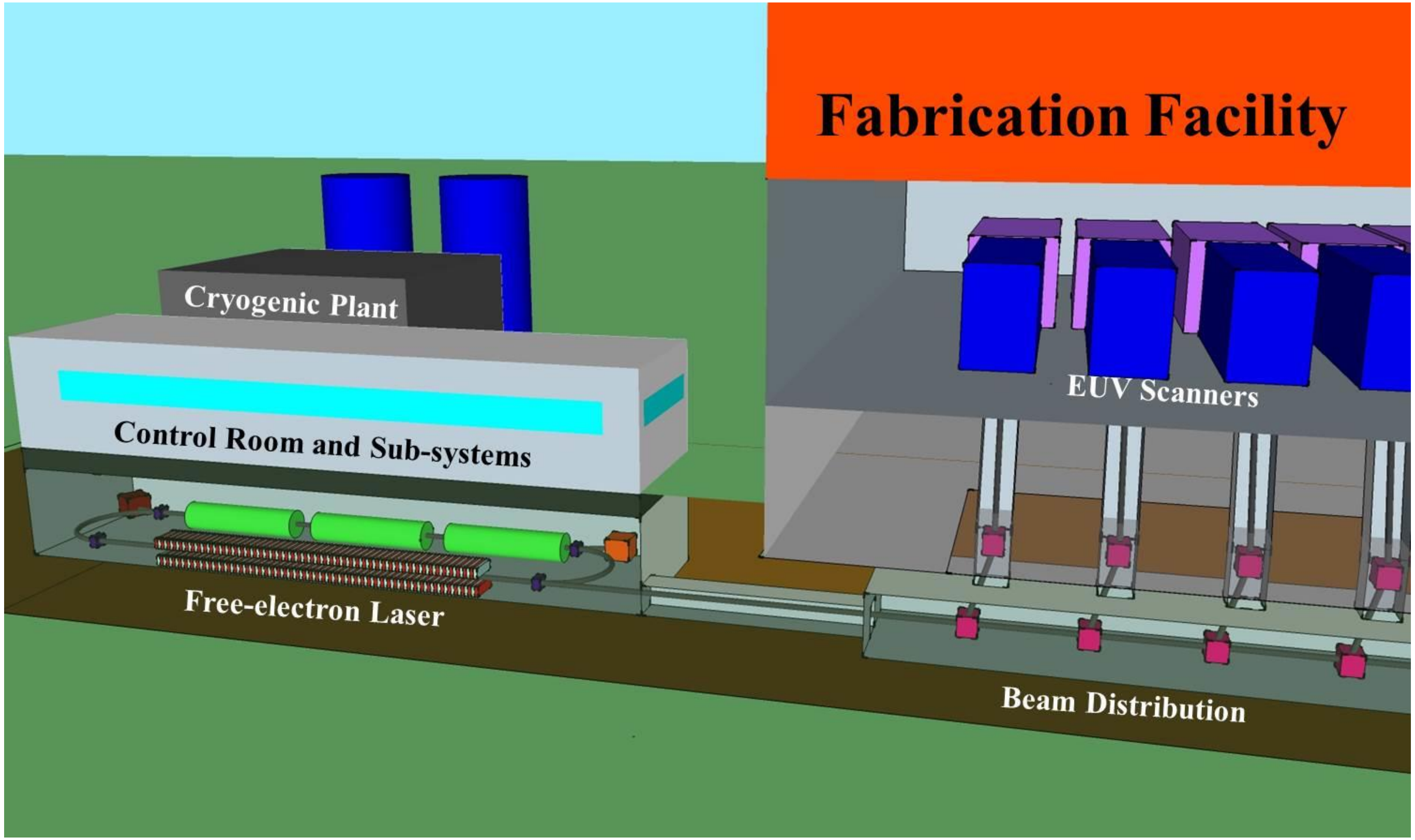
$$\sigma \sim \frac{1}{\sqrt{\langle n \rangle}}$$

EUV free electron laser light sources

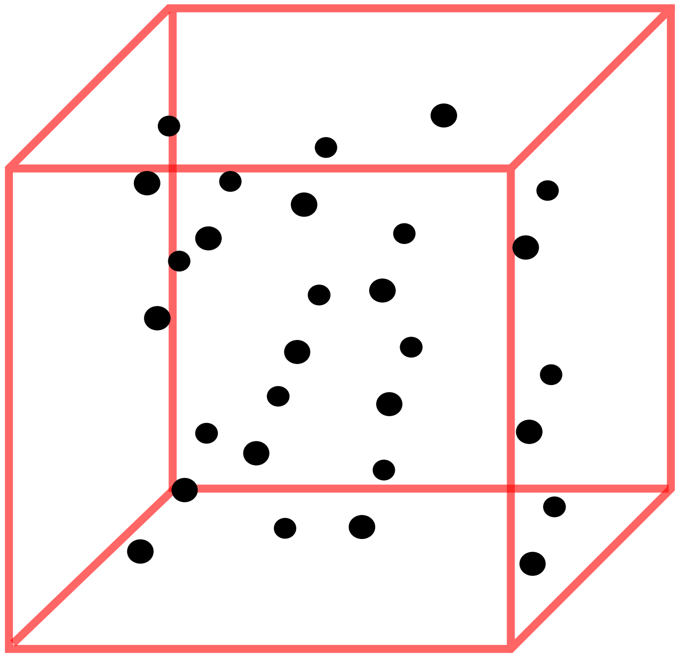


Diagrams courtesy of LBNL APEX Project, ILC, RIKEN, SLAC, ASML

EUV free electron laser light sources



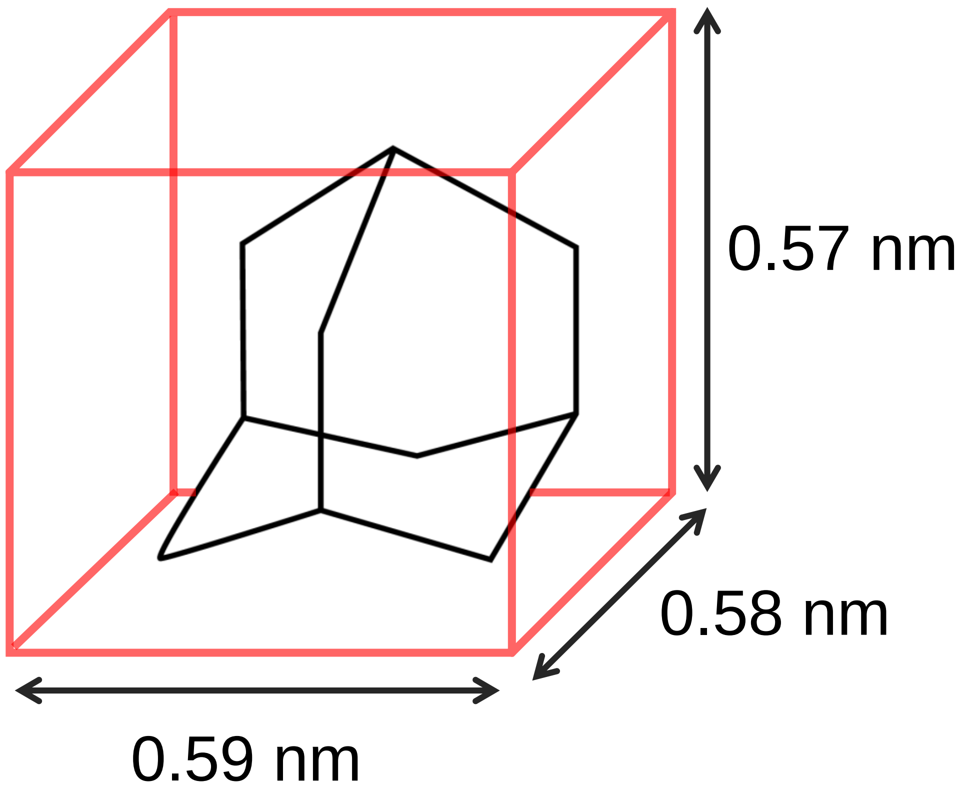
Molecular inhomogeneity



- Mean PAG-PAG spacing ≈ 1.7 nm.
  - In a high PAG-loaded resist.
- Sets another scale for limiting-LER of chemically-amplified resists.
  - This issue applies to all multi-component resists
- Vertical averaging may be important.

Molecular dimensions

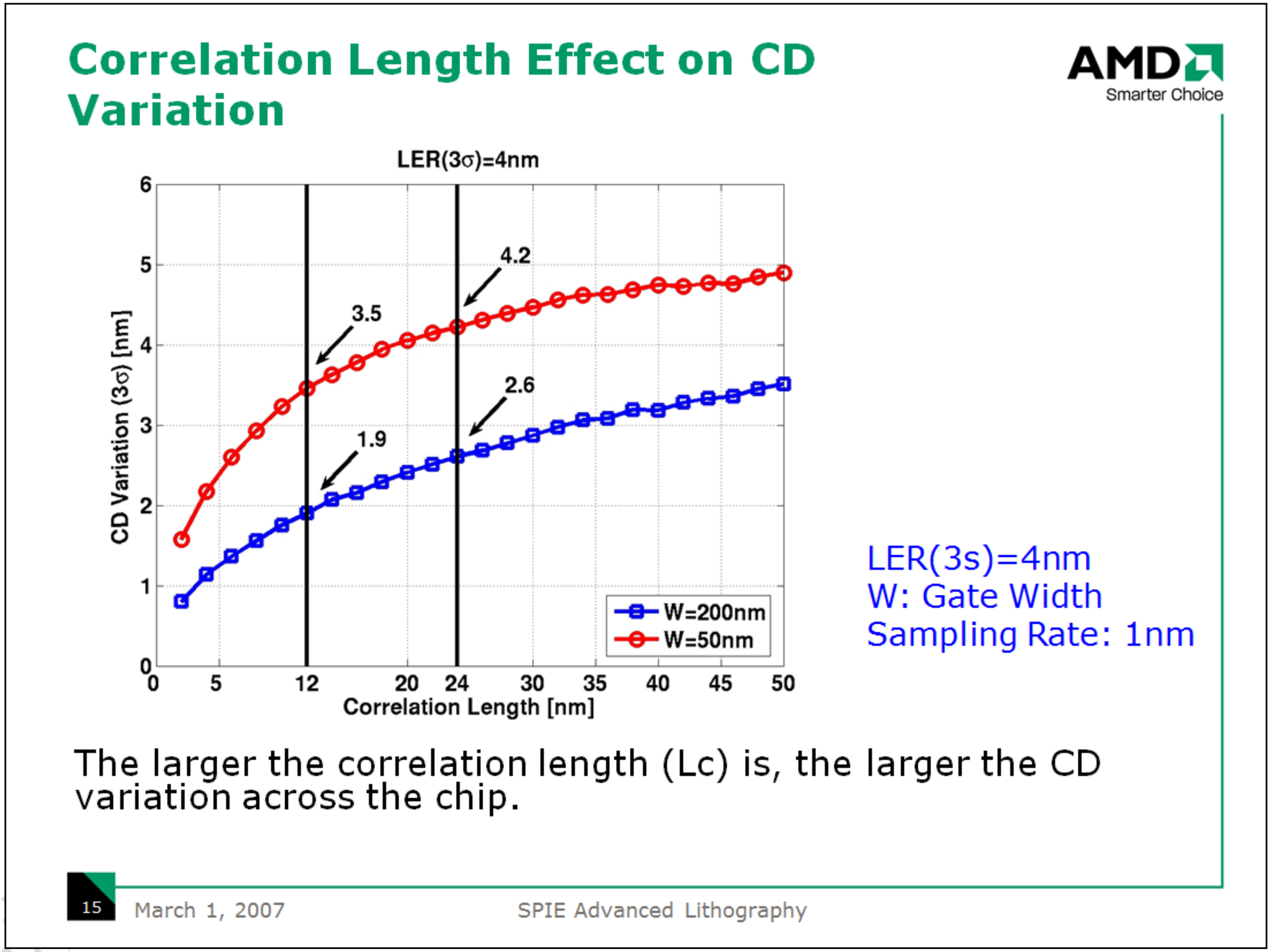
Adamantane molecule



$$10\ \text{nm} = 0.35\,\frac{13.5}{0.5}\ \text{nm}$$

A single moiety represents ~6% of the nominal feature size

LER requirements



- Gate length of planar transistors was considered the most critical linewidth to control
- ITRS specs for LER were based on CD control requirements for planar transistors.
- A new basis for setting LER requirements is needed.

Yuansheng Ma, H. J. Levinson, and T. Wallow, “Line edge roughness impact on critical dimension variation,” SPIE Advanced Lithography Symposium (2007)

Process control

Hypothetical overlay budget

Component	Error (nm)
Exposure tool	1.8
Reticle pattern placement	0.6
Reticle flatness	0.6
Wafer distortion	0.6
Wafer/mask heating	0.6
Mask 3D effects	0.6
Aberrations	0.6
Metrology	0.6
Total	2.4

Components need to be determined to Å level

Summary

- EUV lithography is heading for high volume manufacturing!
  - Engineers still have work to do, but one can see the light at the end of the tunnel.
    - Yield.
    - Process control.
    - OPC.
- Mask defectivity could limit applicability of EUV lithography.
- There are more challenges for extending EUV lithography to the next node.
  - Quanta.
  - Low-defect mask blanks.
  - Continuing challenges of process control.

Acknowledgements

- I would like to thank the following people.
  - Dr. Erik Hosler for providing figures on free-electron lasers.
  - John Biafore of KLA-Tencor for illuminating discussions on stochastic properties of resists.
  - Dr. Timothy Brunner for providing figures.