EUVL Readiness for High Volume Manufacturing

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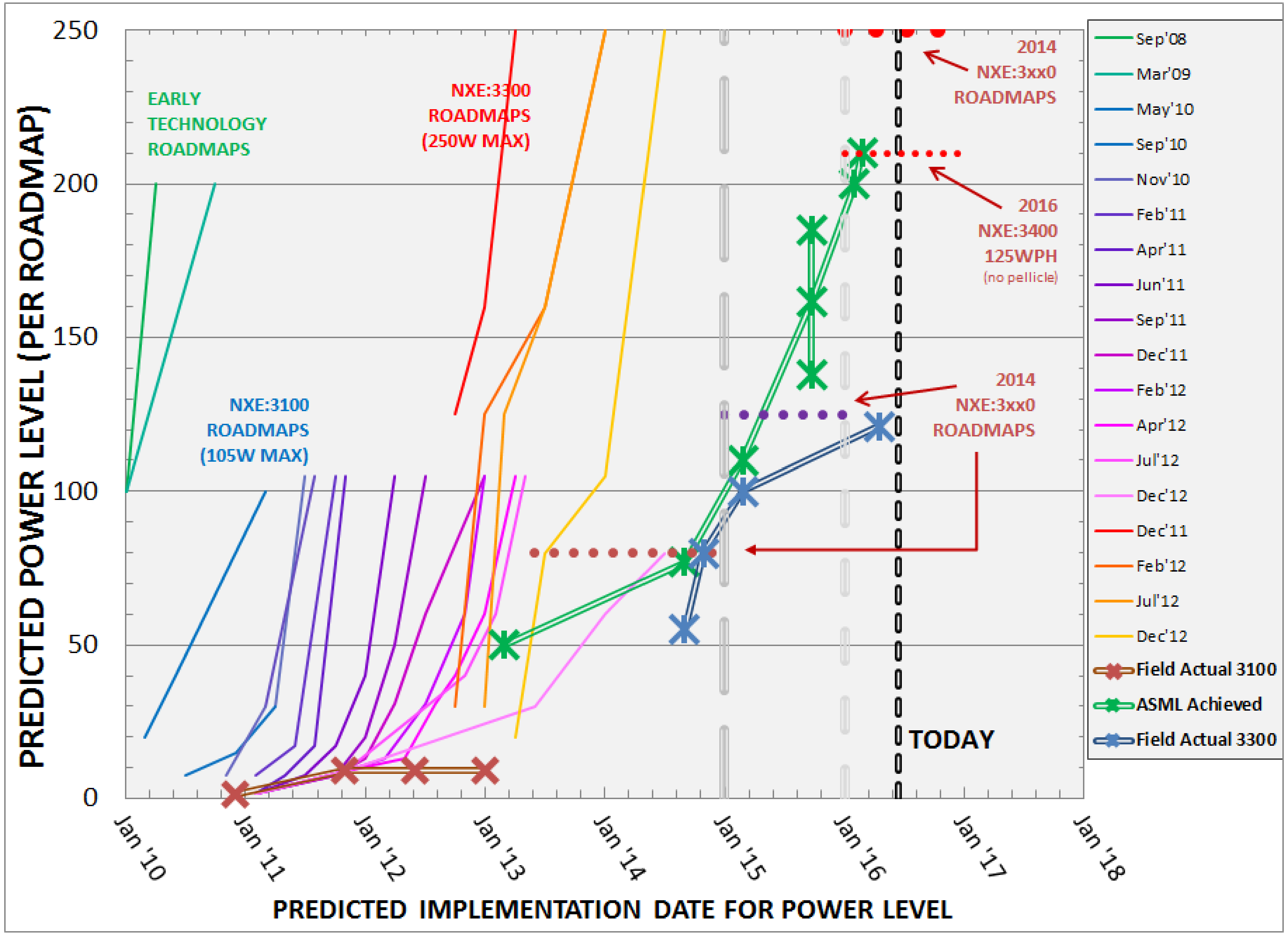
Intel Corporation

Outline

- Exposure Tool Progress
  - Power
  - Availability
  - Intel demo results
- Reticle
  - Defectivity
  - Pellicle
- Materials
- Conclusion

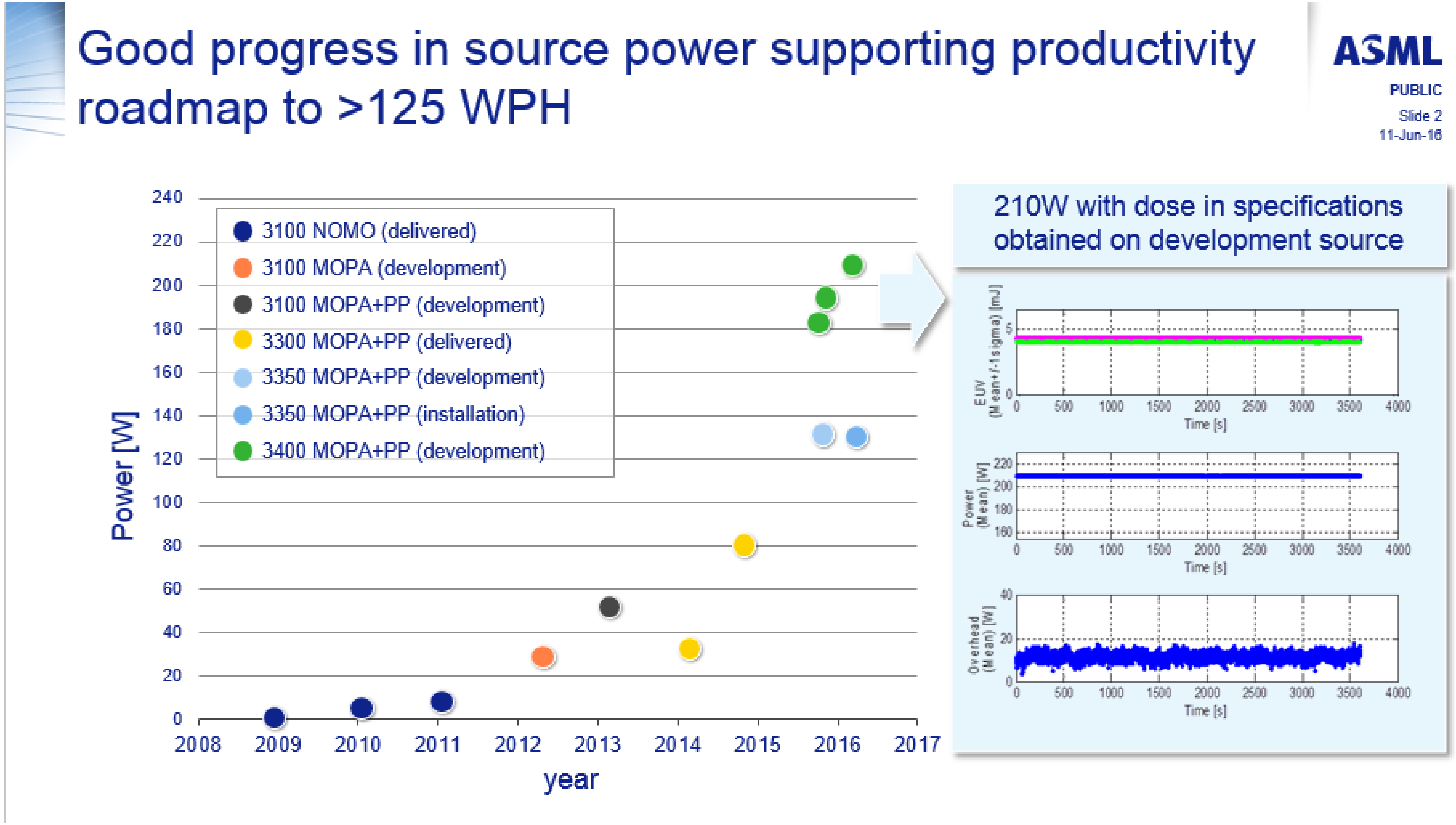
Updated from 2016 SPIE

Source Power Improvements Trending to Plan



- Progress remains on track for EUV exposure source power

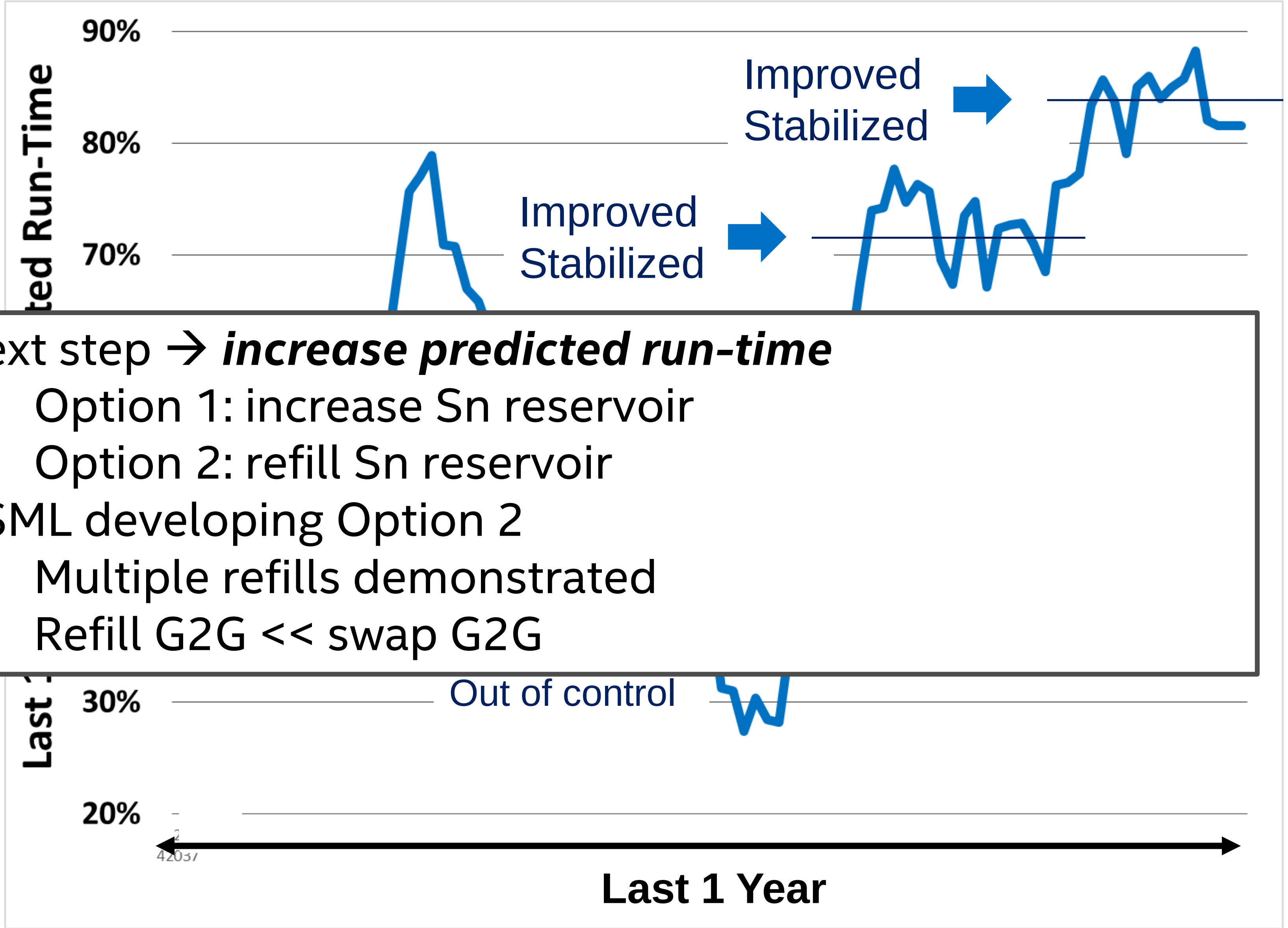
Source Power with Dose Control



- Must ensure satisfactory dose control at high power

Updated from 2016 SPIE

Droplet Generator: run-time and predictability improved



- Next step → ***increase predicted run-time***
  - Option 1: increase Sn reservoir
  - Option 2: refill Sn reservoir
- ASML developing Option 2
  - Multiple refills demonstrated
  - Refill G2G << swap G2G

- >3X increase in run-time
- Improved predictability in actual vs. expected run-time

5x improvement in Droplet Generator run time demonstrated

Data based on ASML internal testing; Field qualification started

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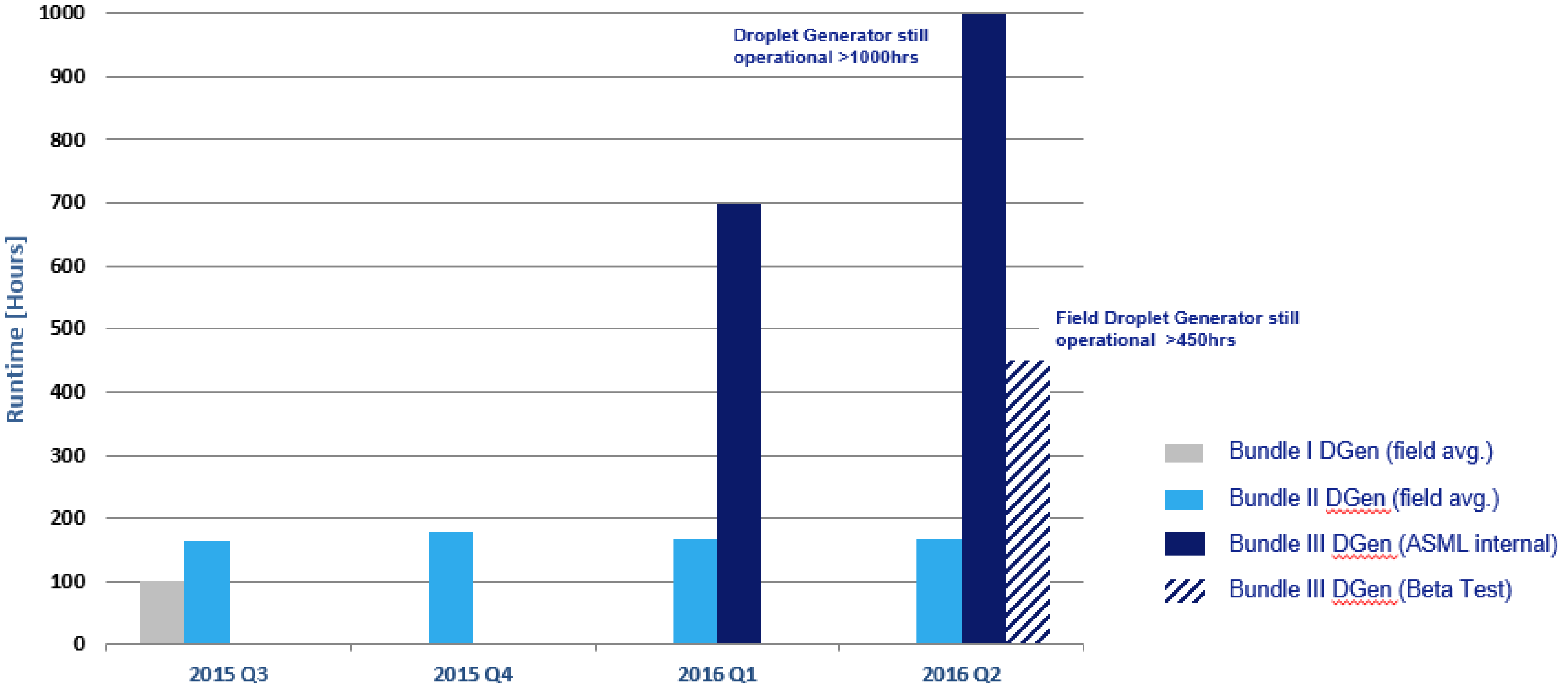


- Expect significant improvement in system availability

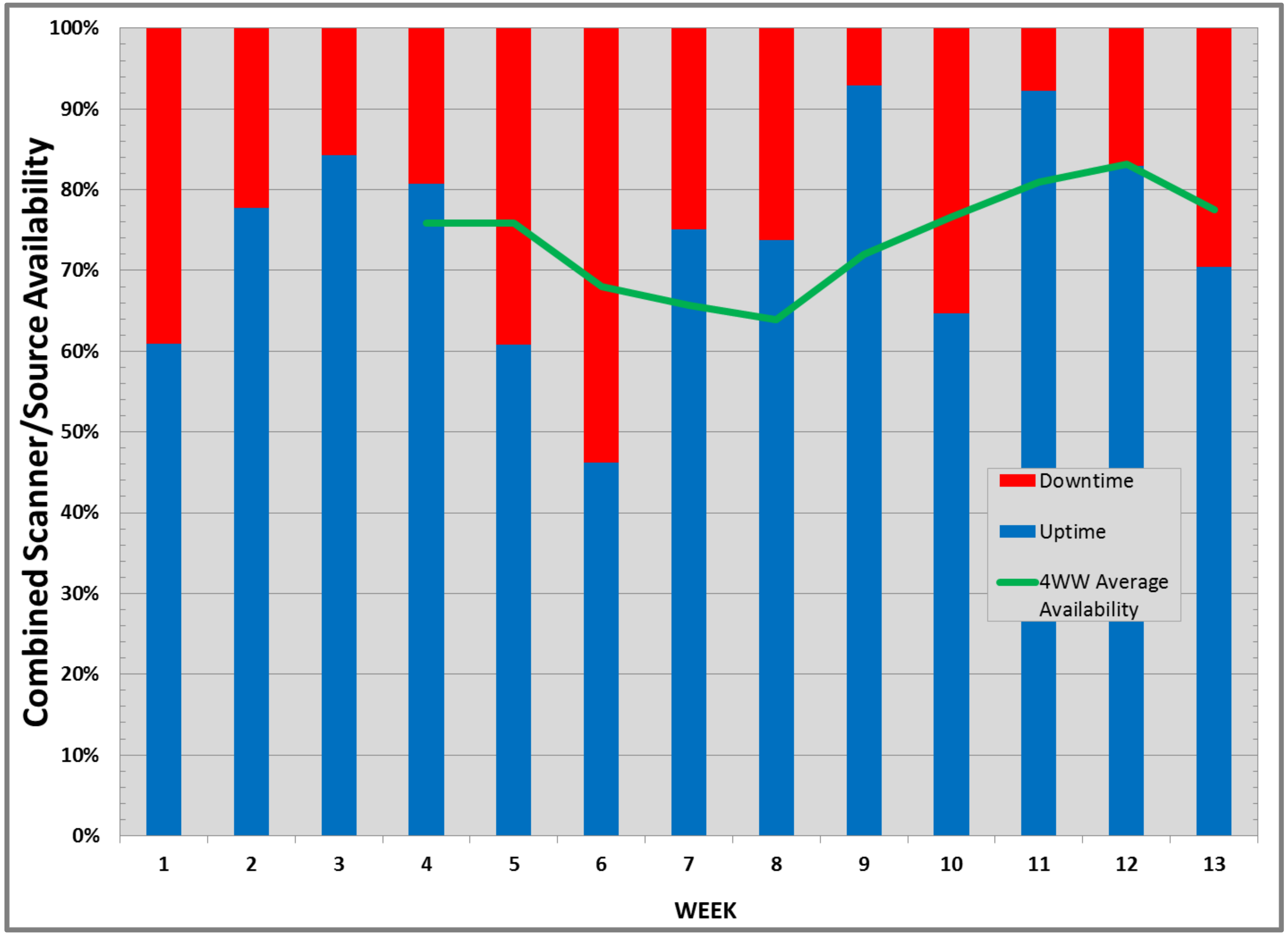
From 2016 SPIE

Extended NXE:3300 demo of availability and predictability

- 21hrs/day wafer cycling with mix of test-chi wafers and bare silicon
- 14nm pilot line (CDs, overlay, in-line test, EOL yield)
- 3-hr daily Intel engineering wi rk)
- Availability counted 24h utput targets set for 21hrs/day in 80W config. (ac
- Only good w ose control specs) counted
- Goal: d l can run as advertised for 80W config today, *including g and overlay*

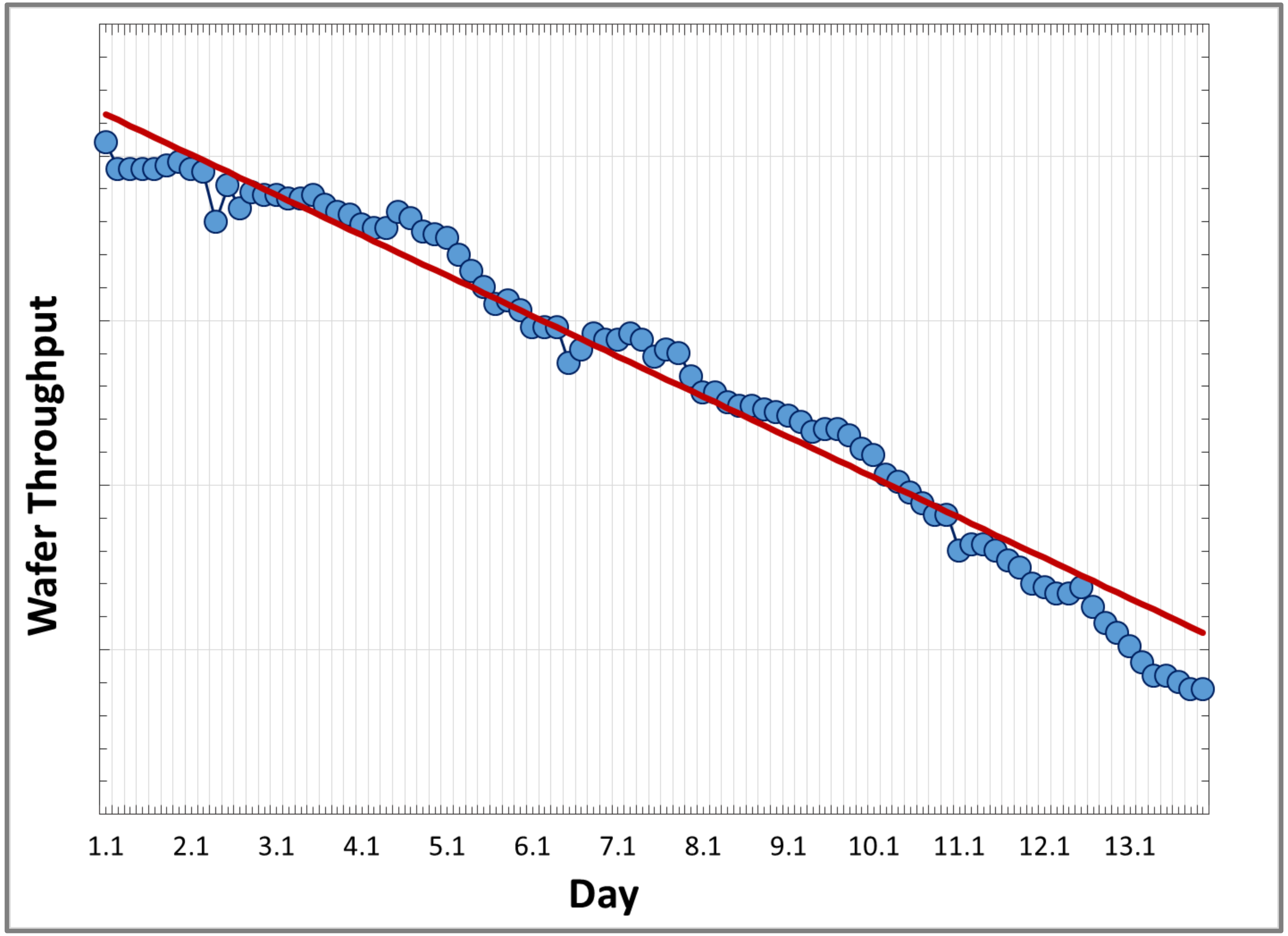
Completed

NXE:3300 Demo: Combined Scanner/Source Availability



- Combined 4-week availability ~70%
- Combined availability meets expectations

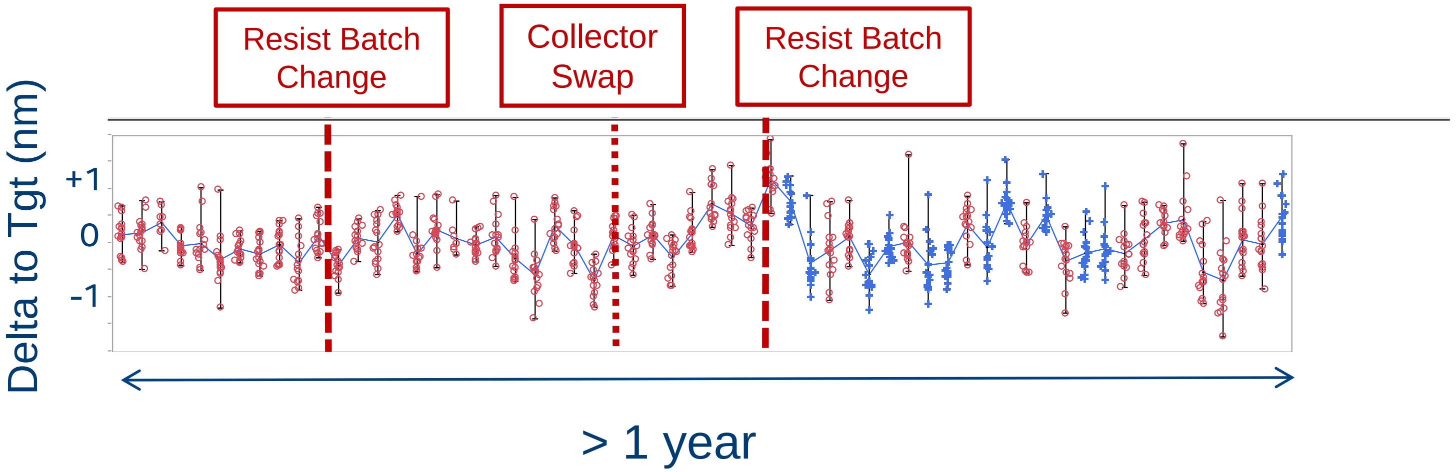
13-week Demo: Collector Reflectivity Effect on TPT

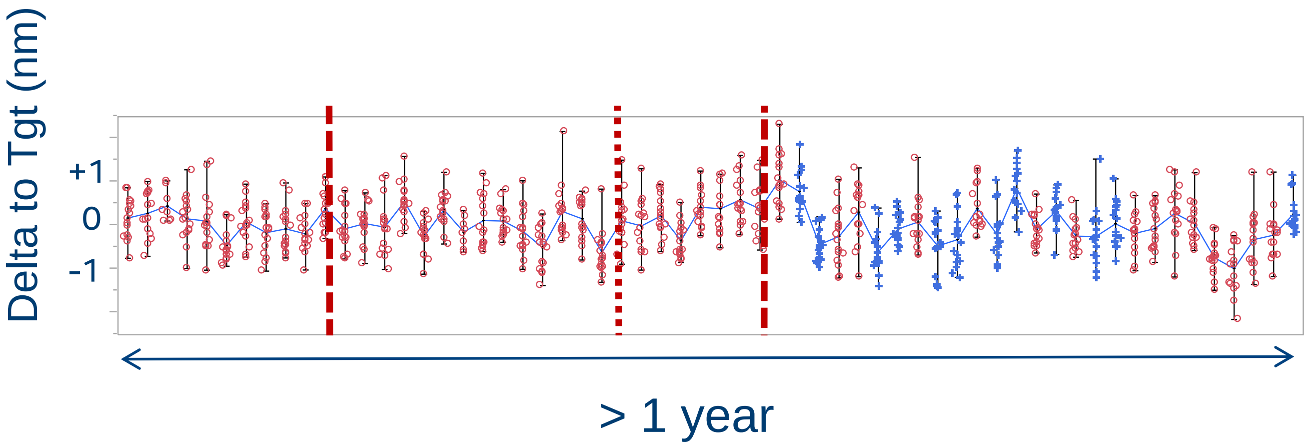


- No collector swap
- Collector degradation – shown by decreasing throughput as a result of reflectivity – follows roughly linear trend

Updated from 2016 SPIE

Intel's 14nm Pilot Line: CD trend





- Stable Via CD performance trend continues
- Introduction of a second tool within existing distribution

Overall exposure tool messages

- Source power
  - Source power continues to make progress and remains on track
  - Need to maintain exposure dose control
- System availability and demonstrated performance
  - Source remains largest contributor to tool down-time
  - Expect ongoing droplet generator developments to significantly improve availability
  - 13-week demo complete with scanner/source combined availability on target
  - 14nm pilot line CD performance stable longer than 1 year on multiple tools

★ Focus must remain on system availability – tools must be up to support technology development

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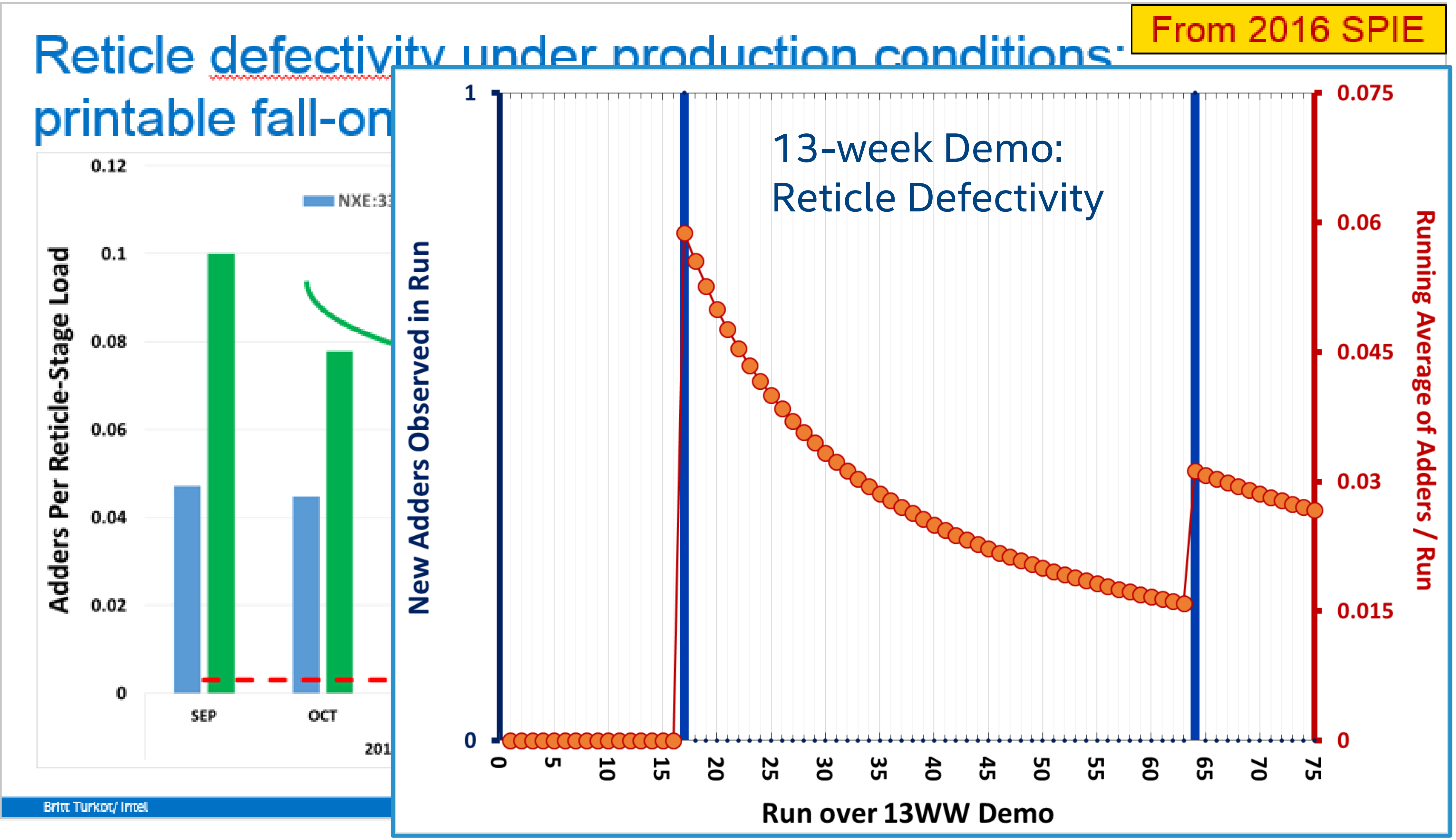
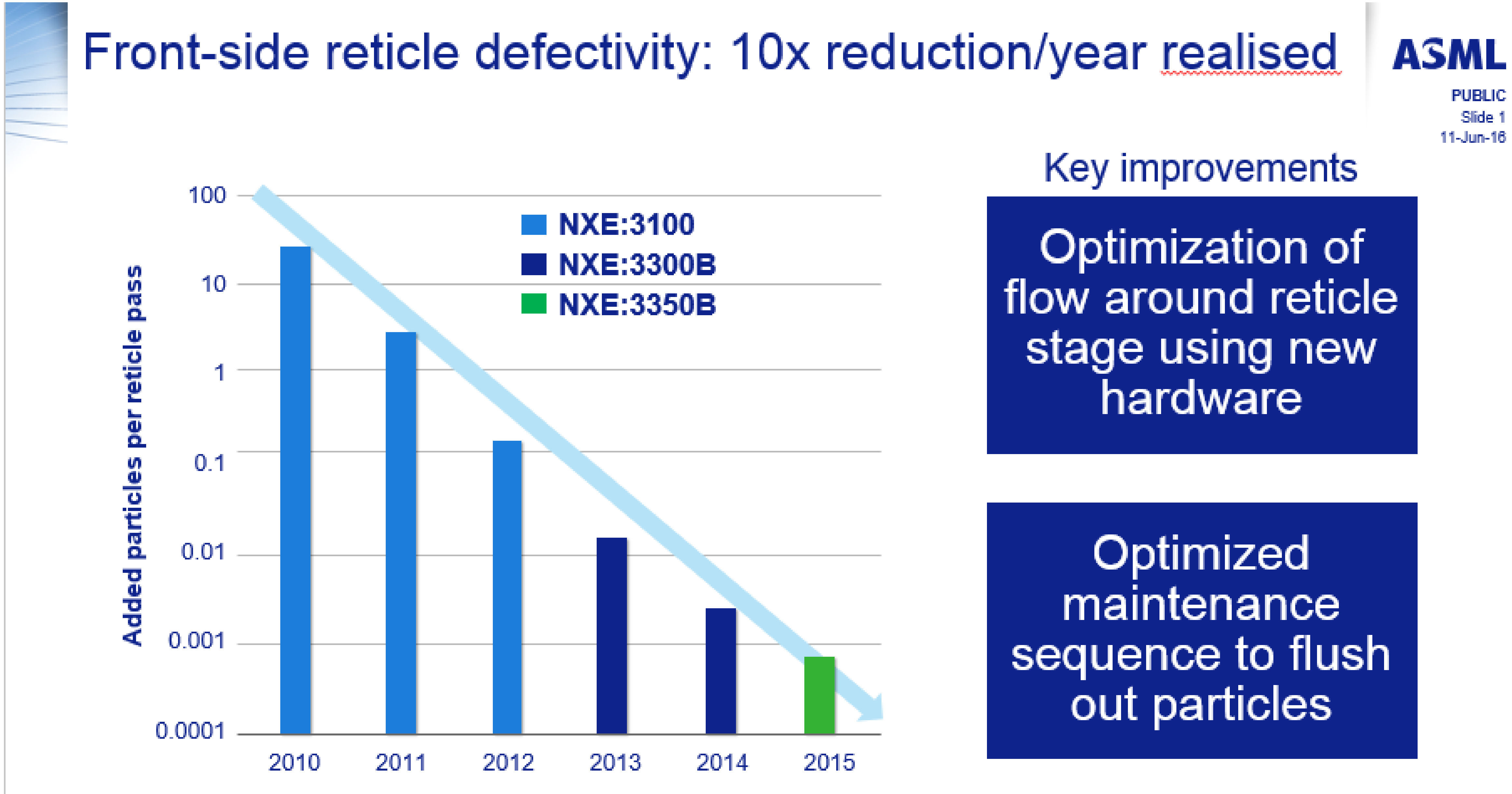
13-week Demo: Reticle Defectivity



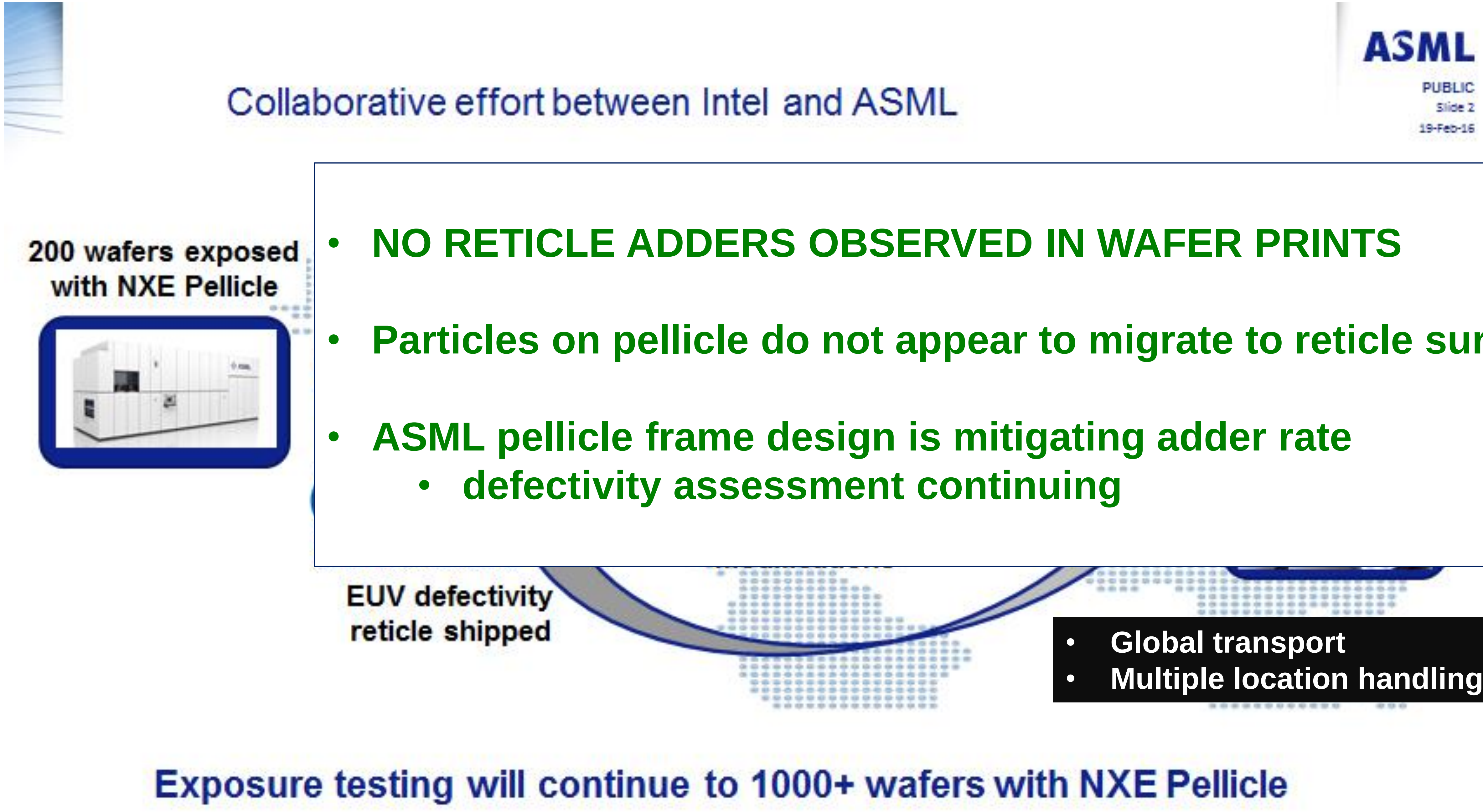
- Comparable results for printable reticle defects
- Mismatch remains between ASML added particle count and wafer print test

Reticle Defectivity Improvement Efforts



Even with defect reduction efforts, a pellicle is required to ensure yield

800 wafers exposed using reticle with 40W pellicle



- **NO RETICLE ADDERS OBSERVED IN WAFER PRINTS**
- **Particles on pellicle do not appear to migrate to reticle surface**
- **ASML pellicle frame design is mitigating adder rate**
  - **defectivity assessment continuing**

- **Global transport**
- **Multiple location handling**

Exposure effects on pellicle membrane

747 wafers exposed using 2 reticles and 5 pellicles (40W capable)
No change observed for EUV transmission and transmission uniformity

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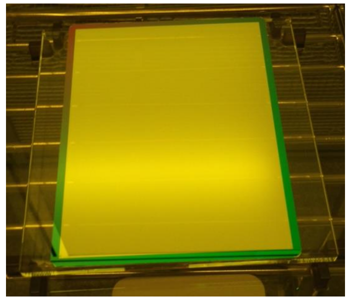
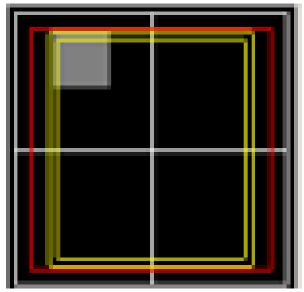
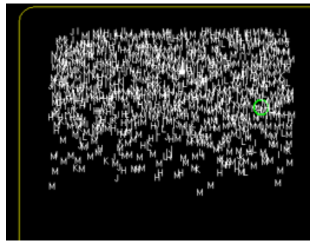
Pellicle	Reticle Repel operation =	Pre exposure measurement		Wafers exposed on NXE:3100	Post exposure measurement (200 wafers exposed)	
		EUVT [%]	Transmission uniformity [%]		EUVT [%]	Transmission uniformity [%]
1	Reticle 1	80.9	1.26	200	81.1	1.21
2	Reticle 1	81.5	1.25	200	81.7	1.72
3	Reticle 2	81.0	1.18	200	80.8	1.89
4	Reticle 2	81.0	1.36	147 – in progress		
5	Reticle 1	80.8	1.24	planned		

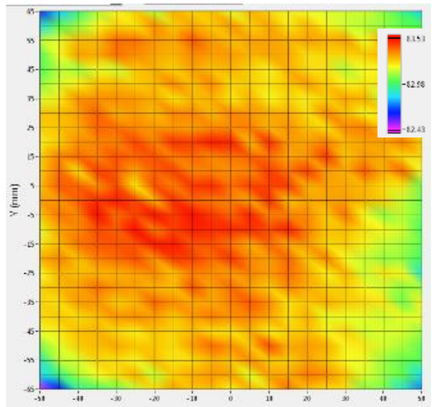
- Exposure testing will continue to 1000 wafers exposures with NXE Pellicle.
- Full pre-post analysis for pellicle films in progress
- New exposures underway using a 125W capable EUV pellicle on NXE:33X0B at ASML
  - Imaging results planned for BACUS

Pellicle development and infrastructure

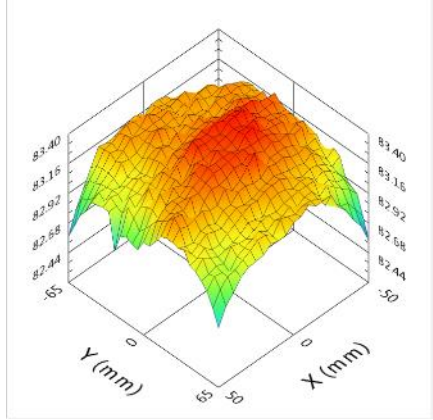
- Full field pellicle membrane exposed in the scanner
- Pellicle mounting and support tooling is being tested and made available to customers
- Pellicle defect inspection is under development

- Pellicle transmission measurement is available at tool suppliers

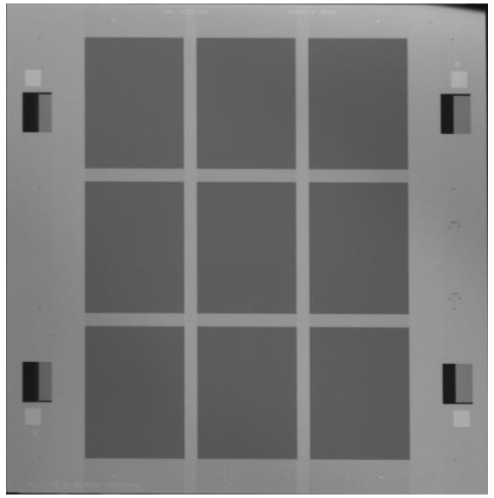


Measured in every 5mm

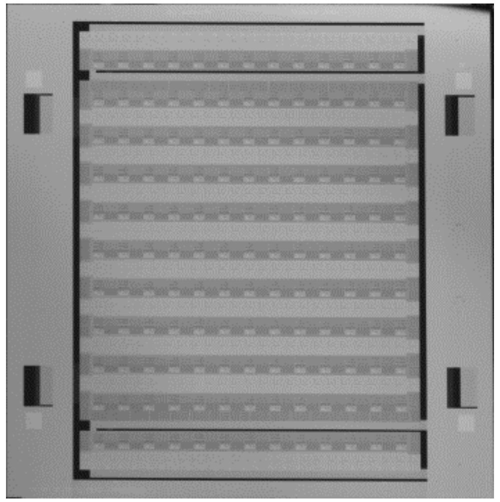


Courtesy of EUV Tech

Pre-pelliclized defectivity reticle



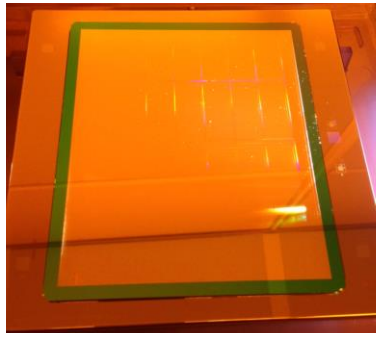
Pre-pelliclized imaging reticle

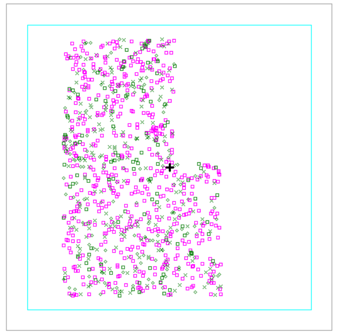


Pellicle membrane defects

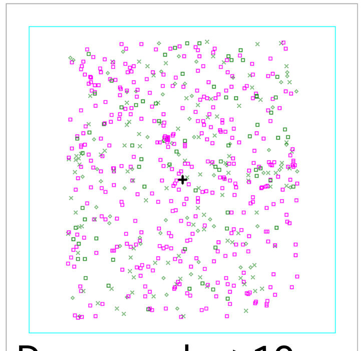
- Inspections done on three mounted pellicles
- All have high defect counts

Requirements for HVM:
- Improved defect levels
- Reliable supply chain
- Membrane material for high power
- Imaging performance

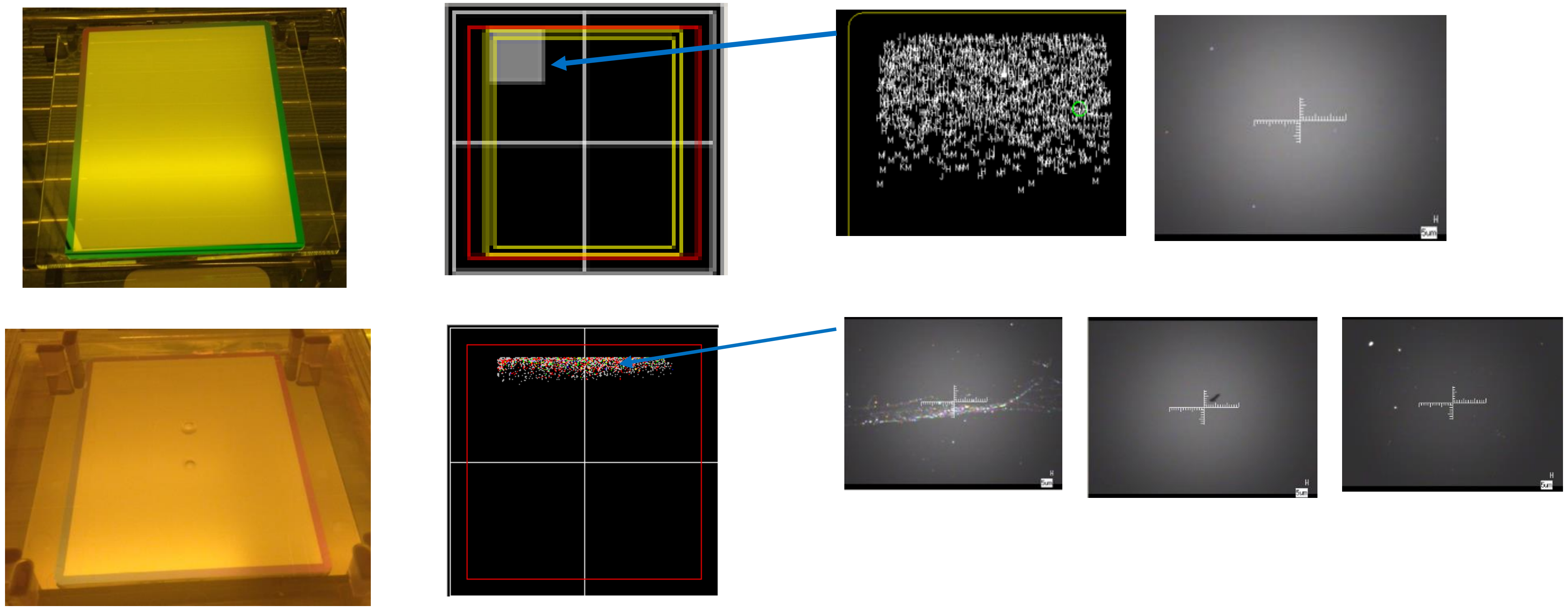


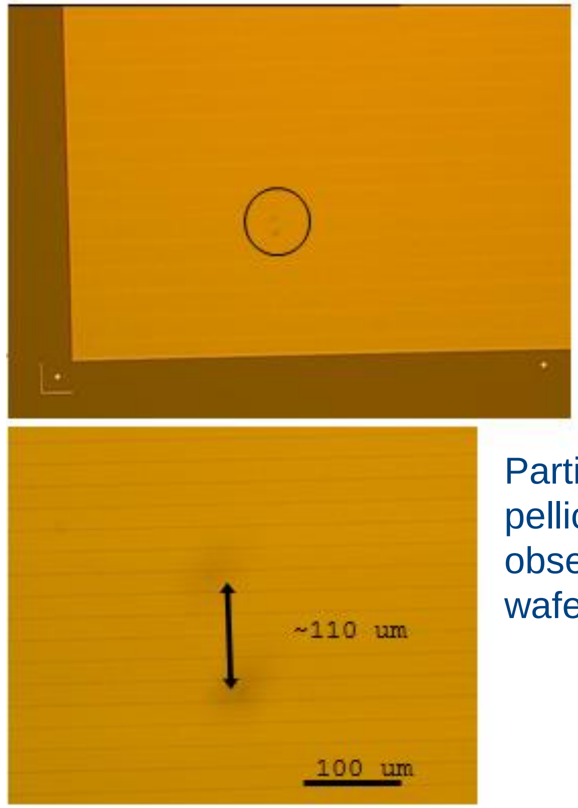


>1000 counts @>5um



De-sensed, ~>10um





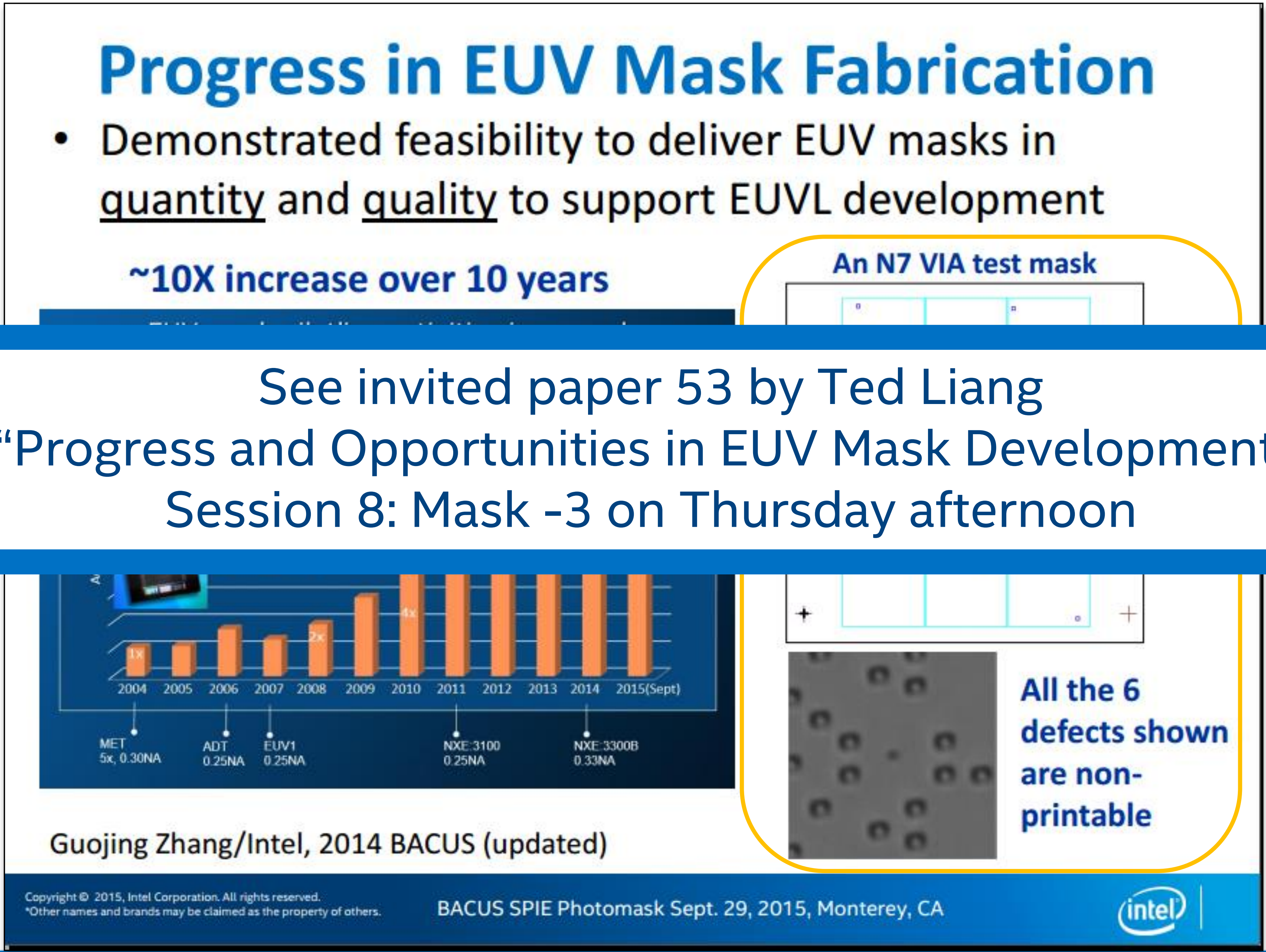
Particle on pellicle observed in wafer print

Updates from 2016 SPIE

Overall EUV pellicle infrastructure

- Basic tool capability exists today to support membrane materials development and quality control
  - Basic tool capability exists today for pellicle membrane defect inspection
  - Basic tool capability exists today for measuring pellicle membrane transmission uniformity accurately and precisely
- Demonstrated pellicle exposure with global transport and handling → 800 exposures with pellicle frame design mitigating adder defects
- Making progress with pellicle mounting tools → on track
- Availability of quality pellicle membranes is the highest risk to timely EUV pellicle implementation → remains high risk
- Inspection of pelliclized reticles is needed to ensure predictable yield. APMI is not a show-stopper, but without it yield and cost may be an issue.

Bottom line: N7 mask without repair: no printing defects

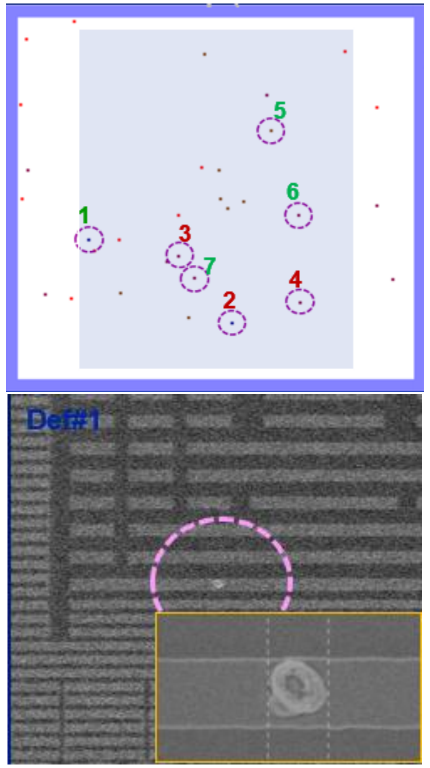


See invited paper 53 by Ted Liang
"Progress and Opportunities in EUV Mask Development"
Session 8: Mask -3 on Thursday afternoon

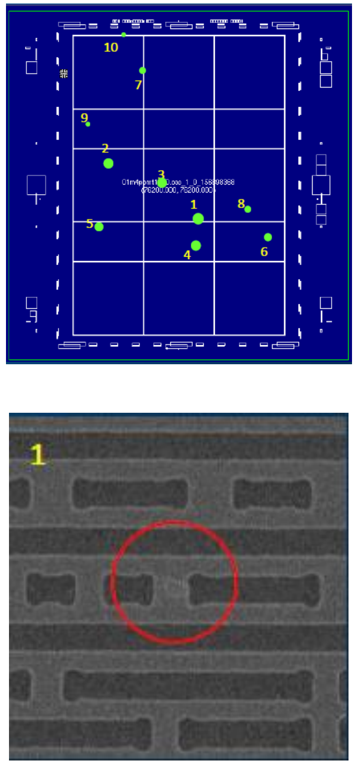
From 2015 BACUS

Defect mitigation demonstrated on multiple devices

- Many defects can be mitigated
- More defects can be covered on a dark field mask



7 mitigated
(22nm device, BF)



10 mitigated
(14nm device, DF)

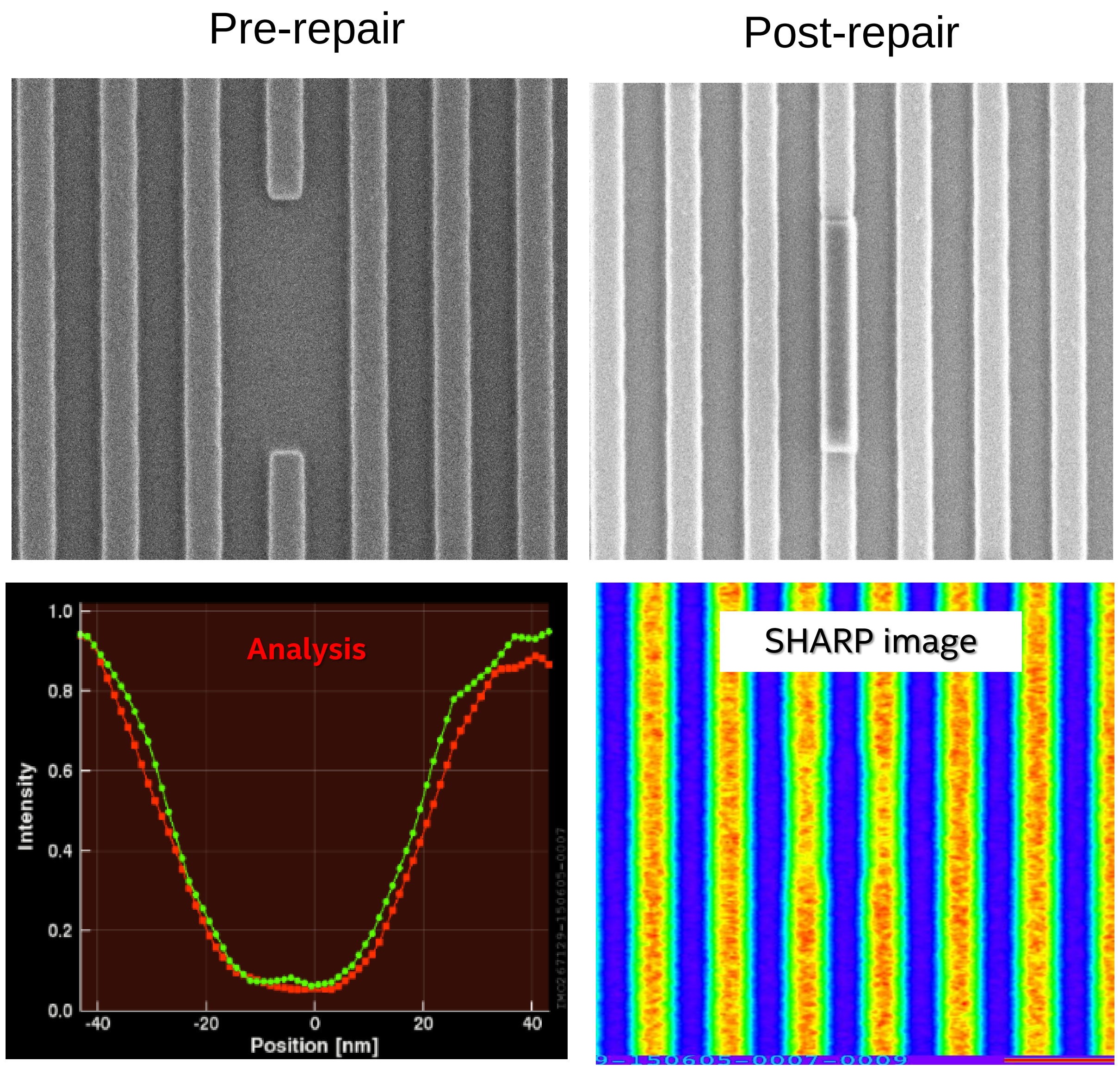
- **Mitigation flow**
  - Blanks with fiducials
  - Sort and pair blank with specific pattern layer
  - Pattern shift computations
    - These two steps require fast data automation
  - During write: accurate alignment
  - After patterning: AIMS verification

Foil from Ted Liang (Intel) et al. BACUS 2015, Monterey, California, USA, 9/29/2015

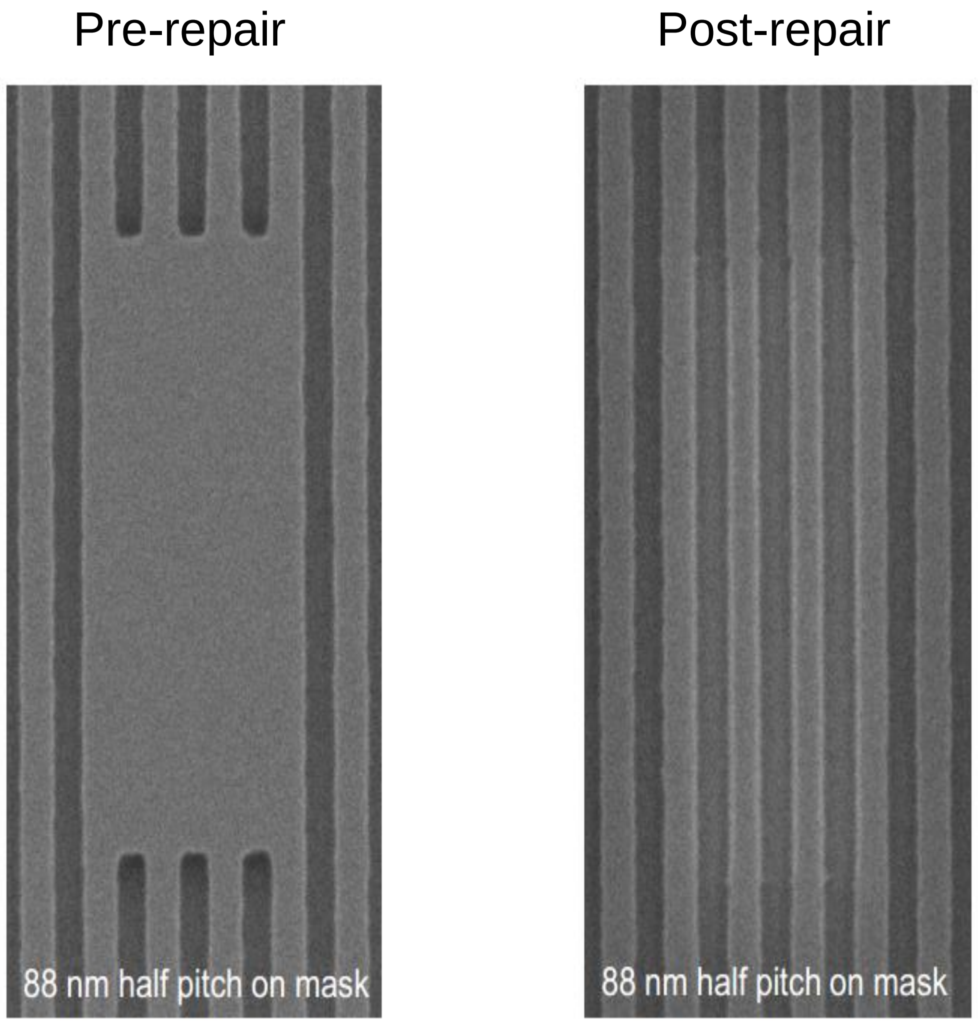
Complicated process to mitigate defects → continued blank defect reduction needed

From 2016 SPIE

E-beam pattern defect repair capability well-established



Patching repair



Cutting repair

From 2016 SPIE

Overall reticle messages

- Manufacturing
  - EUV reticle fabrication is maturing and matching to HVM
  - Stable EUV reticle performance has been demonstrated
  - Defect-free EUV reticles are achievable; yield improvement is a challenge
  - Defect mitigation process is well established, but it is not ideal due to process complexity and risks
- Materials
  - Defect-free blanks in volume need to be materialized for HVM
  - Progress has been made in pellicle material development, but slow and needs to be accelerated
- Tools
  - AIMS development is in the integration stage and needs to remain on schedule
  - Reticle defect inspection through pellicle requires a clear path for commercialization

★ Yield improvement, cost control, and ecosystem development remain the focus areas in EUV mask fabrication

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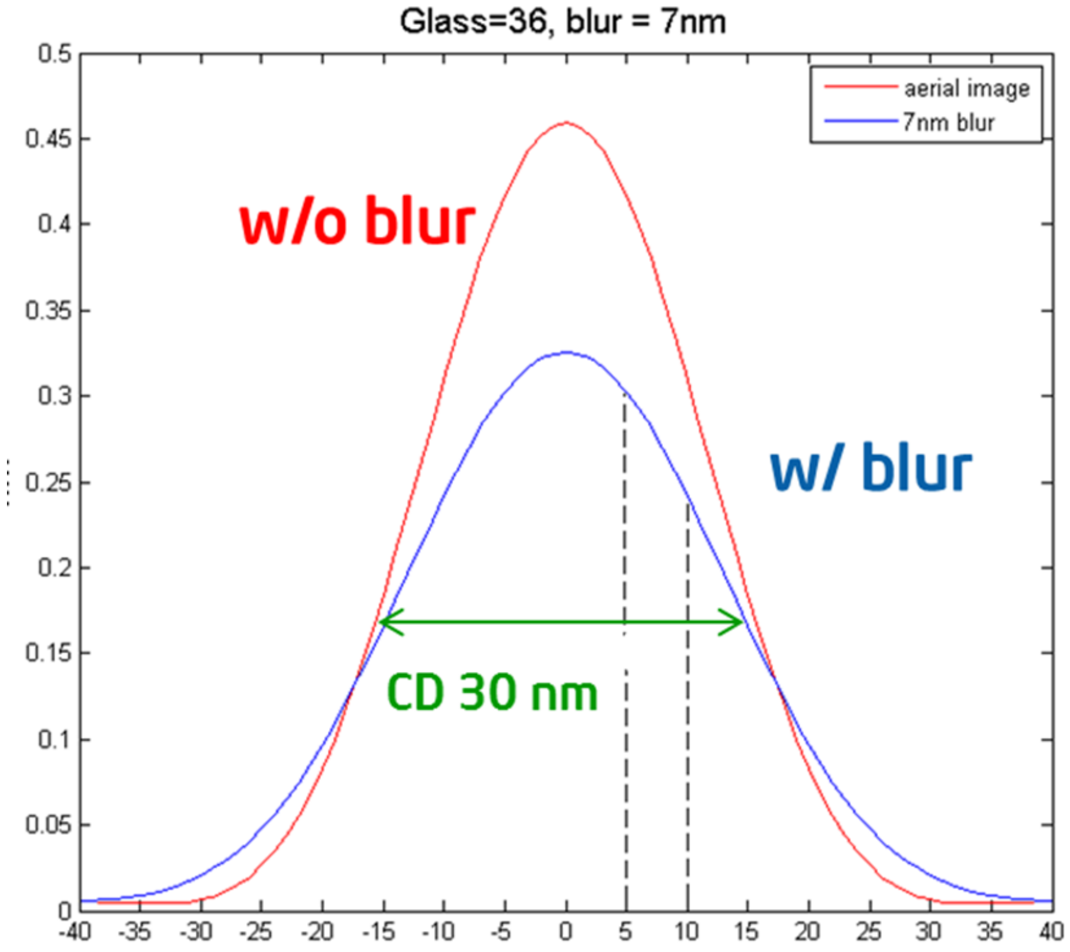
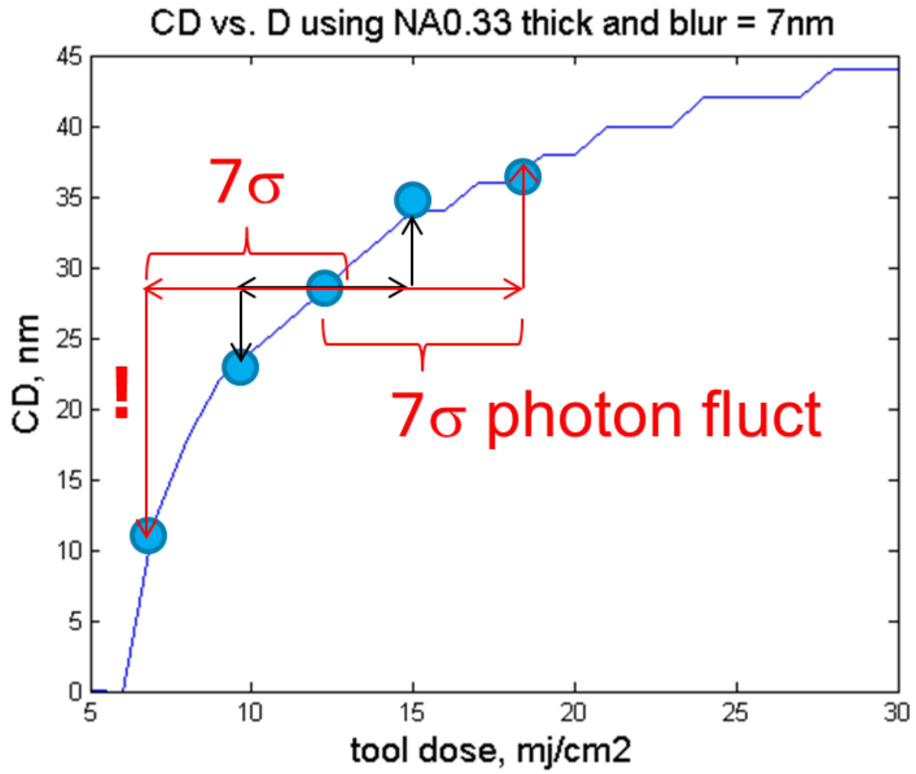
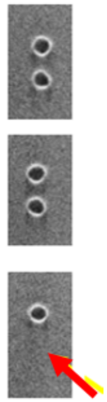
EUV Photoresists: The Photon Shot Noise Problem







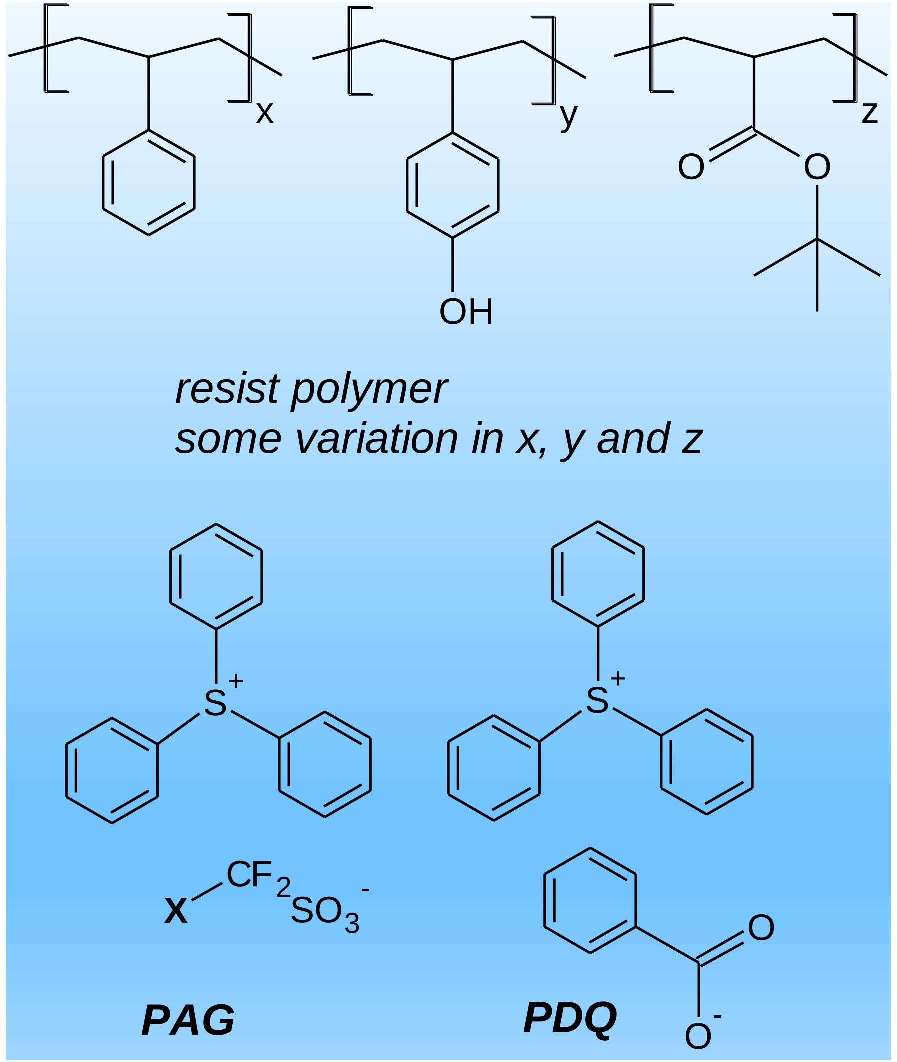
For 10^{10} contacts, some contacts will see 7σ fluctuations

High photospeed: Some contacts may not print at all

EUV Photoresists: The Resist Stochastic Problem

	24 nm hole	16nm hole
Incident photons	4610	2050
Absorbed photons in aerial image	700	215
N PAG (0.15/nm3)	3260	970
7σ PAG variation	26%	48%
N Quencher (1/5 PAG)	650	190
7σ Q variation	27%	50%

Assumes a dose of 15 mJ/cm2 and EUV Absorbance 5 /um



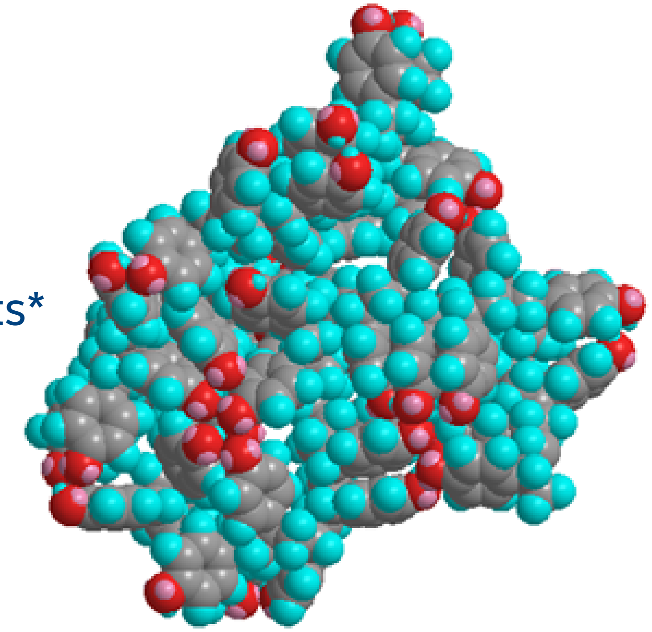
- Need thinner film thickness
- Large variations expected for PAG and quencher concentration
- Need to remove the sources of stochastic variation

Effect of Resist Structure on Stochastics

* Source IMEC 2016 PTW

Polymer acid amplified resists

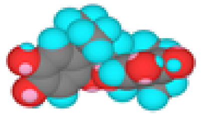
- EUV absorbance **5 /um**
- **More efficient:** ~2x more electrons per absorbed photon than inorganic resists*
- Multicomponent system (polymer, PAG, quencher)



~5nm
radius of gyration

Inorganic Nanoparticle Resists

- EUV absorbance **15 /um**
- **Higher absorption:** ~2x electrons per incident photon than EUV CAR*
- Single component system



1-2nm
Particle size

- Inorganic systems **absorb more** photons, but are **less efficient** in doing resist chemistry.
- Smaller size and single-component nature provide higher effective density of photon-absorbing sites
- Simple resist structure may improve resist stochastics

EUV Materials: next steps

We need to address all sources of stochastic variation in resists

- High EUV absorption
- High efficiency in utilizing absorbed photons and facilitating resist chemistry
- Random mixing of resist components can lead to significant resist component noise

→ **A Mechanistic understanding of novel resists is key to assess resist stochastic benefits**

- In nanoparticle resists, what causes solubility switch, what is the analog of PAG / quencher?
- With higher absorption, why do nanoparticle resists require high dose?

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What gates EUV implementation in HVM?

Judged as of today

- EUVL is highly desirable for the 7nm node but will only be used when it is ready
- Technology Development requires rapid information turns
  - Availability: tools must be up to run TD wafers without delay – This remains the critical, gating concern today
- HVM requires reasonable COO and predictability, driven by:
  - Productivity (mostly source power) – Good progress
  - Availability (mostly source availability) – Long way to go, but demonstrating progress
  - OpEx (mostly source consumables) – Long way to go, but demonstrating progress
- HVM requires confidence in yield, driven by:
  - Mask (blank and manufacturing) defects and mitigation – Demonstrating good progress
  - Pellicle readiness – Long way to go, but making progress
  - Mask pattern defect detection (manufacturing and fall-on particles) – Need actinic solution for long term
  - Materials performance – Won't gate introduction of EUV, but need to improve stochastics for long term

Acknowledgements

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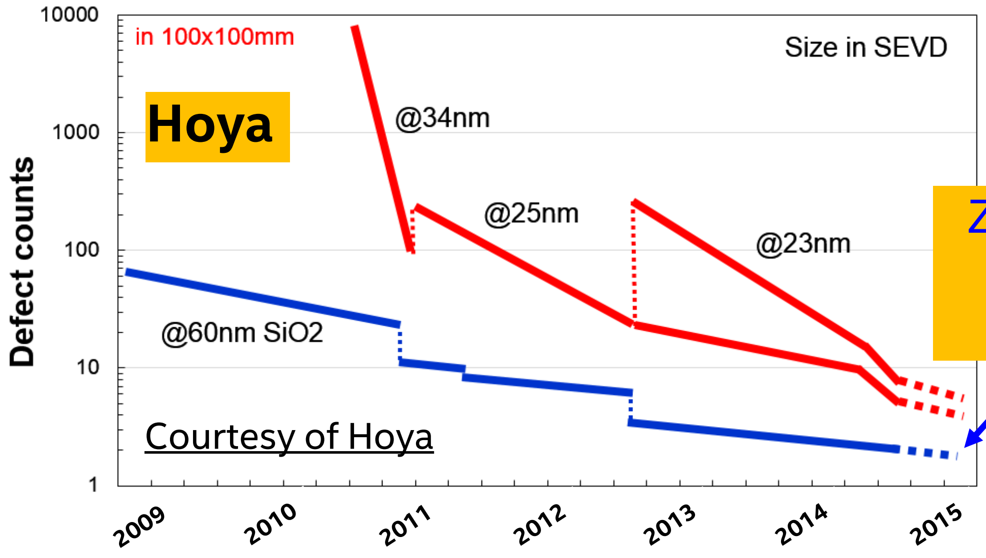
Jeff Farnsworth (Intel)
Sang Lee (Intel)

Dan Smith (ASML)

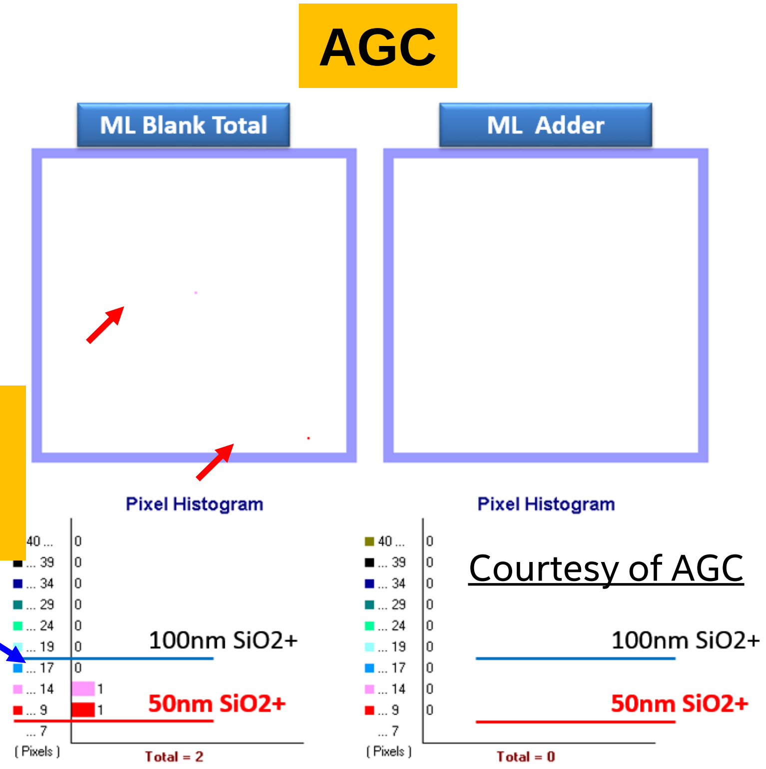
Backup

EUVL mask blank ML defect trend

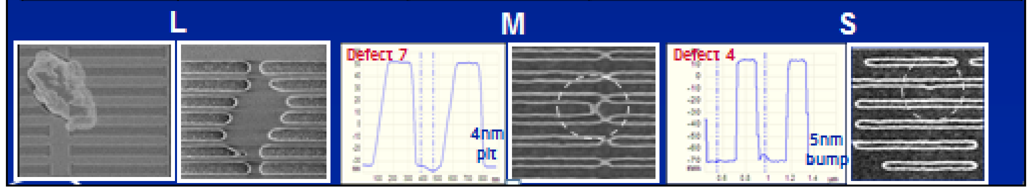
- Blank quality continues to improve
  - Defect # in single digit on best blanks
  - Large defects mostly eliminated on quality blanks



Zero large defects possible



Bin	Relative Size	Impact	Goal : Solution
Large	> hp	Killer	Elimination
Medium	≈ hp to ½ hp	Killer to ΔCD	Elimination + reduction : Mitigation
Small	≈ < ½ hp	ΔCD	Reduction : Compensation



Analysis presented at EUV Symp 2011, still true today

- Blank quality for patterning tighter pattern layers
  - Eliminate ML defects > hp; difficult to covered by absorber
  - Reduce ML phase defects; become printable, require actinic blank inspection

Foil from Ted Liang (Intel) et al. BACUS 2015, Monterey, California, USA, 9/29/2015

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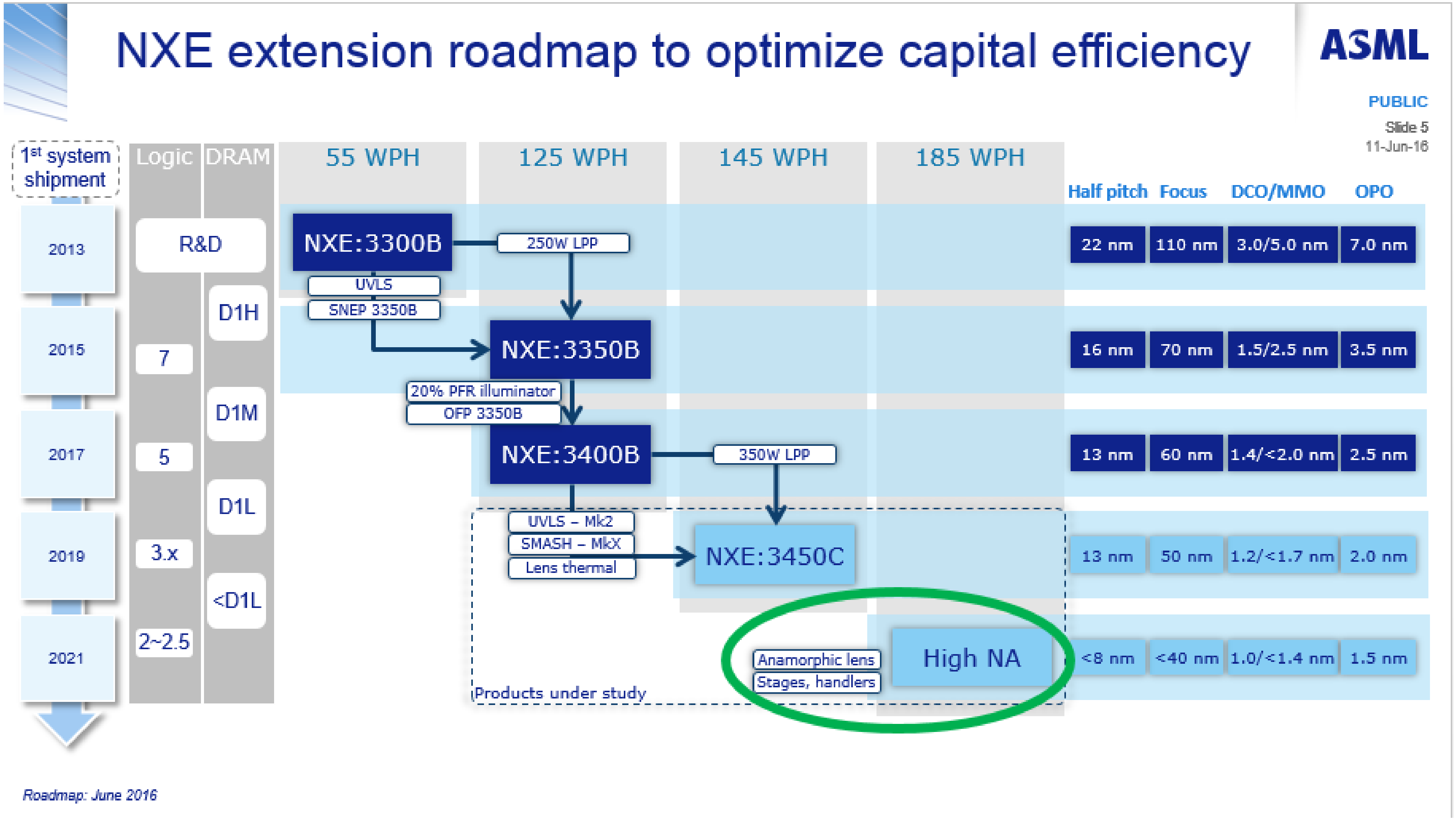
EUV Extension: High NA



EUV Extension: High NA