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Stochastic investigation of the impact of absorber variations on wafer patterning

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Outline

- Overview of development DTCO process
- Historic perspective: process variability bands and lithography print simulations
- EUV considerations for DTCO development
- Mask process interactions in DTCO flows
- Impacts of OPC dissection choices on resist patterns
- Summary

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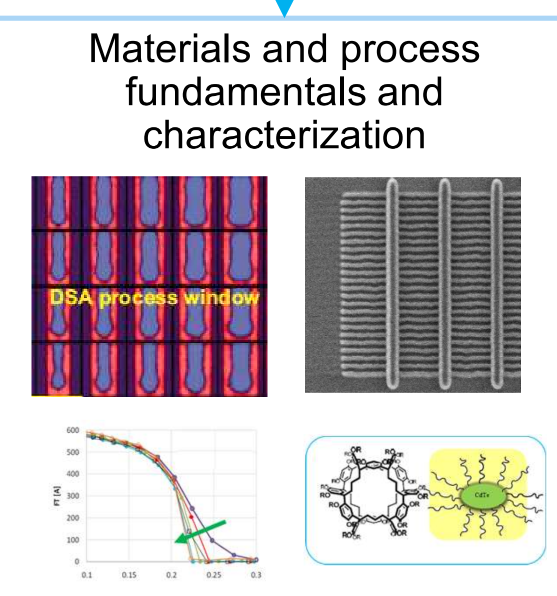
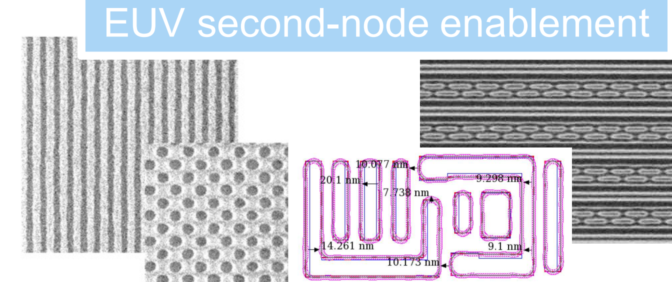
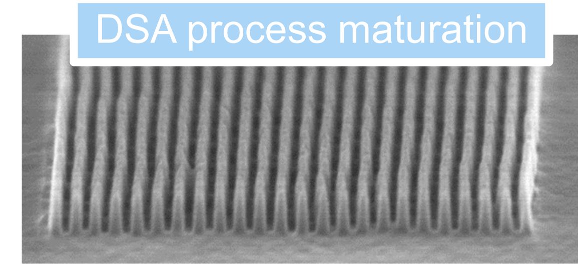
Materials and process fundamentals and characterization



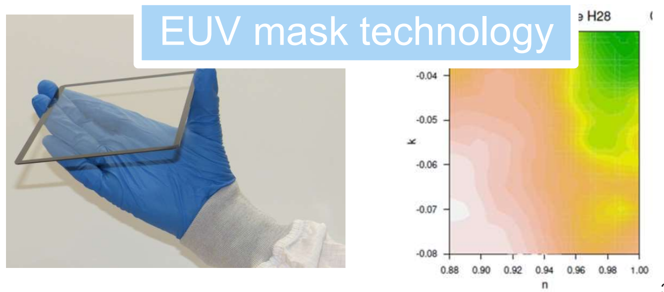
EUV second-node enablement



DSA process maturation



EUV mask technology



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RET & DTCO Flow: Design Arc Methodology

Development DTCO: identify initial design arc

Device
Design
RET Selection
Inputs:
• n-1 wafer data.
• Current scaling targets.
• Device "must-haves".
• Process assumptions.
• Process marginalities.
Integration
Process
Ground Rules DTCO
OPC Models
Litho/Etch Process Dev
OPC/ORC
Wafer Learning

Goal:
- Identify competitive design arcs early.
- Explore arc content on wafer as early as possible
- Iterate based upon electrical and process feedback.

Design arc wafer learning & down-select

Possible Technology Definition

Output:
- Unit process structural analysis.
- Input to eco-system vendors on requirements for materials tools.
- Early feedback to design and integration team.
- Jump start new technology ramps.

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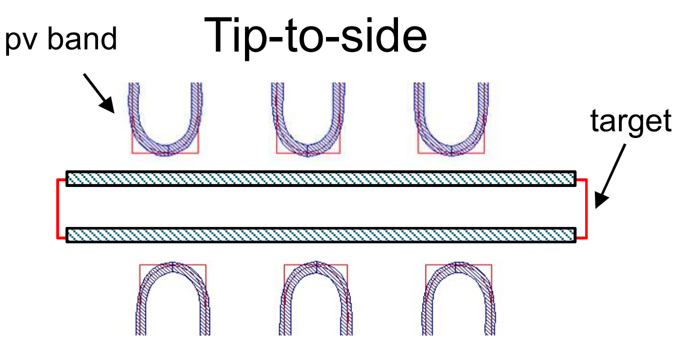
Historic Design Arc Definition: PV- Bands



Tip-to-tip

etch
contour

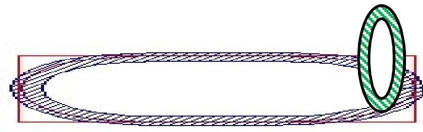
Orthogonal contacts

Staggered contacts

Methodology:

- Automate construct generation.
- Simulate process variability bands using variations in mask size, dose, and focus
- If PV band exceeds threshold, construct is disallowed.
- Over time, began to add multi-layer area overlap, post-etch contours, additional unit process biases

Multi-level contact area



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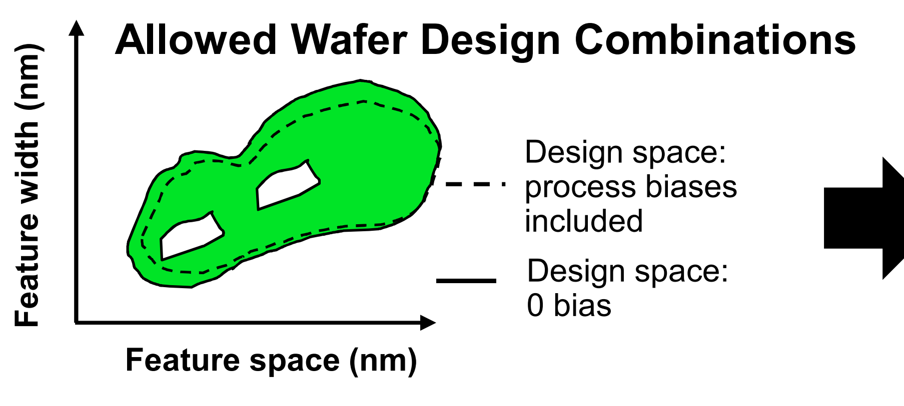
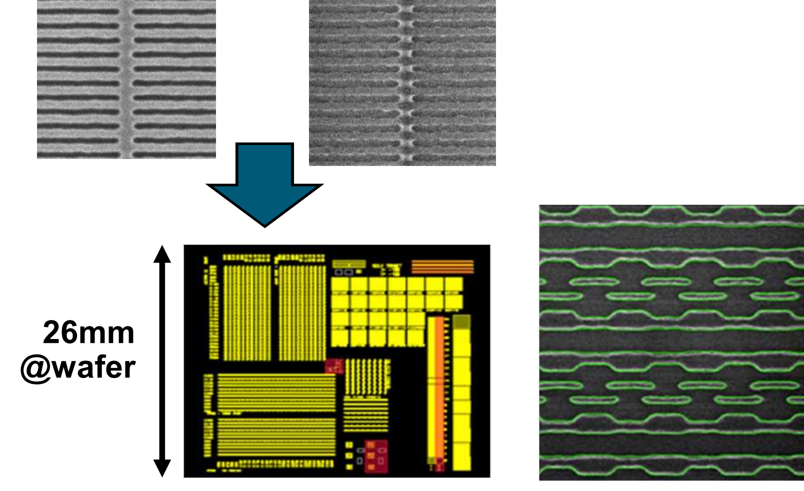
Historic Design Arc Definition

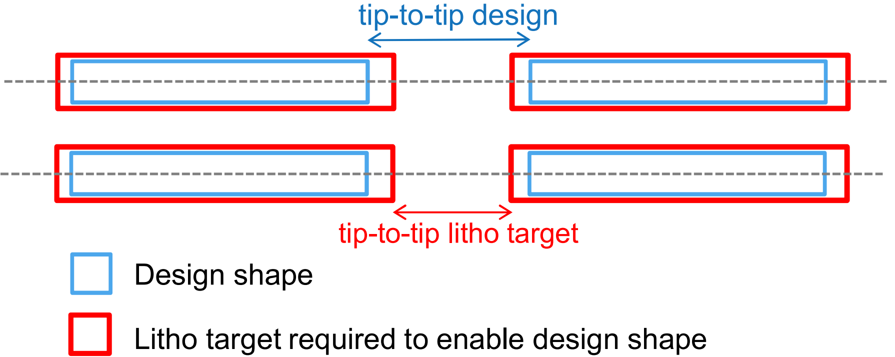
Allowed Wafer Design Combinations



Construct exploration enables technology



Design space limiting factors



Goals

- Explore design styles
- Process space
- Improve boundaries of design space through cycles of learning

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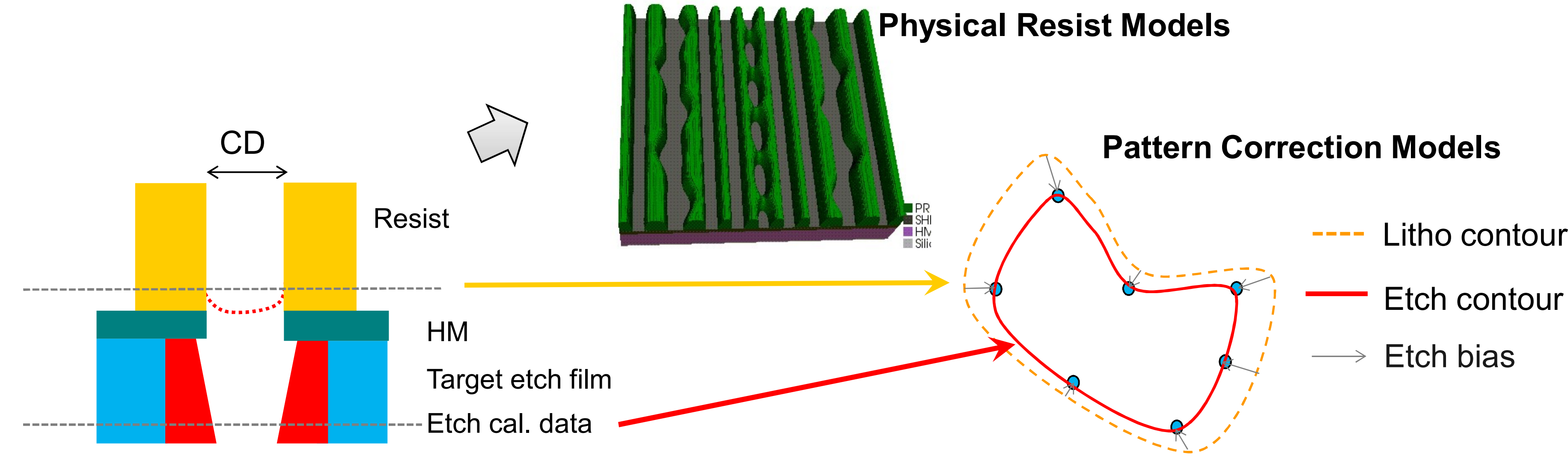
Extend 2D Arc Definition to 3D



- Assumes that PV-bands accurately represent process variability
- Implicitly, we are capturing 3D effects in 2D
- Remarkably compact and efficient for direct print levels
- Hidden aspects for some process limiting effects:
  - Resist top-loss
  - Profile angles and sidewall variation

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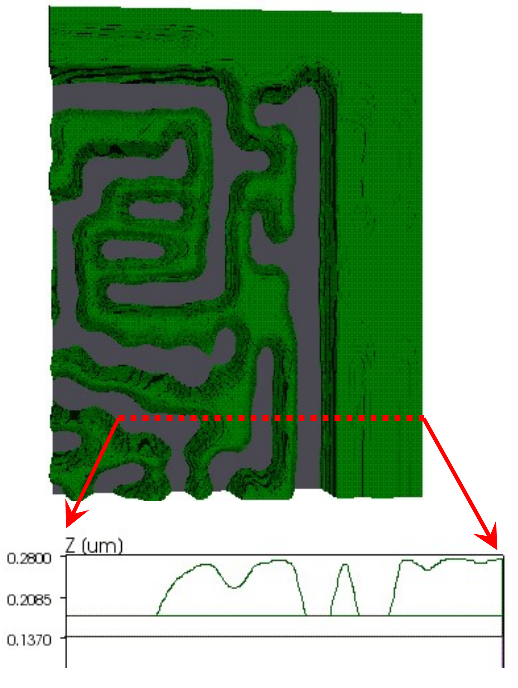
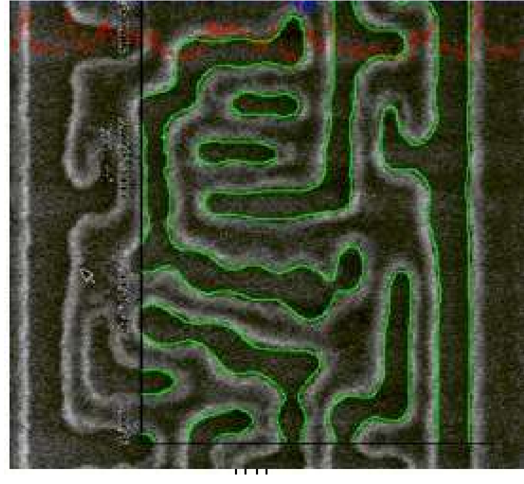
3D Features of Patterning are Increasingly Important

3D Resist Profile Simulation



2D resist profile: out of wafer plane



2D resist contour overlay on SEM image

Observations

- As feature density increases, 3-D resist effects impact ability to transfer patterns to hardmask stacks
- Impacts profiles transferred to hardmask stacks due to resist profile variation
- Required additional analysis out side of PV band simulations to assess risk

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EUV Challenges to PV-Band Methodologies

EUV challenges for design arc analysis:

- Resist systems are thin relative to previous generations
- Etch processes need to be selective to resists
  - Scumming → pattern transfer problems
- Noise impacts on profile roughness
- Secondary electron effects can blur chemical gradients in resist
- Mask process challenges driven by scaling

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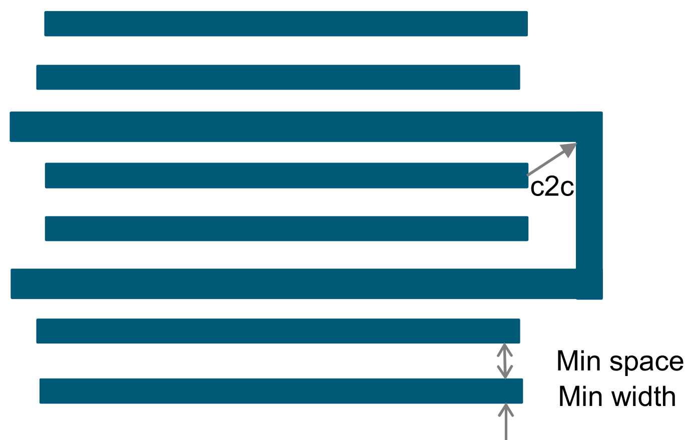
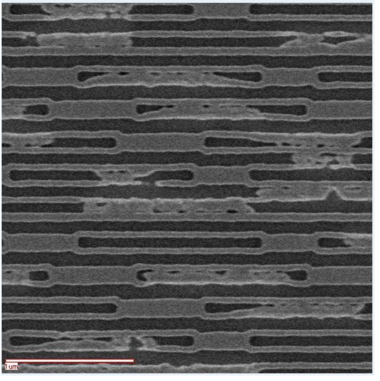
EUV Challenges: Mask Process Awareness

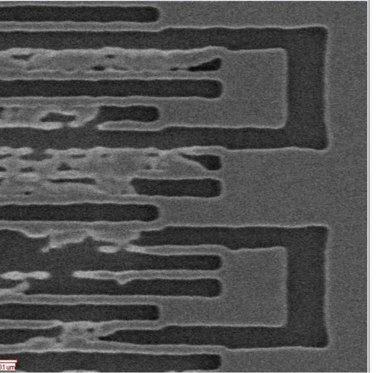
- Early in development, critical processes are not optimized
- Awareness of process capabilities needs to extend to mask process
- Traditional mask rule constraints are likely not sufficient to enable early design arc definitions
- Need to develop mask process aware RET selection and OPC flows

Layout schematic: expected to transfer to mask



Line and space mask process challenges





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EUV Challenges: Mask Process Awareness

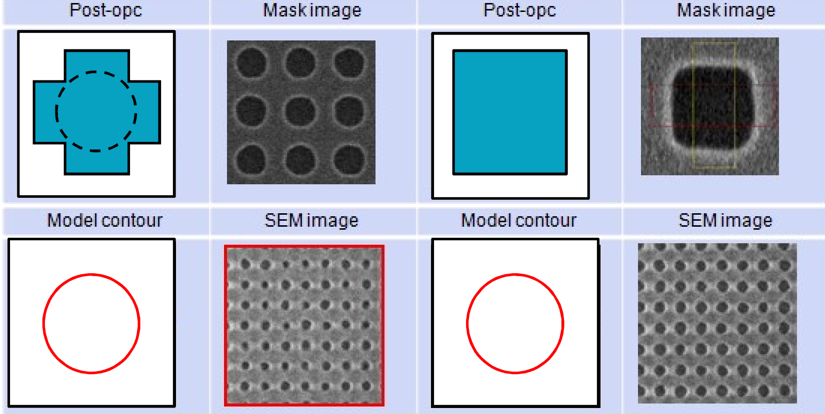
Contact example

- Early in development, critical processes lag
- Traditional mask rule constraints are likely not sufficient to enable early design arc definitions
- Need to develop mask process aware RET selection and OPC flows

Contacts:

- Min pitch contact arrays used re-entrant OPC to meet MRC
- Mask shapes transferred as inscribed circular shapes
- Difficult to center full pitch range

Contact and via mask process challenges



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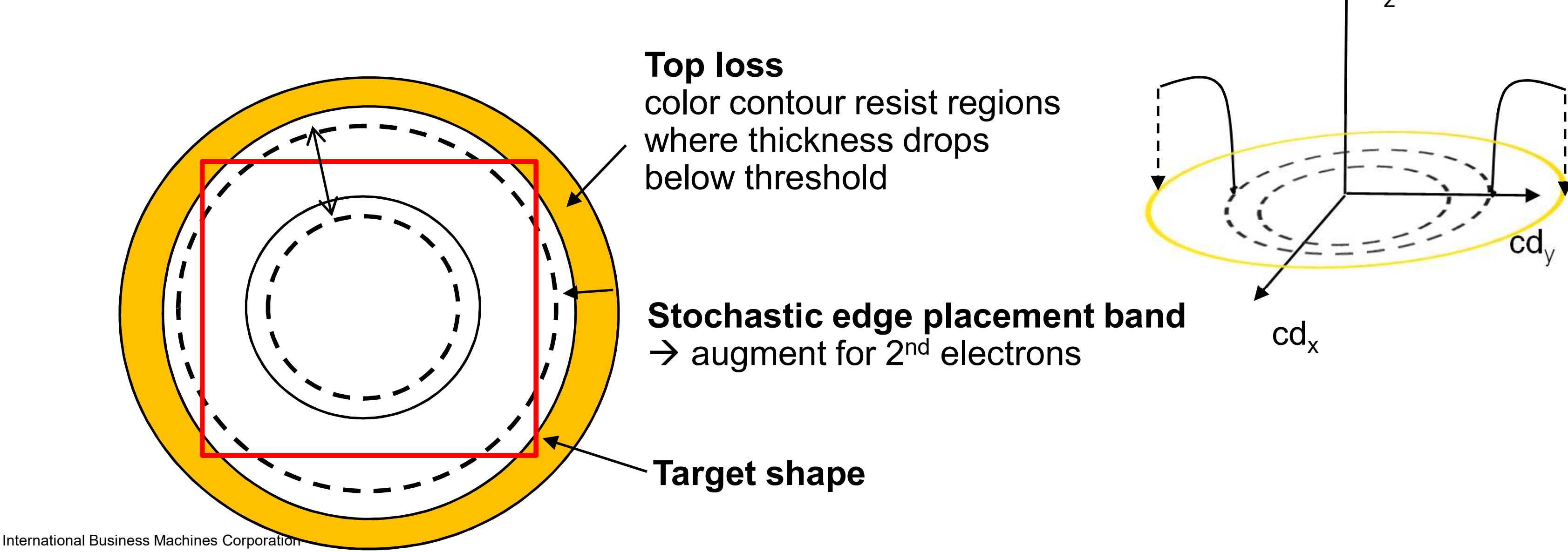
Proposed EUV Adjustments to PV-Band Metrics

- Nothing inherently wrong with PV bands, but need to identify right surfaces to derive them
- Capture EUV sources of variation:
  - Stochastic effects from EUV photon-resist interaction.
  - Impact of secondary electrons on NILS– broadening in PV band
  - Resist top-loss – second contour formed by projecting resist thickness below threshold into plane of design
  - Mask process constraints on OPC



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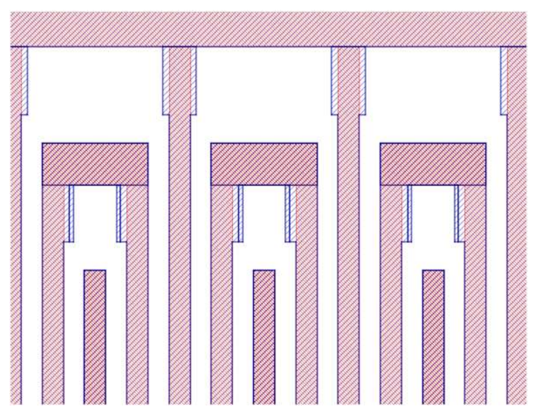
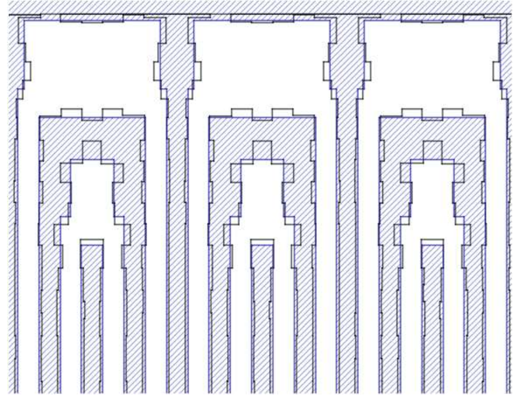
Proposed flow: include mask process models in patterning simulations

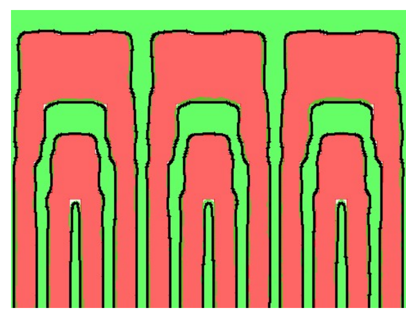
Retarget design for process biases



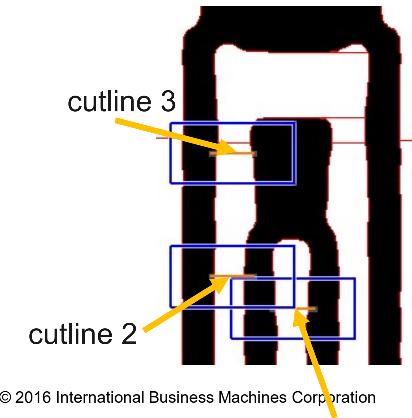
OPC with/without retargeting



Apply mask process correction model



Pvband, physical lithography simulations



Proposed flow:

1. Retarget to mitigate process biases
2. Explore OPC parameters with and without retargeting
3. Apply mask biases to post OPC output
4. PVBand analysis
5. Physical patterning simulations simulation
6. Stochastic patterning simulations
7. Construct assessment

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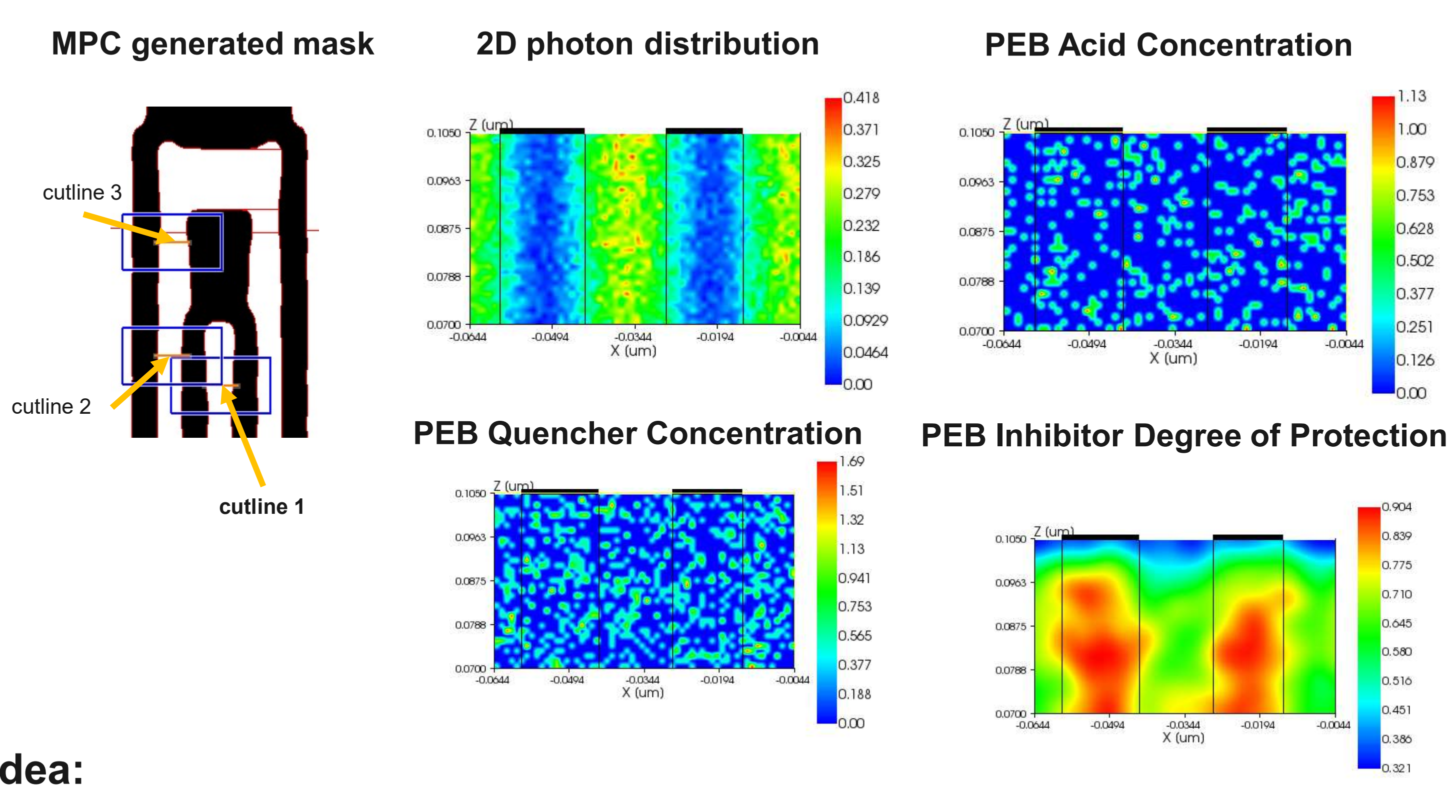
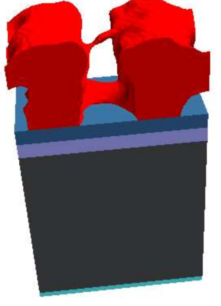
Add stochastic lithography simulations pv band analysis



3D Resist Profiles



Idea:

- Explore impact of mask process and OPC choices on process variability
- Physical simulator to explore snapshot profiles and statistical excursions

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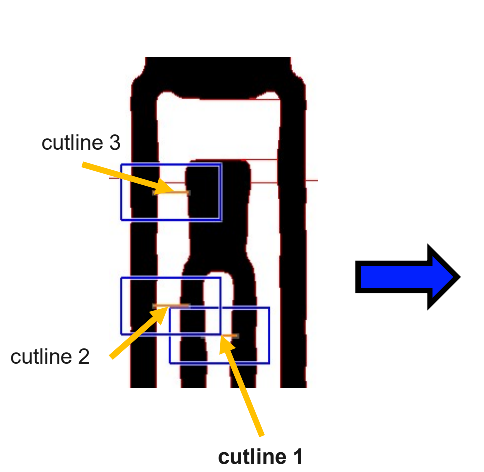
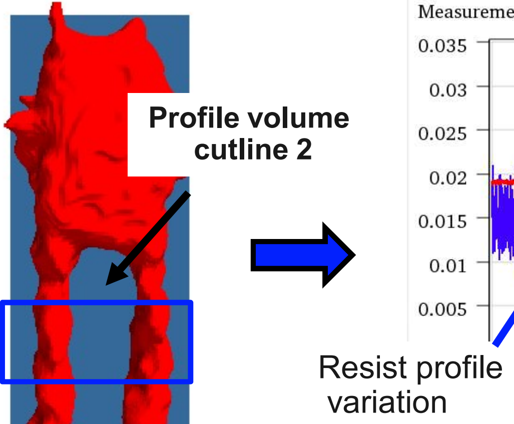
Stochastic simulations

MPC generated mask



Mask

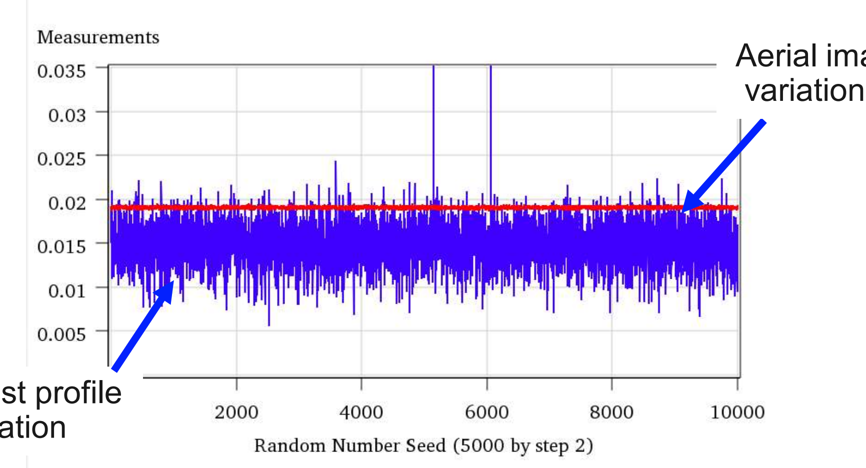
- Use PV bands & wafer data to identify potential hotspots
- Construct metrology volumes



Profile

- Generate resist profiles in hotspot volume
- Identify max allowed profile deviations

Stochastic simulations from volume



Statistic Information

RMS	Mean	St.Deviation	Min	Max	Median	Data
0.01521	0.01501	2.45084e-03	5.69007e-03	0.05039	0.01513	0.01501 ± 0.00006
0.01911	0.01911	1.04955e-04	0.01875	0.01953	0.01911	0.0191 ± 2.4e-06

Stochastic analyses

- Run stochastic simulations over meaningful number of trials
- Identify number of resist profiles that exceed a threshold excursion i.e. min width, min space, etc
- Count number of excursions above threshold as trial fails

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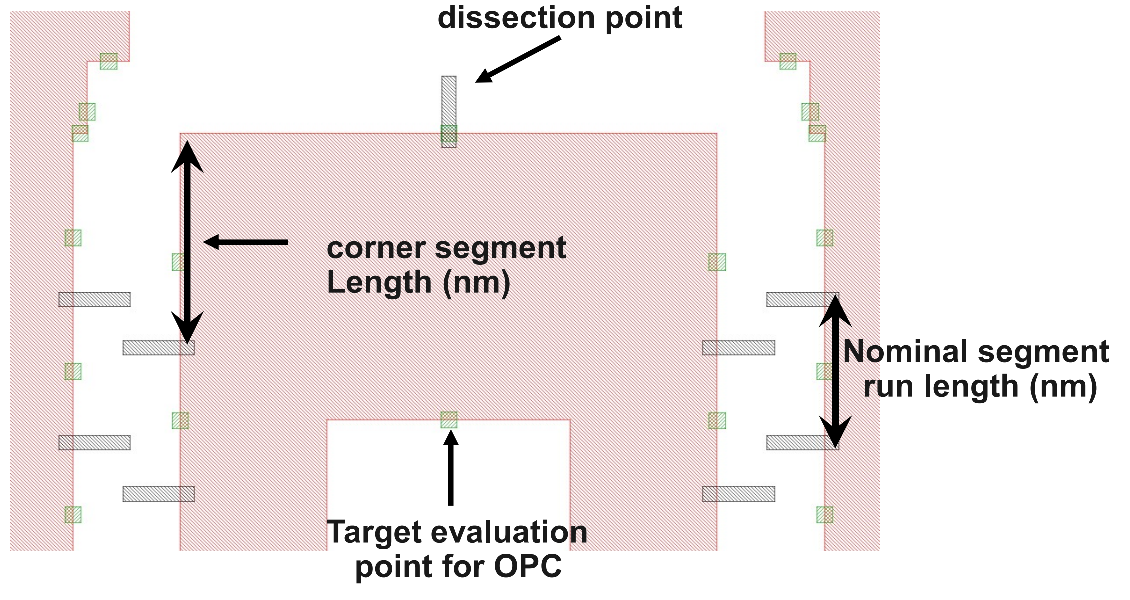
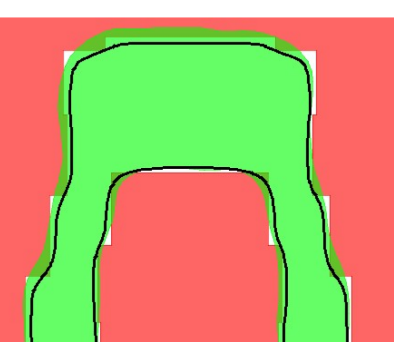
Exploring the interaction of retargeting and OPC dissection with MPC

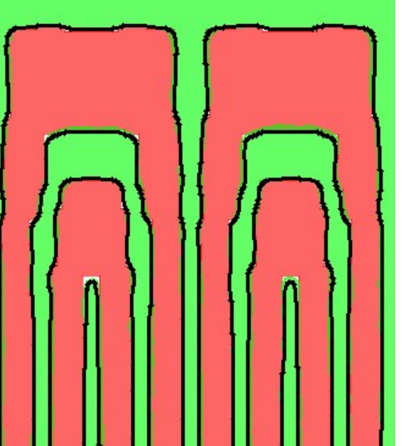
Layout dissection and evaluation point placement

Mask model applied to post-OPC shapes





Mask model applied to post-OPC shapes



Method:

- Explore retargeting vs as designed
- Change OPC dissection and target strategy
- Apply mask model to post-OPC shapes
- Use mask contours in stochastic simulations

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Cutline 1 stochastic simulations

Nom Seg (nm)	Cor. Seg (nm)	Cor targ offset (nm)
12	12	12
16	24	18
20	30	18

Standard

Retargeted

cutline 3

cutline 2

cutline 1

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Cutline 2 stochastic simulations

Nom Seg (nm)	Cor. Seg (nm)	Cor targ offset (nm)
12	12	12
16	24	18
20	30	18

Standard

Retargeted

cutline 3

cutline 2

cutline 1

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Cutline 3 stochastic simulations

Nom Seg (nm)	Cor. Seg (nm)	Cor targ offset (nm)
12	12	12
16	24	18
20	30	18

Standard

Retargeted

cutline 3

cutline 2

cutline 1

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Results

- PV band and stochastic PV band methods are inherently blind to interactions of OPC with mask process effects
- Strong dependence of failure relative frequency on OPC dissection and evaluation point strategies
- Retargeting to mitigate downstream unit process biases does not necessarily result in lower EUV hotspot relative frequency → need to consider carefully interaction of dissection and mask process interaction
- Interactions of local construct environments with retargeting, OPC dissection and targeting need to be considered carefully to minimize relative frequency of hotspots.
- Including mask process awareness and stochastic simulations in DTCO flow will enable finer grained design arcs → more competitive development design arc definition

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