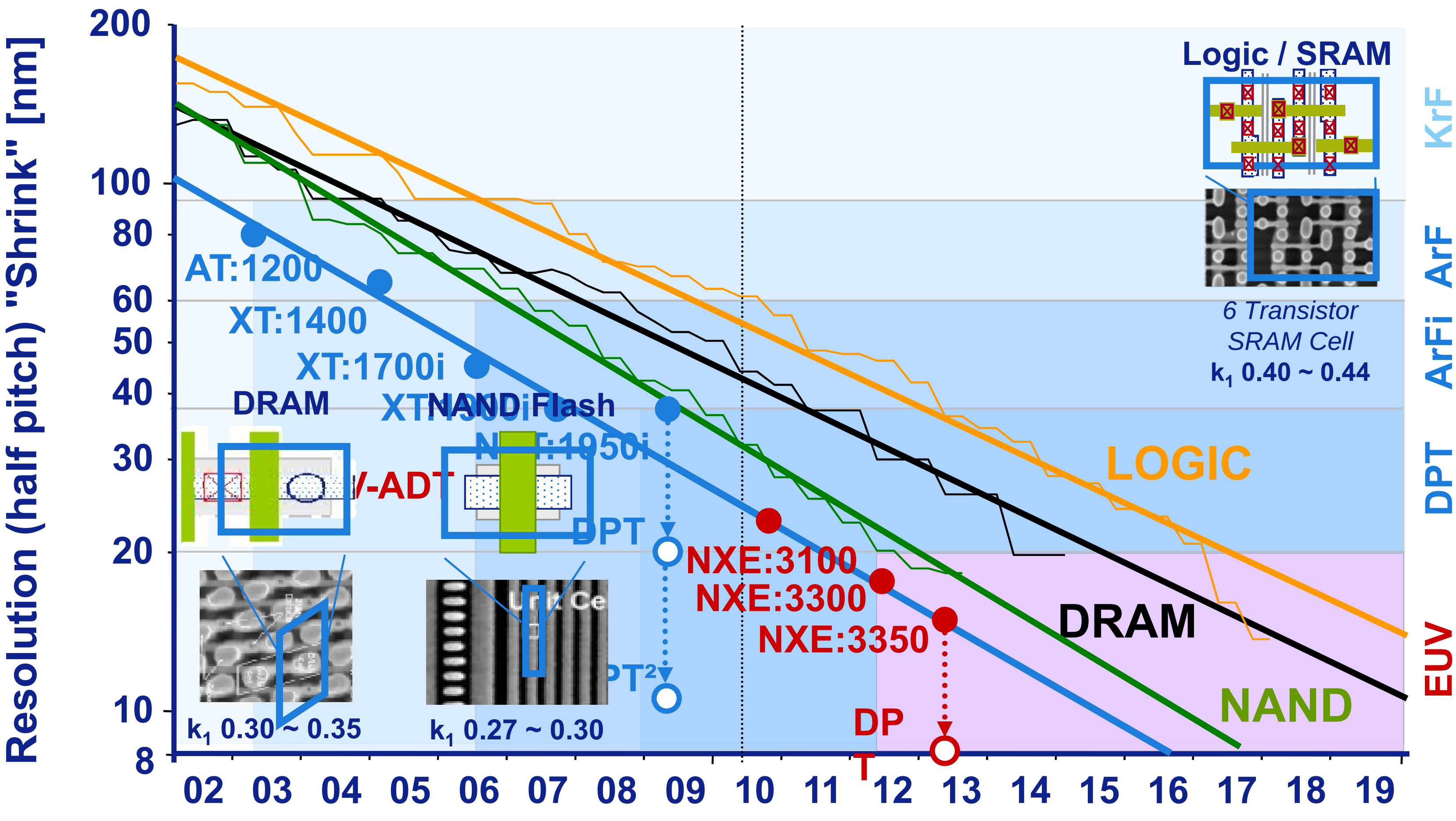
EUV: Status and Challenges Ahead
International Workshop on EUVL, Maui 2010

Jos Benschop

Agenda

- Roadmap
- Status
- Challenges
- Summary & conclusion

IC & Lithography roadmap towards <10nm



Source: Customers, ASML, 05/10

Notes:
1. R&D solution required 1.5~ 2 yrs ahead of Production
2. EUV resolution requires 7nm diffusion length resist
3. DPT = Double Patterning

Likely lithographic options

k_1 = (half-pitch) * numerical aperture / wavelength

- Most likely
- Opportunity
- Challenge

Half pitch (nm)		65	45	32	22	15	11	7	5
	Year	2005	2007	2009	2011	2013	2015	2017	2019
λ (nm)	NA								
193	0.93	0.31							
	1.20	0.40	0.28						
	1.35		0.31	0.22	0.15	0.10			
13.5	0.25				0.41	0.31			
	0.32				0.52	0.36			
	0.45					0.50	0.37		
	0.70							0.36	0.26

Double (Double) patterning, DP: CoO challenge

DP, $k_1 > 0.125$

DP², $k_1 > 0.0625$

Low $k_1 > 0.25$ challenge

Infrastructure challenge

6.8nm?

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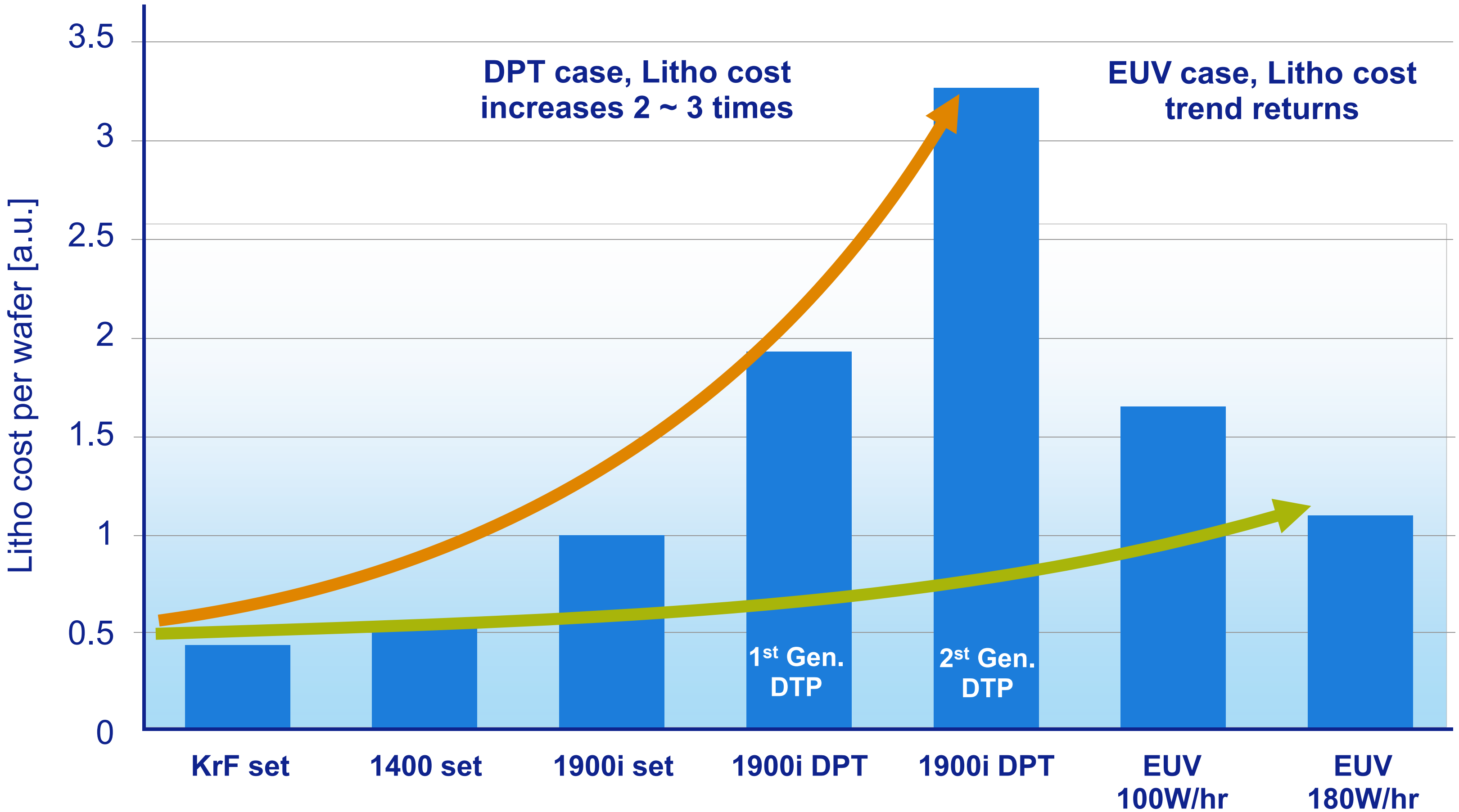
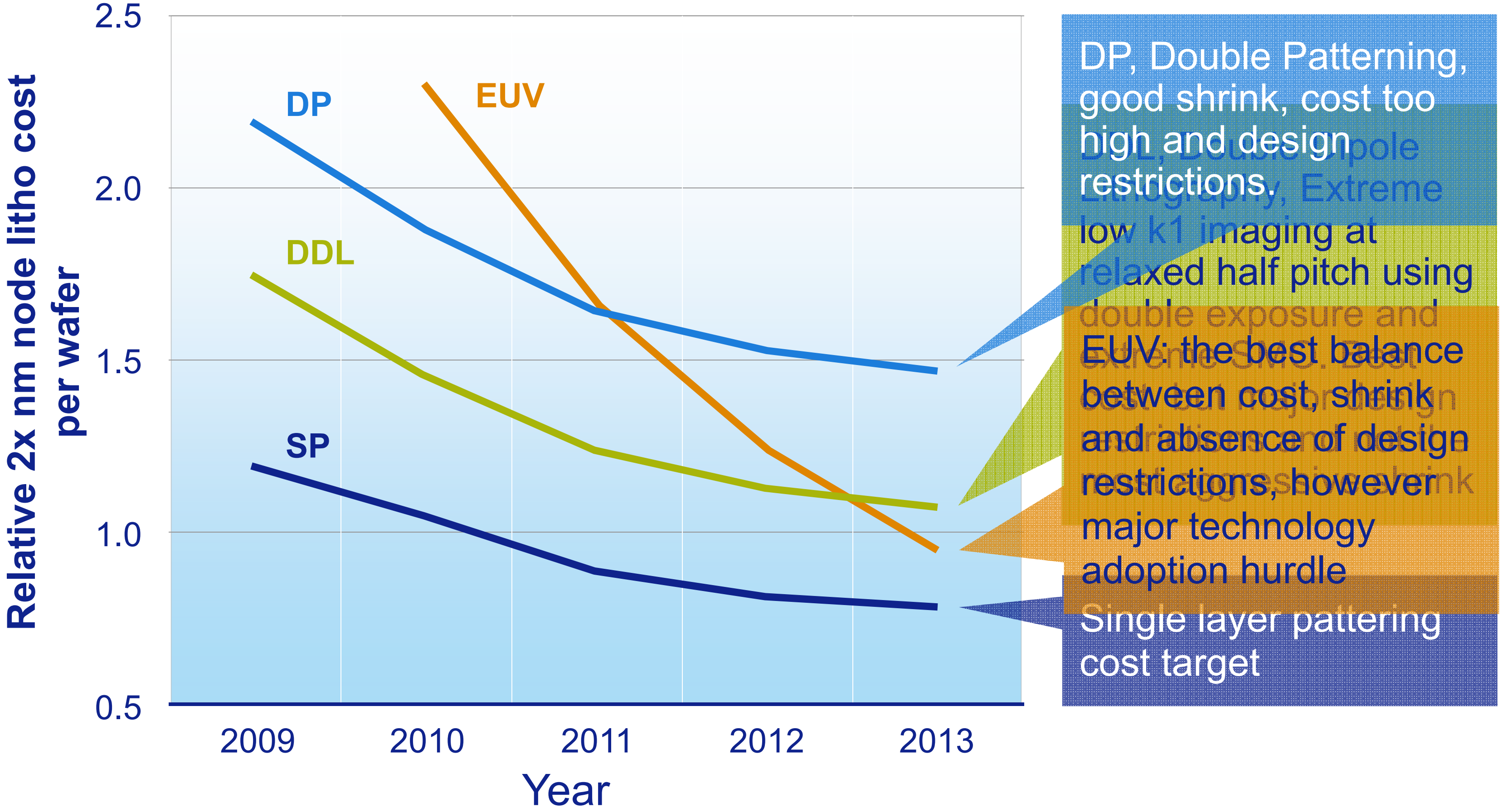
Litho costs back to normal with EUV >100 W/hr



Source Samsung, Litho Forum, New York, May 2010

EUV is the only feasible litho technology for foundries

Enabling cost effective shrink to 2x node without design restriction



Source TSMC, Prague 2009

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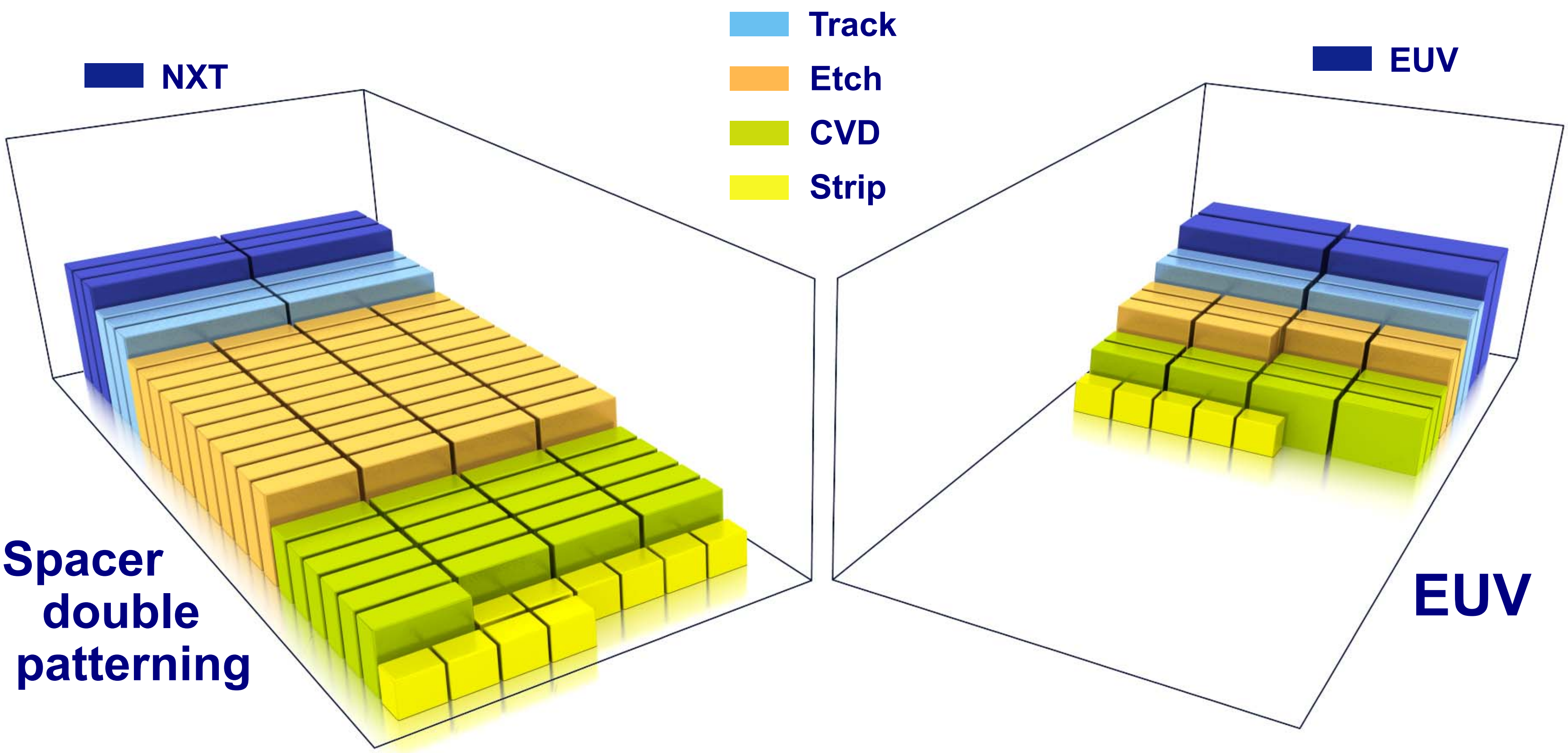
EUV can increase the fab capacity

Larger footprint required to support Multi Patterning schemes



1200 m^2 clean room
130k Wafers / Month

627 m^2 clean room OR
250k Wafers / Month

EUV has come a long way in last 25 years

1st papers soft X-ray for lithography (LLNL, Bell Labs)

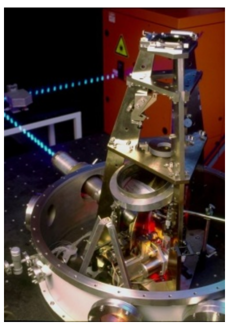
ASML start EUVL research program

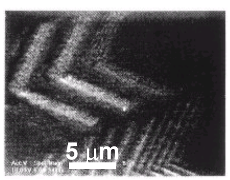
ASML ships 2 alpha tools to IMEC (Belgium) and CNSE (USA)

ASML pre-production tools planned shipment

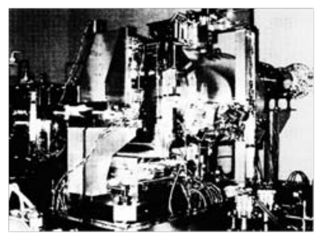
'85	'86	'87	'88	'89	'90	'91	'92	'93	'94	'95	'96	'97	'98	'99	'00	'01	'02	'03	'04	'05	'06	'07	'08	'09	'10

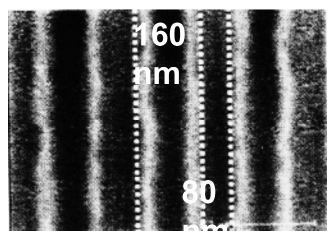
NL:



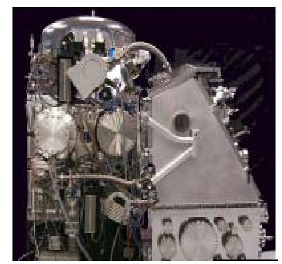


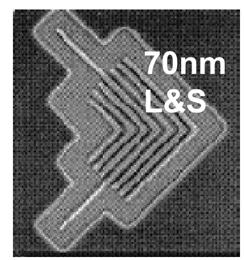
Japan:



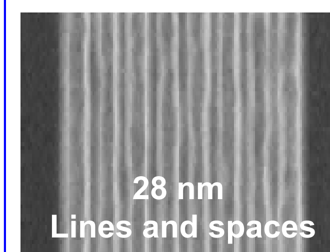


USA:





NL:



- ASML has active program since 1997.
- Currently ~1000 people work on pre-production system to be shipped 2010.

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… and much more to come in the next few years

	2006 Proto System	2010 NXE:3100	2012 NXE:3300B	2013 NXE:3300C
Resolution	32 nm	27 nm	22 nm	16* nm
NA / σ	0.25 / 0.5	0.25 / 0.8	0.32 / 0.2-0.9	0.32 / OAI
Overlay (SMO)	< 7 nm	< 4.5 nm	< 3.5 nm	< 3 nm
Throughput W/hr	4 W/hr	60 W/hr	125 W/hr	150 W/hr
Dose, Source	5 mJ/cm², ~8 W	10 mJ/cm², >100 W	15 mJ/cm², >250 W	15 mJ/cm², >350 W

Main improvements
1) New EUV platform: NXE
2) Improved low flare optics
3) New high sigma illuminator
4) New high power source
5) Dual stages

Main improvements
1) New high NA 6 mirror lens
2) New high efficiency illuminator
3) Off-axis illumination optional
4) Source power increase
5) Reduced footprint

Platform enhancements
1) Off-Axis illumination
2) Source power increase

* Requires <7 nm resist diffusion length

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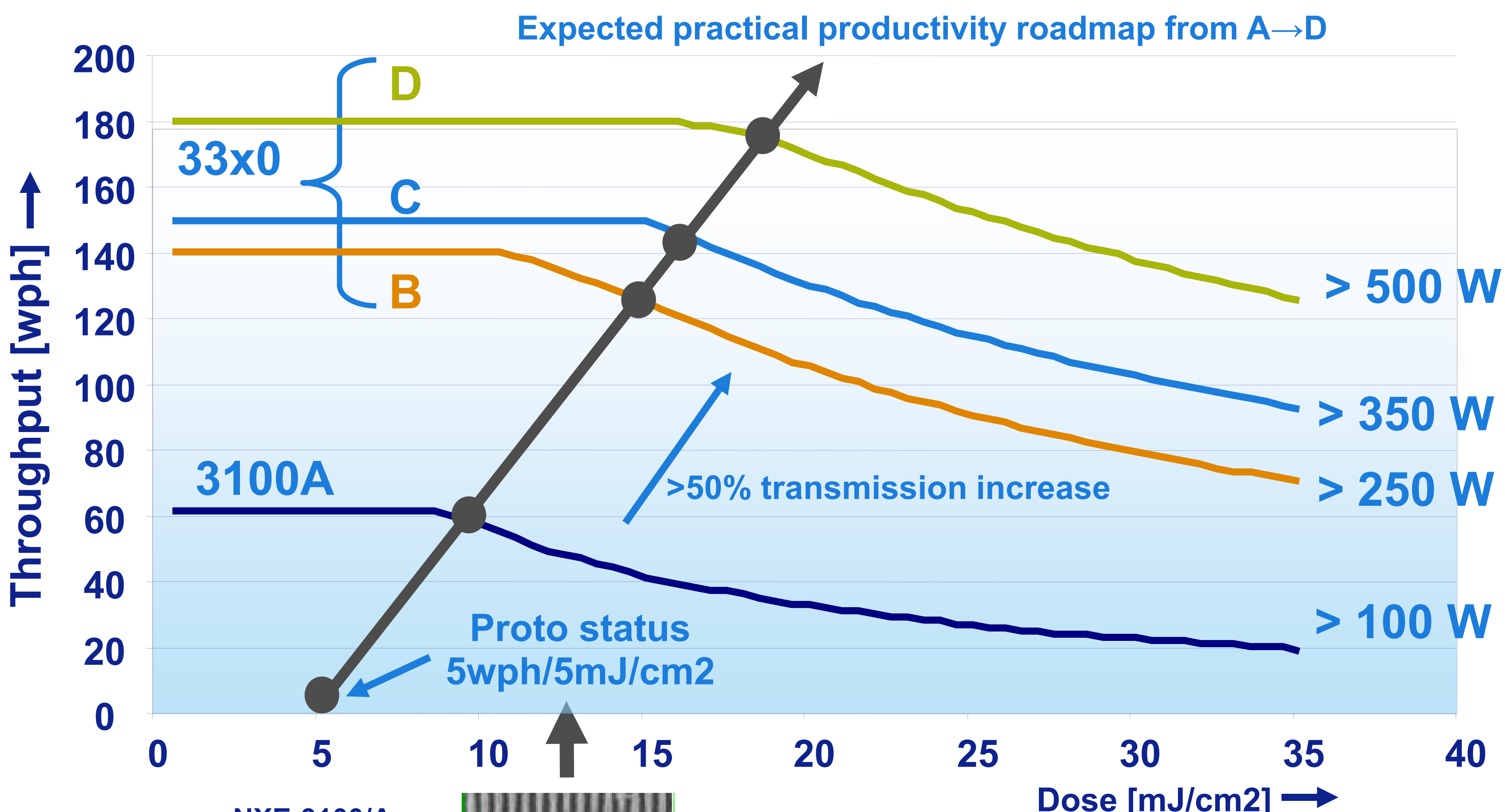
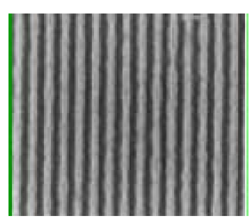
Source Power, Resist Sensitivity, Transmission, Stages

All need to increase over time to meet user cost targets





22nm dense lines
12.8mJ/cm2, 4.3nm LWR MET,
Intel Younkin et al, EUVS,
Prague 2009

Agenda

- Roadmap
- Status
  - Alpha Demo tool
  - NXE:3100
- Challenges
- Summary & conclusion

2 Alpha-demo tools used by multiple customers since 2006

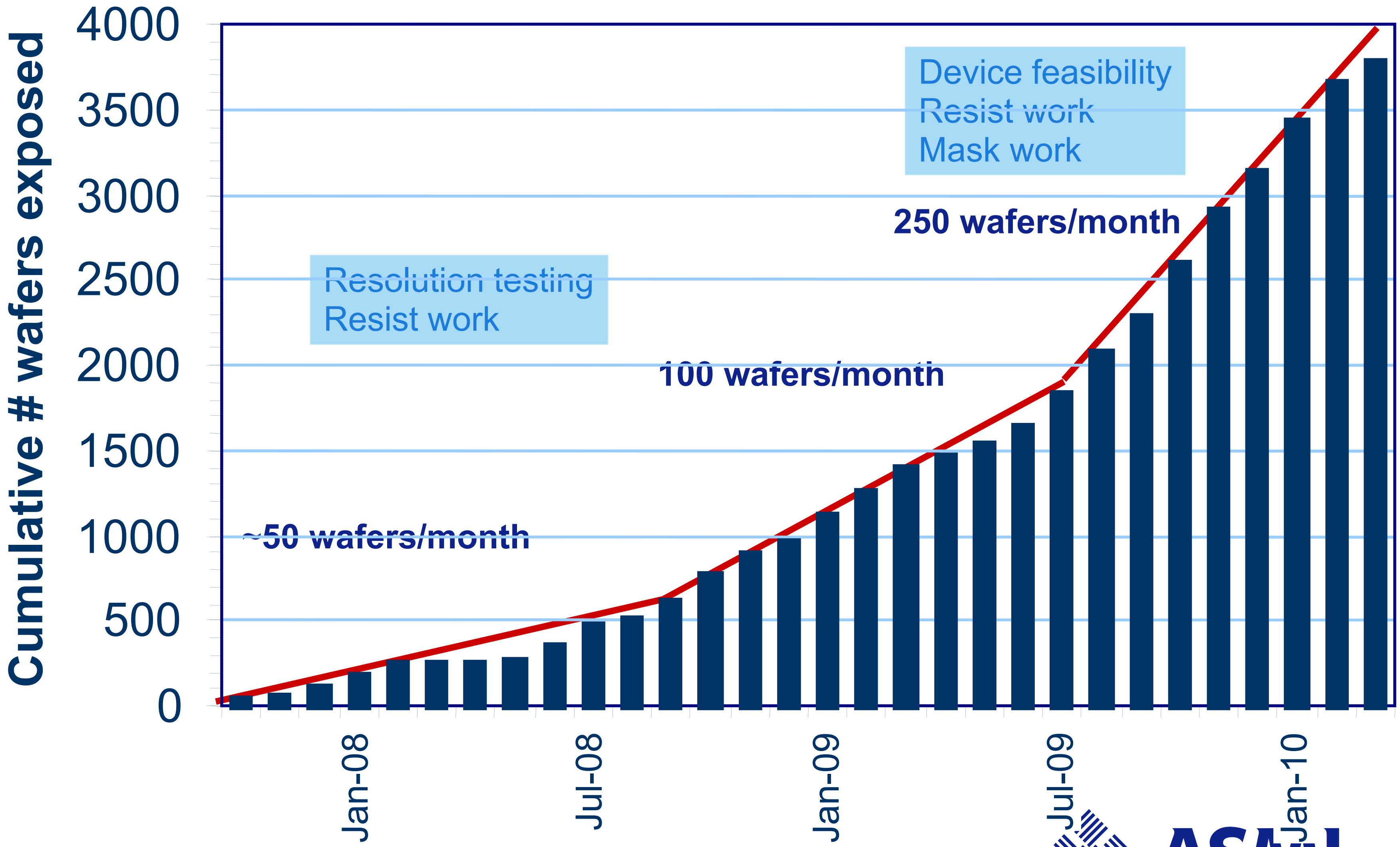
COLLEGE OF NANOSCALE SCIENCE & ENGINEERING
UNIVERSITY AT ALBANY State University of New York

λ	13.5 nm
NA	0.25
Field size	26 x 33 mm^2
Magnification	4x reduction
Sigma	0.5

- 300mm Single stage
- linked to track
- Single reticle load
- Uses TWINSCAN technology
- Sn discharge source

0.25NA Systems producing >3000 R&D wafers

and number of wafers per month continues to improve



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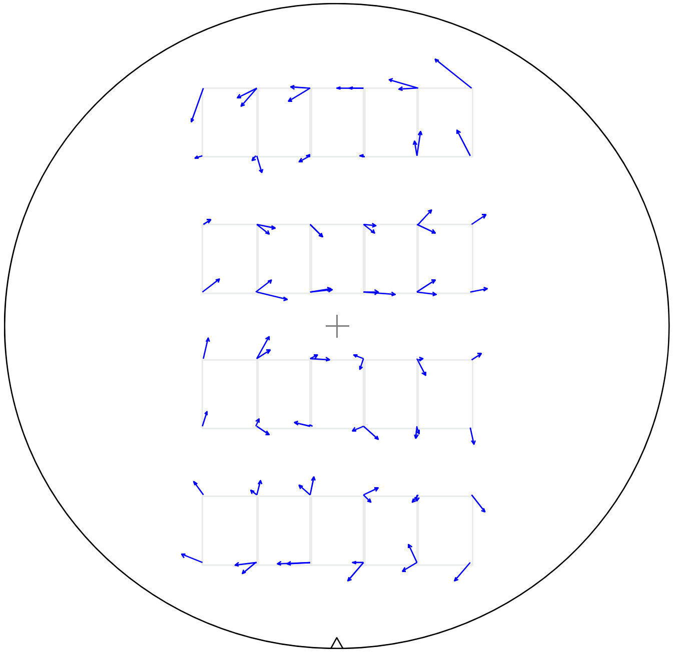
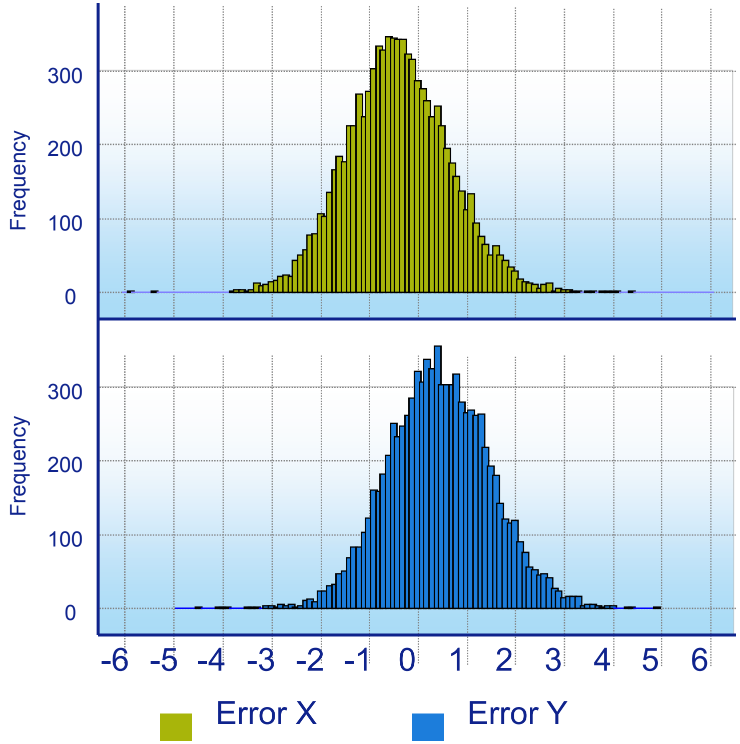
Overlay performance supports device integration

On-product Overlay Residuals
X = 8.0 nm, Y = 7.8 nm



Single Machine Overlay
X = 2.2 nm, Y = 2.8 nm



source: Global Foundries

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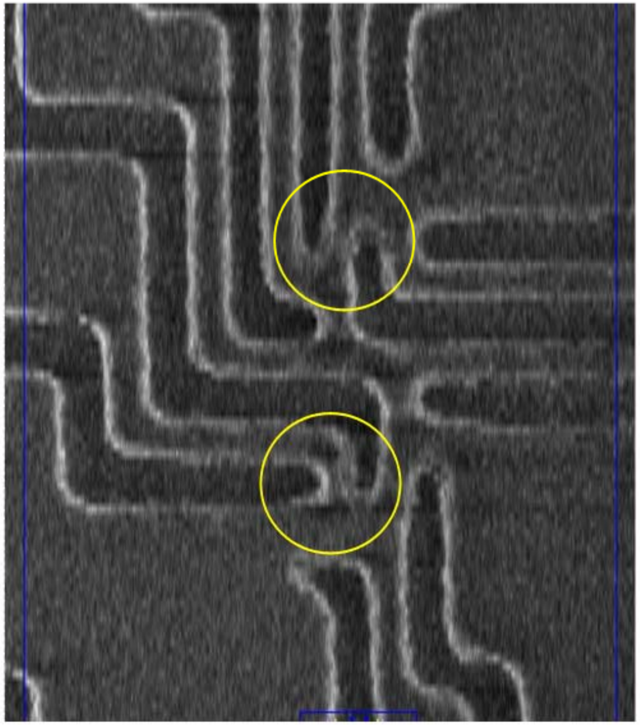
EUV has demonstrated superior imaging compared to 193

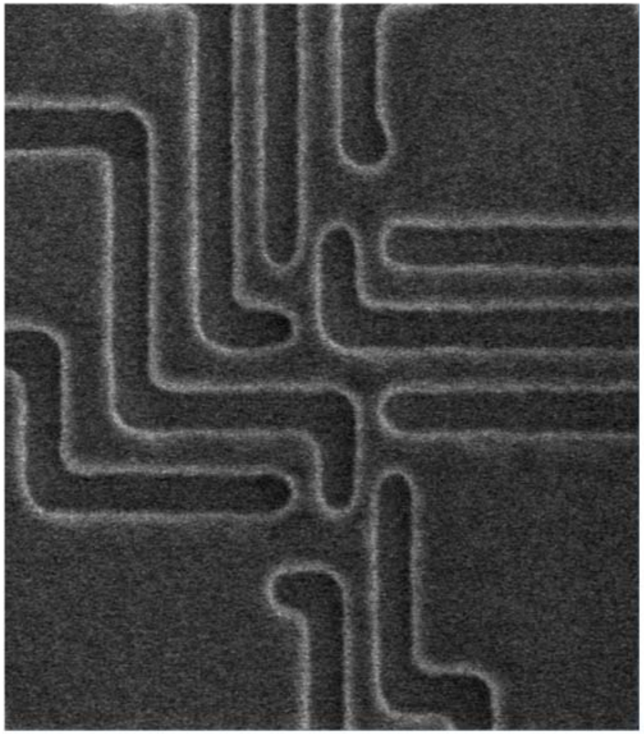
EUV Lithography: SRAM - M1 Level

AMD Smarter Choice

0.08 μm² SRAM Flycell



Best image by 193i Litho
(Double Dipole exposures)

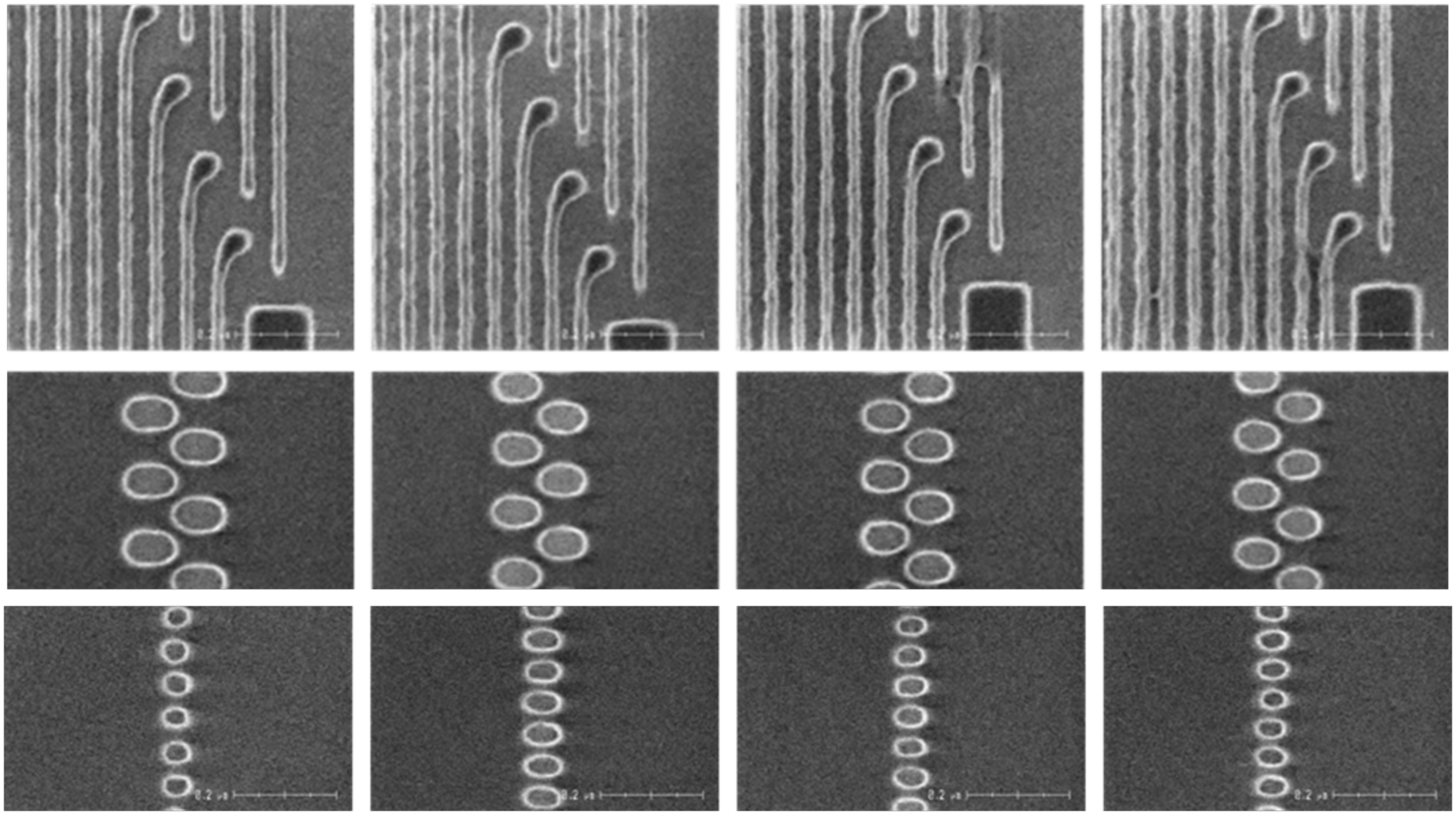


By EUV ADT

NAND word line connectivity area down to 26 nm

Staggered and slot contacts

30 nm L/S | 28 nm L/S | 27 nm L/S | 26 nm L/S



Mask funded by EU EXEPT program
in cooperation with IMEC

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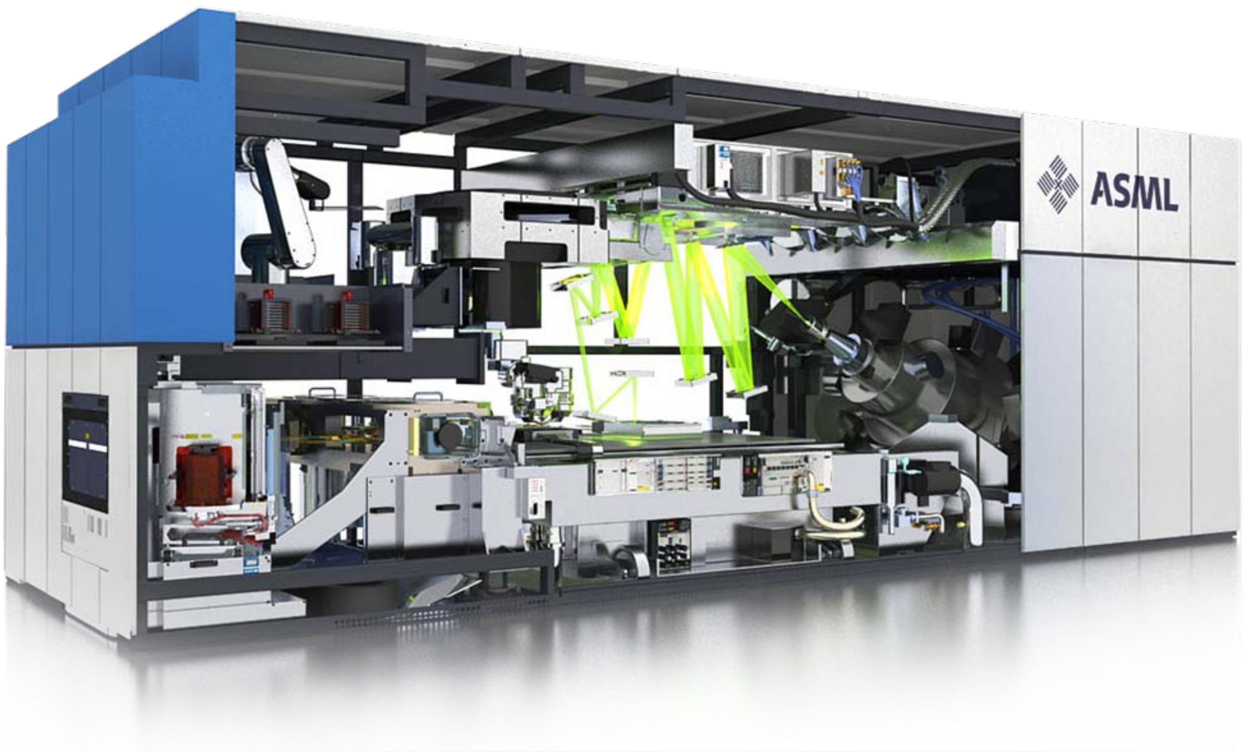
NXE:3100 is the 1st generation of the NXE platform



- NA=0.25
- Sigma=0.8
- Resolution 27 nm
- SMO=4.5 nm
- MMO=7.0 nm
- Productivity 60wph at 10mJ/cm^2 resist

Status Integration Oct. 2009

3 NXE:3100 systems: Integration, Early Access and 1st Output

NXE:3100 #1

System completed
ArF source used for integration and qualifying overlay, S/W, TPT

NXE:3100 #2

System completed
Source being installed

NXE:3100 #3

Wafer Stage installed
Optics installed
Reticle Stage June
Source June
1st ship H2 2010

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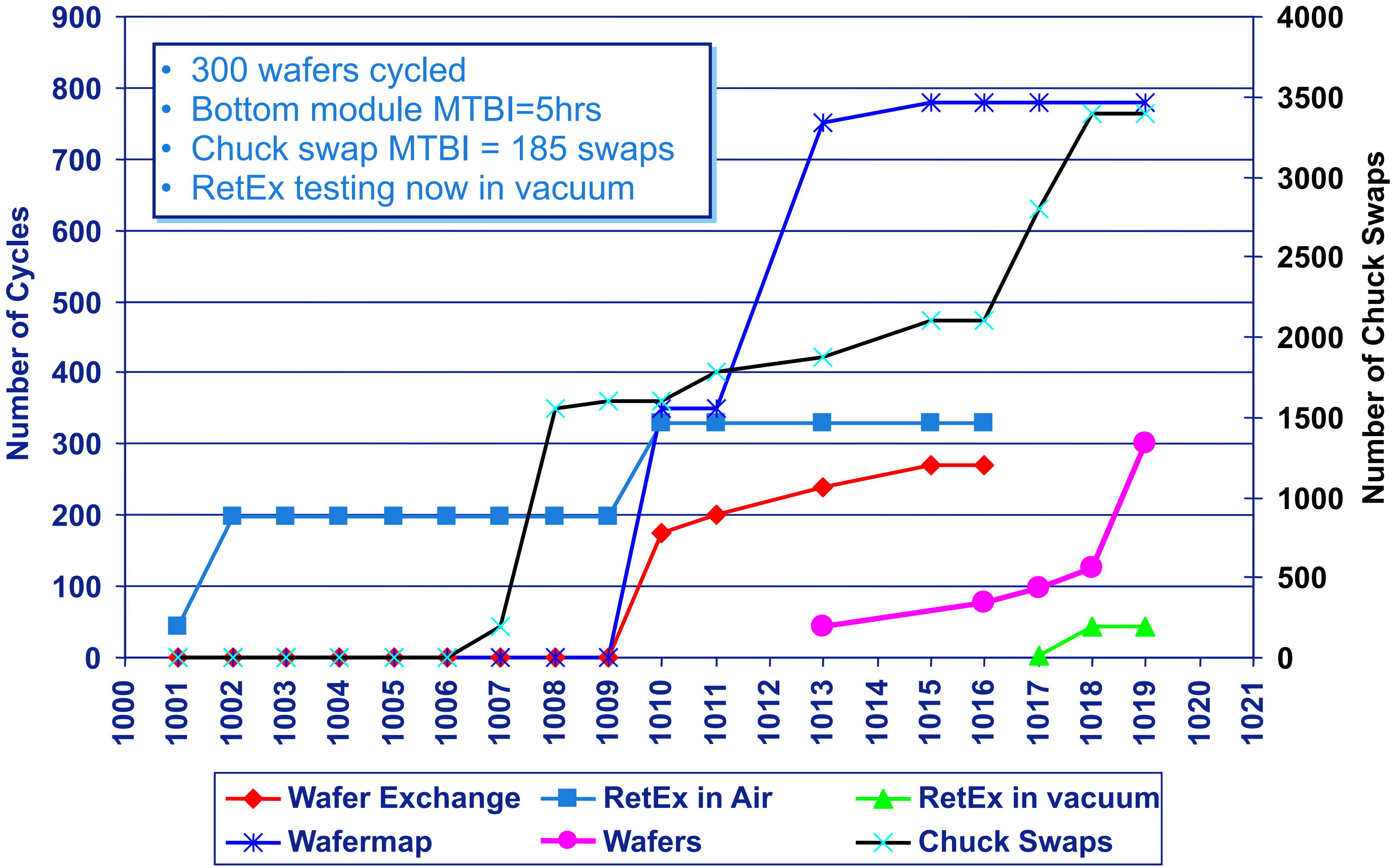
3 more NXE:3100 in build-up, 2 additional cabins

NXE:3100 #4

NXE:3100 #5

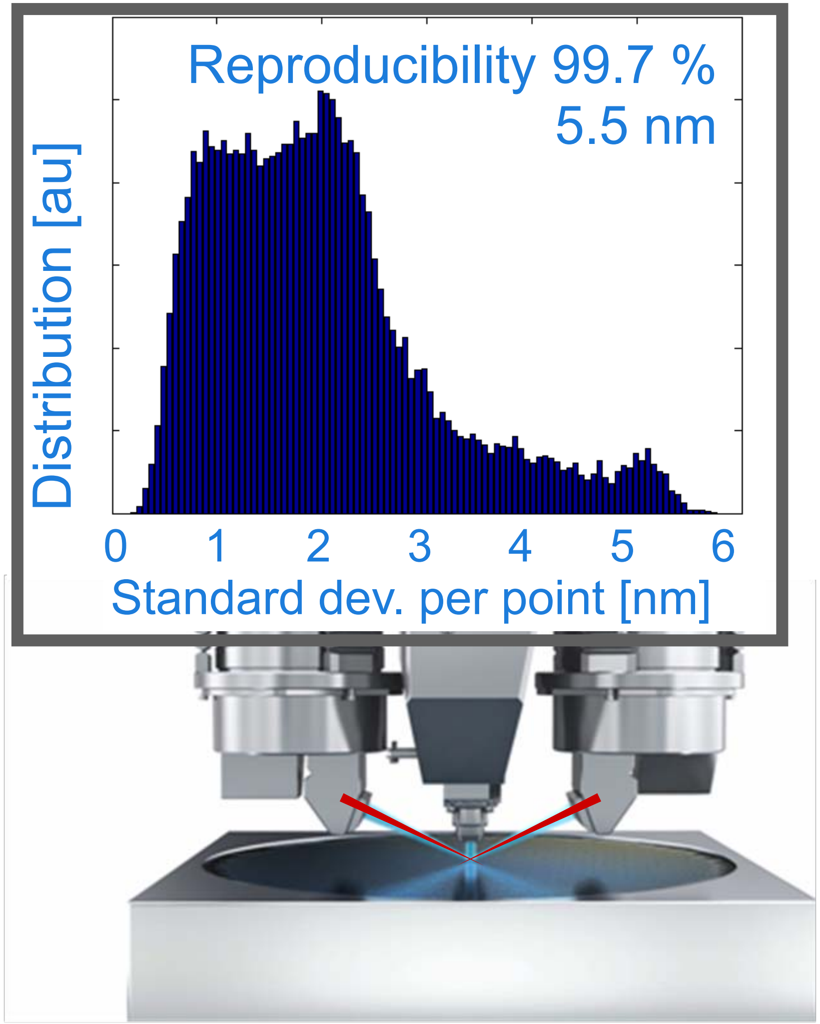
NXE:3100 #6

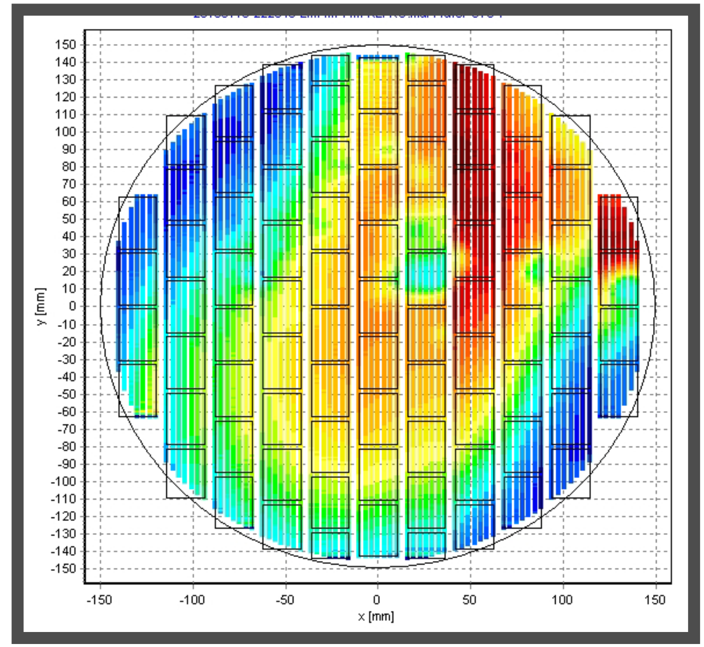
Reliability Testing Progressing



Wafer Stage Integration in vacuum

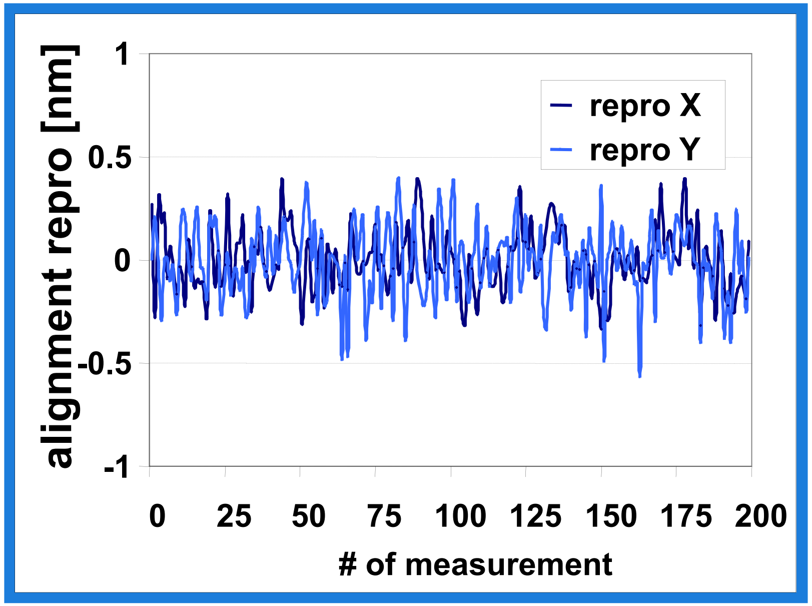
Focus Control and Leveling verified

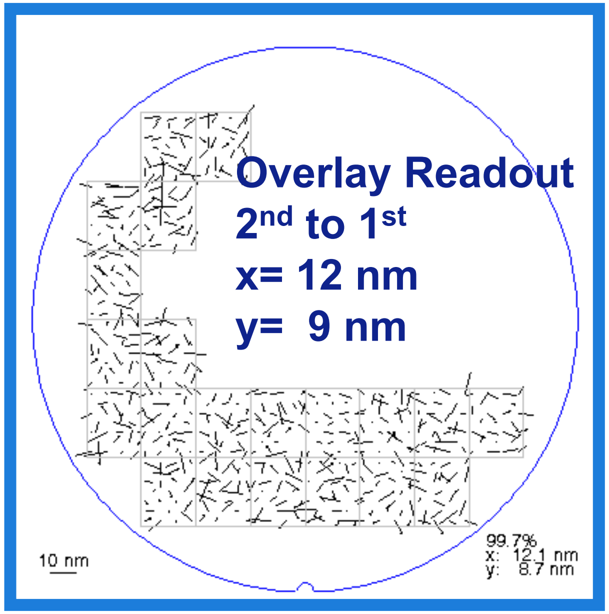


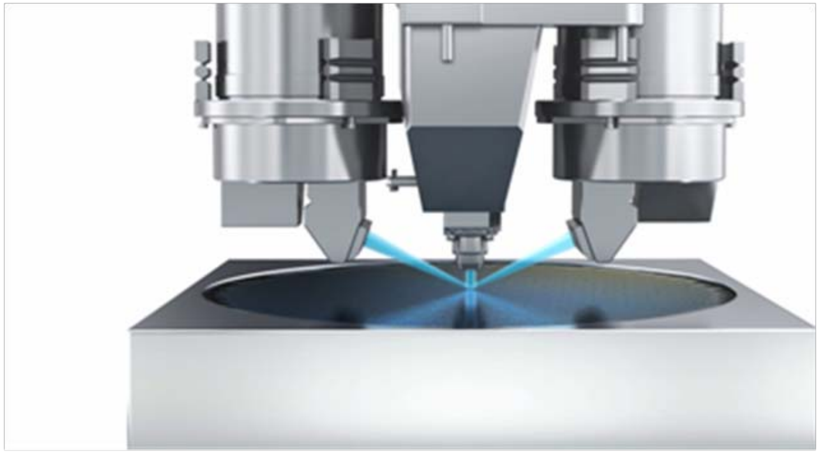


Wafer Stage Integration in vacuum

Alignment and Overlay readout verified







Agenda

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- Challenges
  - Critical issues
  - Extension of Shrink roadmap
- Summary & conclusion

Critical issues EUV 2005-2009

2005 / 32hp	2006 / 32hp	2007 / 22hp	2008 / 22hp	2009 / 22hp
1. Resist resolution, sensitivity & LER met simultaneously	1. Reliable high power source & collector module	1. Reliable high power source & collector module	1. Long-term source operation with 100 W at IF and 5MJ/day	1. MASK
2. Collector lifetime	2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Defect free masks through lifecycle & inspection/review infrastructure	2. SOURCE
3. Availability of defect free mask	3. Availability of defect free mask	3. Availability of defect free mask	3. Resist resolution, sensitivity & LER met simultaneously	3. RESIST
4. Source power	4. Reticle protection during storage, handling and use	4. Reticle protection during storage, handling and use	• Reticle protection during storage, handling and use	• EUVL manufacturing integration
▪ Reticle protection during storage, handling and use	5. Projection and illuminator optics quality & lifetime	5. Projection and illuminator optics quality & lifetime	• Projection / illuminator optics and mask lifetime	
▪ Projection and illuminator optics quality & lifetime				

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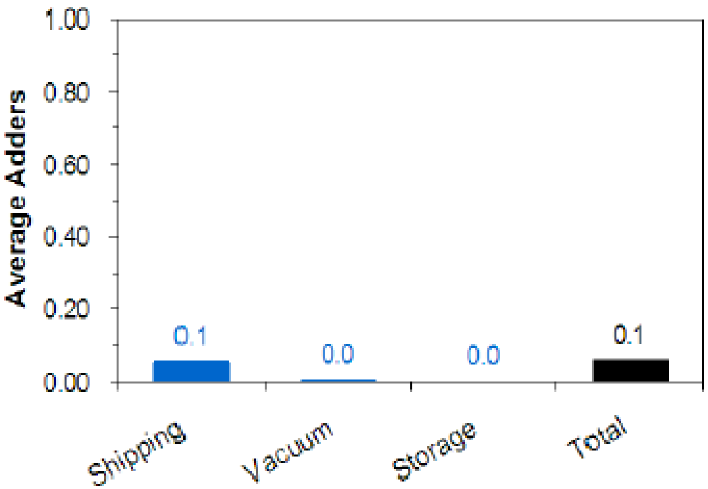
Mask critical issues

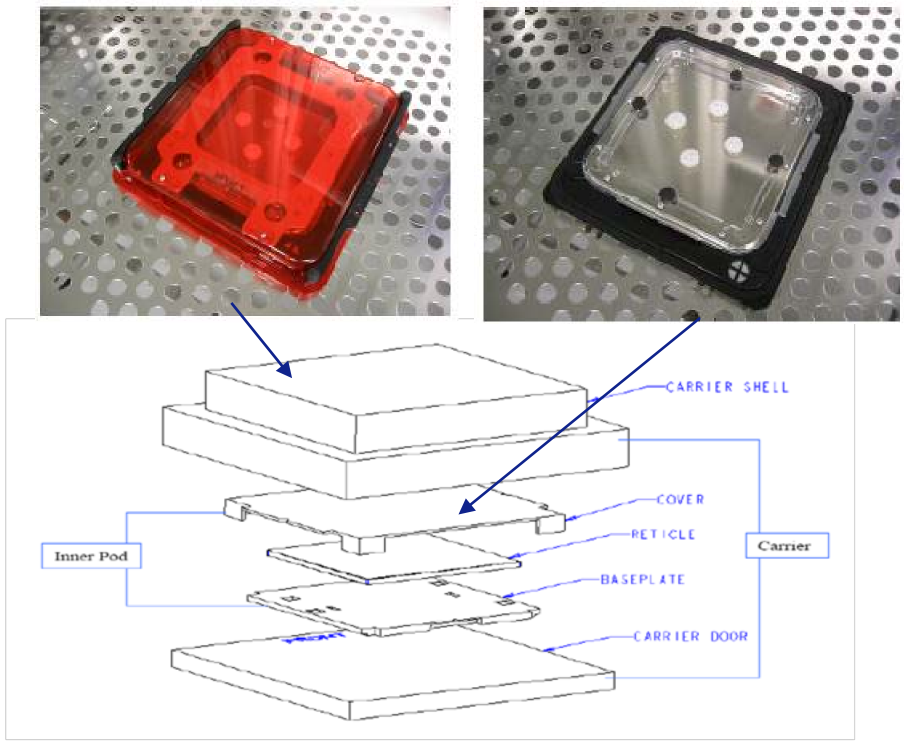
- Make a defect free mask
- Maintain a defect free mask
  - Avoid contamination
  - Inspection
  - Cleaning

Protection during shipping-handling

- MIRAI Selete and Sematech showed (SPIE 2008) that
  → dual-pod handling system is very effective in preventing contamination during handling/shipping: ~0.1 particles/reticle average for lifetime use.
- However potential risk of contamination during exposure

Lifetime use defined as a round-trip shipment, vacuum, pump-vent, and accelerated storage test, at 53nm PSL equivalent inspection capability.



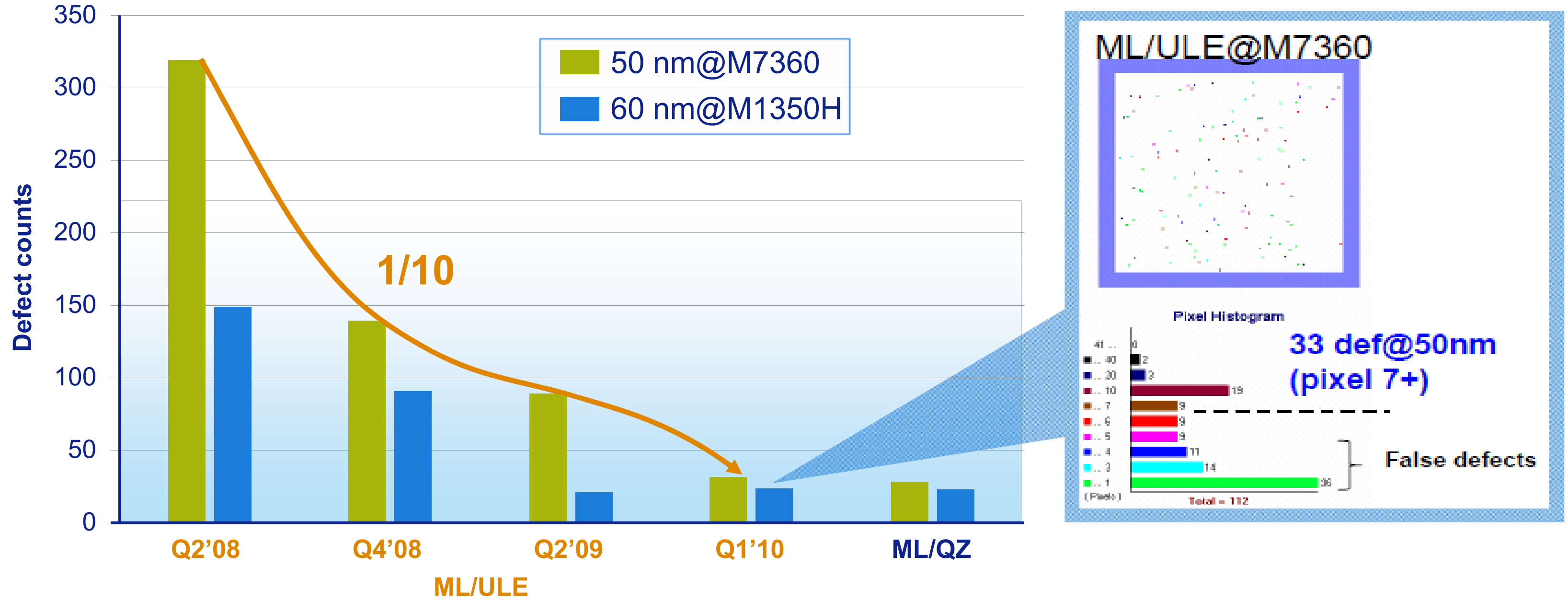


Reticle Technical and Infrastructure Gaps

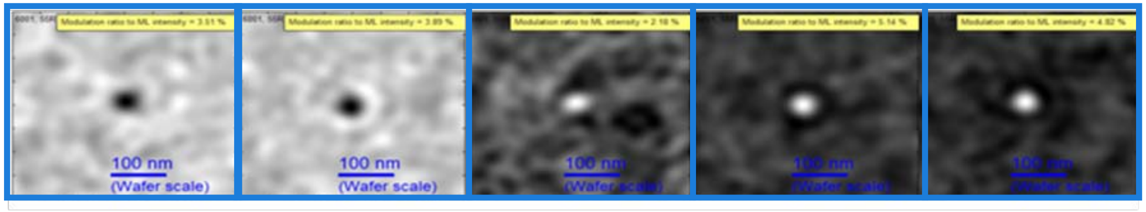
- Current reticle defectivity gap is about 25-100X
  - Need continuous improvement
  - Relaxation of flatness spec might help bridge gap
- Inspection gaps
  - Actinic blank inspection
  - Patterned defect inspection spec vs. actual
  - In-situ inspection
  - AIMs inspection
- SEMATECH is adopting a "bridge" tool solution for actinic blank and AIMS inspection so that some capability will be available for "pilot line" in 2011
- Production actinic inspection, AIMS, and patterned inspection will require industry-wide funding (July workshop)

Mask infrastructure improvements: blanks & inspection

Multi-layer Ultra Low Expansion blank defects approaching quartz performance[1]



Optical inspection able to detect phase defects 3.4 nm x 45.4 nm in size[2]



1 Source: Hoya, Samsung EUV conference april 2010
2 Source: KLA, EUV symposium Prague, October 2009

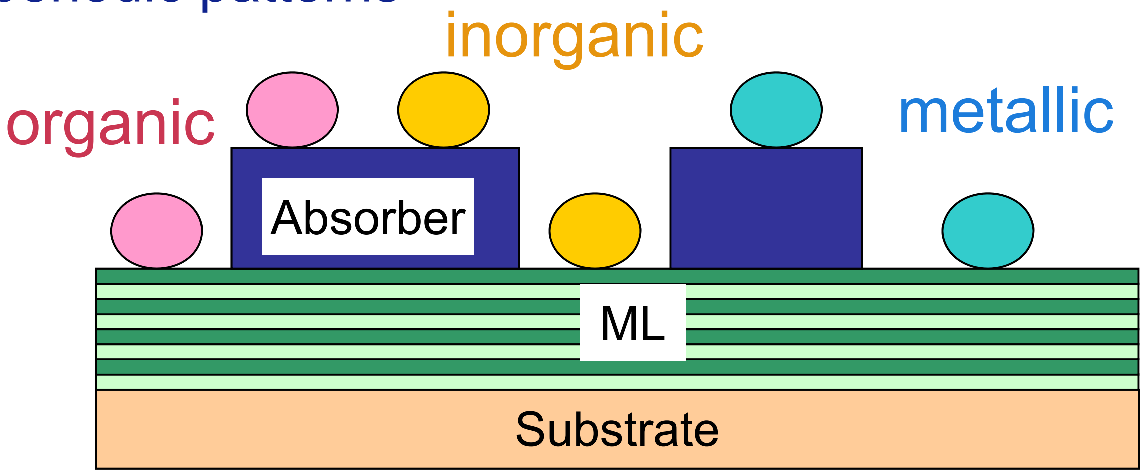
Slide 29 | Public

In-situ Inspection

- Need to verify reticle cleanliness AFTER loading into scanner and BEFORE printing wafers
  - Repeater concern is serious due to lack of pellicles
  - ArF scanners have in-situ reticle inspection capability
- Not having in-situ capability would require printing of defect look-ahead wafers
  - Manageable in development and perhaps in pilot line mode
  - Unacceptable for HVM
- Need focus from tool vendors to have capability avaialable in HVM tooling platforms

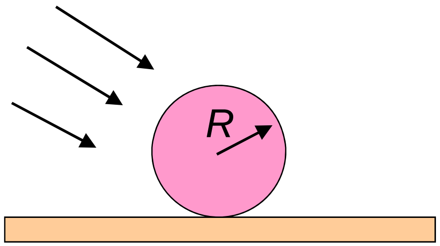
Reticle contamination: overview of the challange

- Mask → Substrate (ULE, 6mm)+ Multilayer mirror (Mo/Si-Ru capped, ~200nm) + Absorber (e.g.,TaN/TaNO, 50-70nm)
- Particles → organics, Al, Fe (steel), Zn, Sn, Ni, Ti, Cu, oxides of previous metals, ceramics, ML, absorber, … (?)
  - Any shape, any size > 25nm (@22nm node)
- Topography → Ridges, trenches, contact holes, periodic/non-periodic patterns

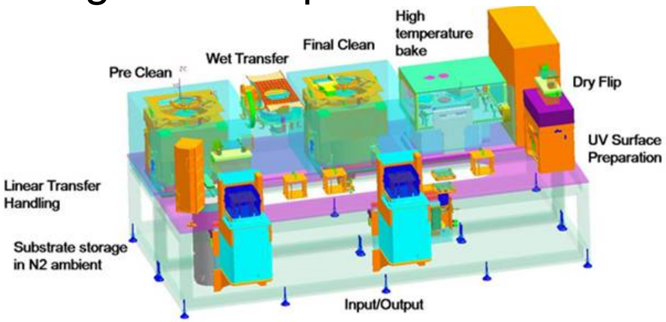


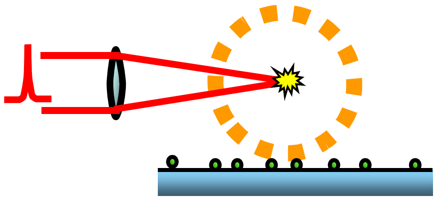
Cleaning challenges/issues

- Smaller particles are more difficult to remove
  → Adhesion force ~ ***R***
  → Applied cleaning force ~R^2
- Challenge: remove particles without damage
- Standard off-line wet cleaning:
  - Can clean as far as it can be inspected (~40nm)
  - Number of cleanings is limited (slight damage from chemicals)
  - Not vacuum compatible → difficult to integrate into scanner
- Challenge: dry, local, vacuum-compatible cleaning technique for integration in EUV tool
  - Laser Shockwave Cleaning



Multi-stage wet (/dry) cleaning – megasonics / plasma





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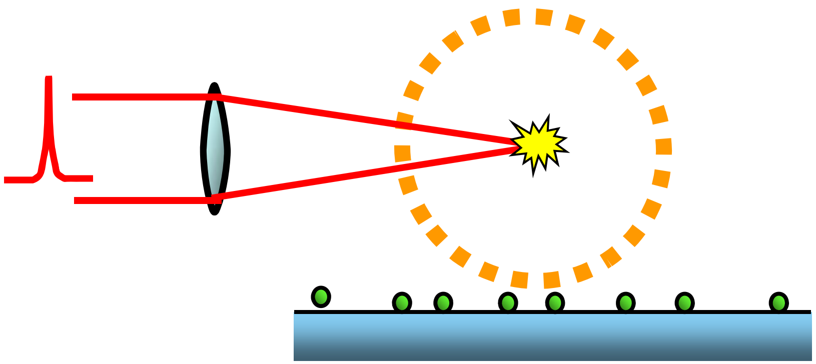
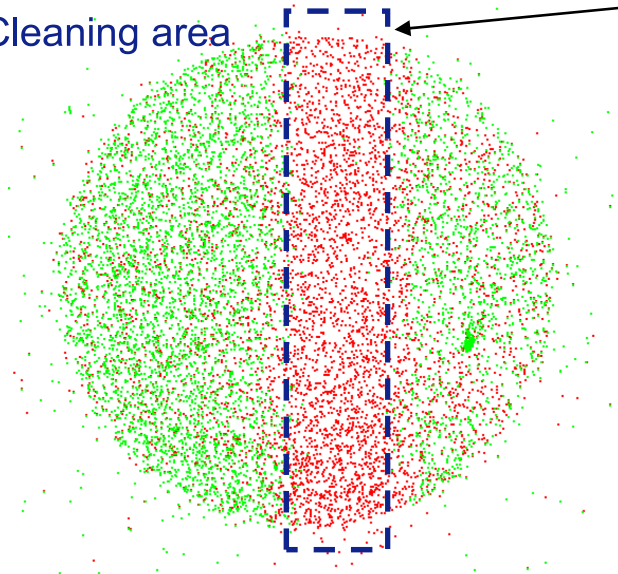
Laser Shockwave Cleaning

- Dry, contact-free method of cleaning
- Local cleaning possible → very fast!
- Vacuum operation theoretically possible
- The shockwave produced by the Laser-Induced Breakdown (LIB) from a high-energy pulse in air provides the necessary cleaning force



Cleaning area

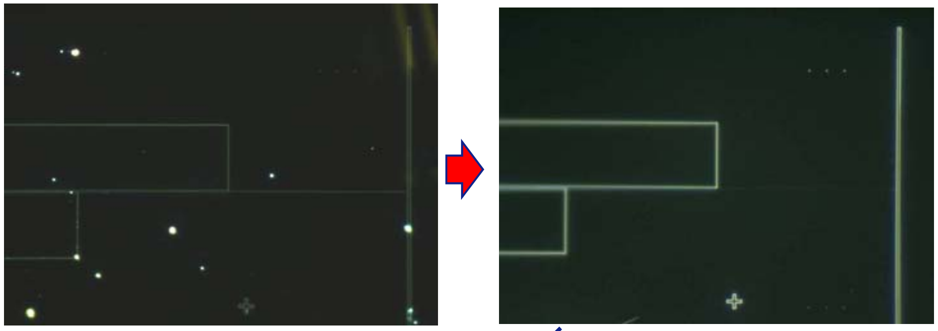


Before cleaning

After cleaning

MIX 40-100nm PSL on Silicon wafer	>120nm	100%
	>60nm	98%
Removal efficiency	>40nm	95%

Cleaning from real EUV reticle



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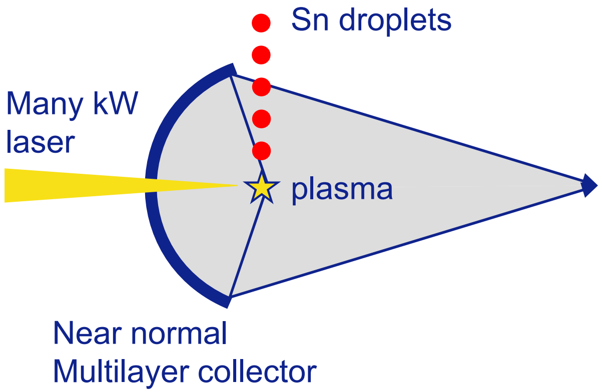
Source critical issues

- Power
- Burstlength (>400 msec), duty cycle (80%), uptime
- Cleanliness
- Cost (initial cost, operational cost)

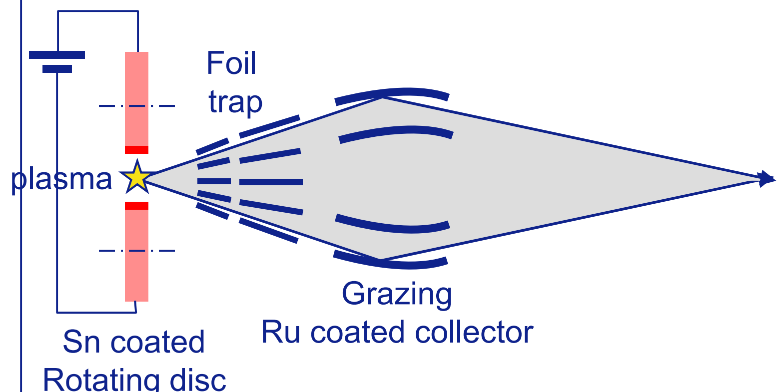
2 different source concepts pursued: LPP vs DPP

- **Laser-Produced Plasma source**



- CO2 laser
- Sn droplet target
- Debris mitigation using background gas and/or magnetic fields
- Near normal multilayer collector
- Pursued by: Gigaphoton, Cymer

- **Discharge Produced Plasma source**



- Direct conversion electricity => plasma
- Sn liquid
- Debris mitigation by set of foils
- Grazing incident collector
- Pursued by Ushio

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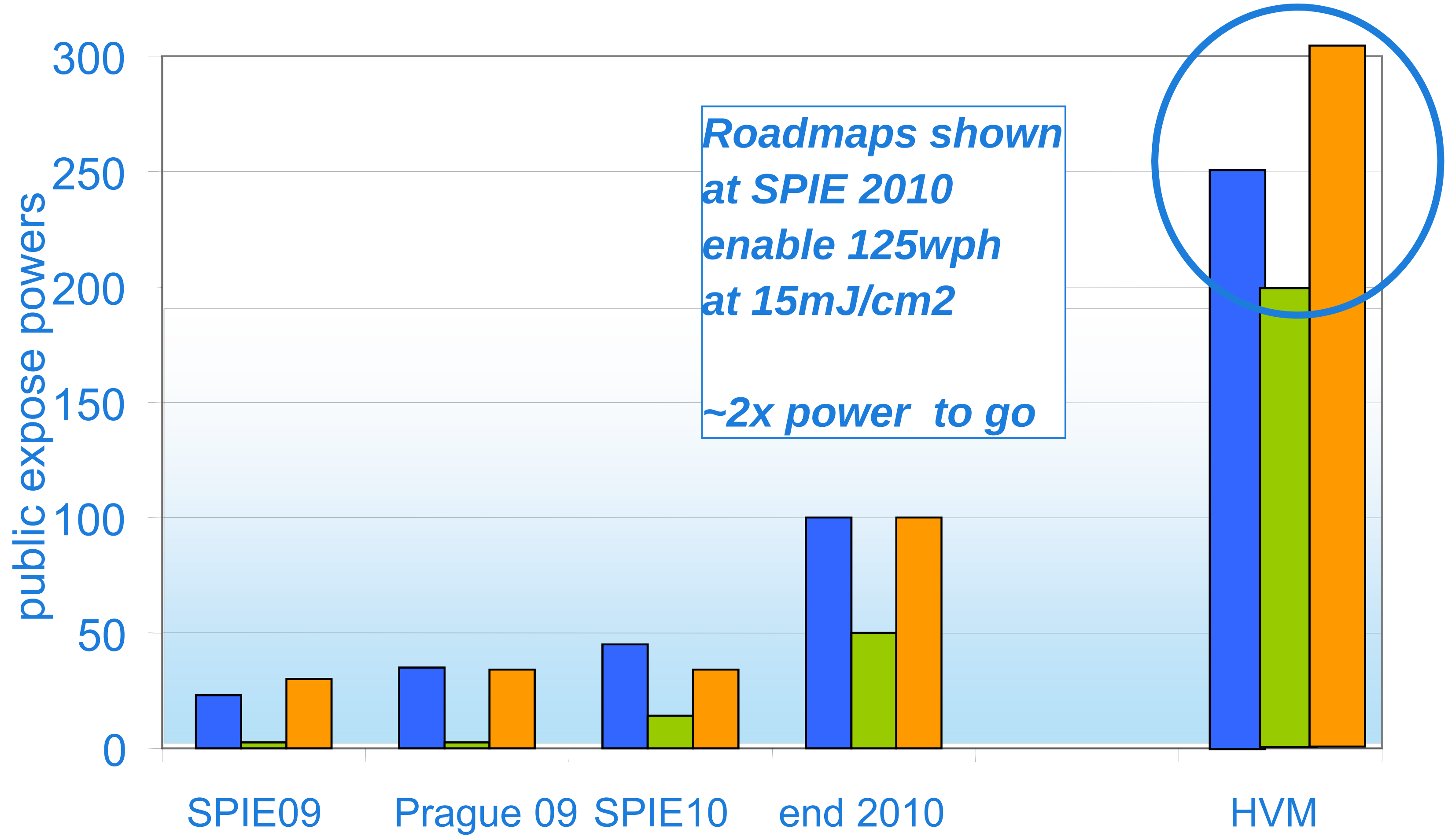
3 suppliers demonstrated steady progress However further increase of power is required



C. Wagner et al SPIE 2010

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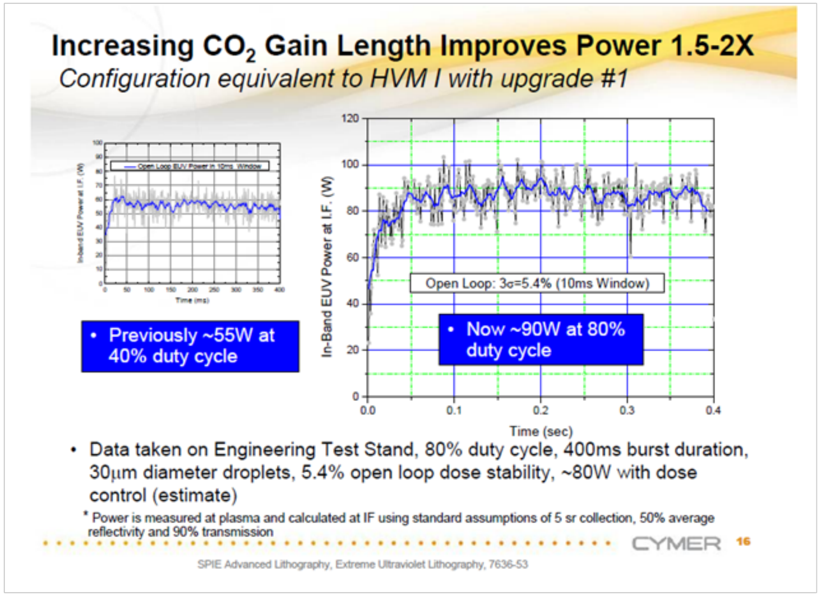
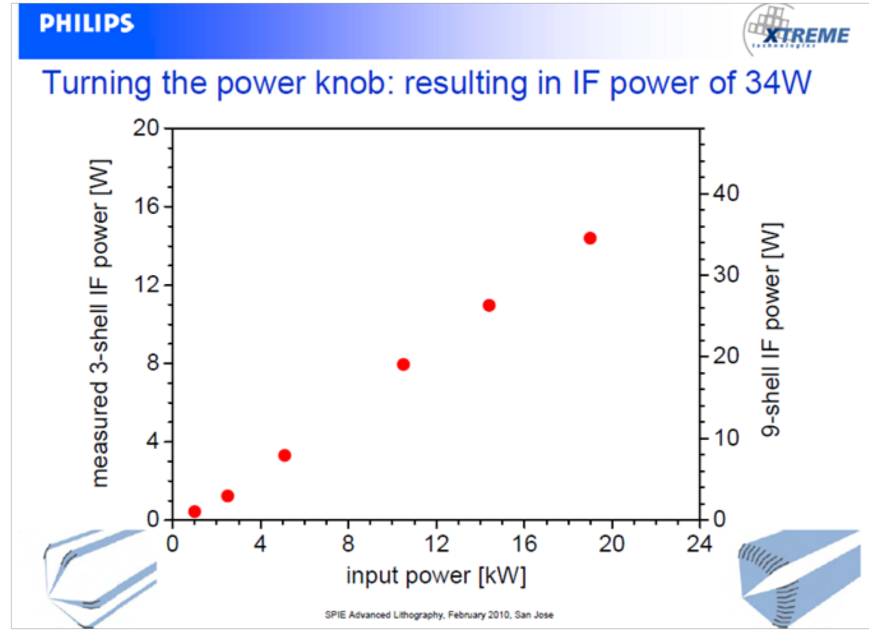
EUV increase by more power and/or increased CE

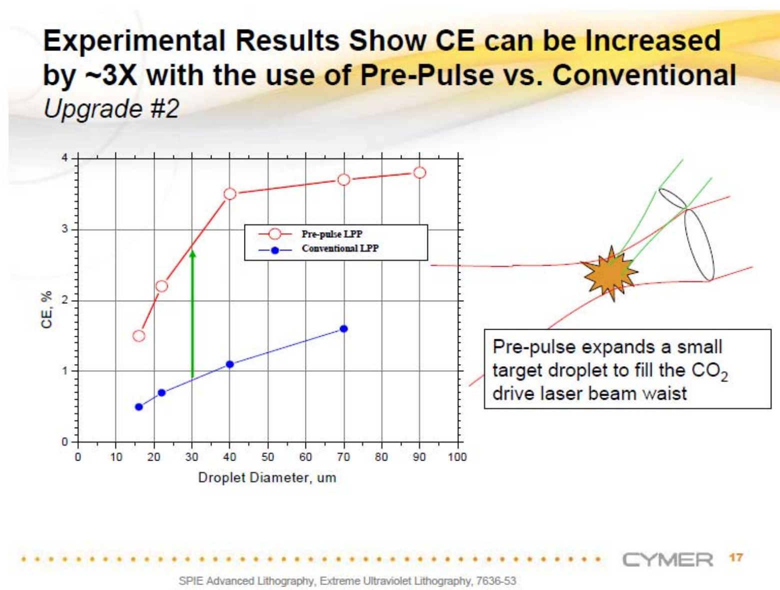
CE improvement is strongly preferred way

By "power knob" turning:





By CE gain (3x)



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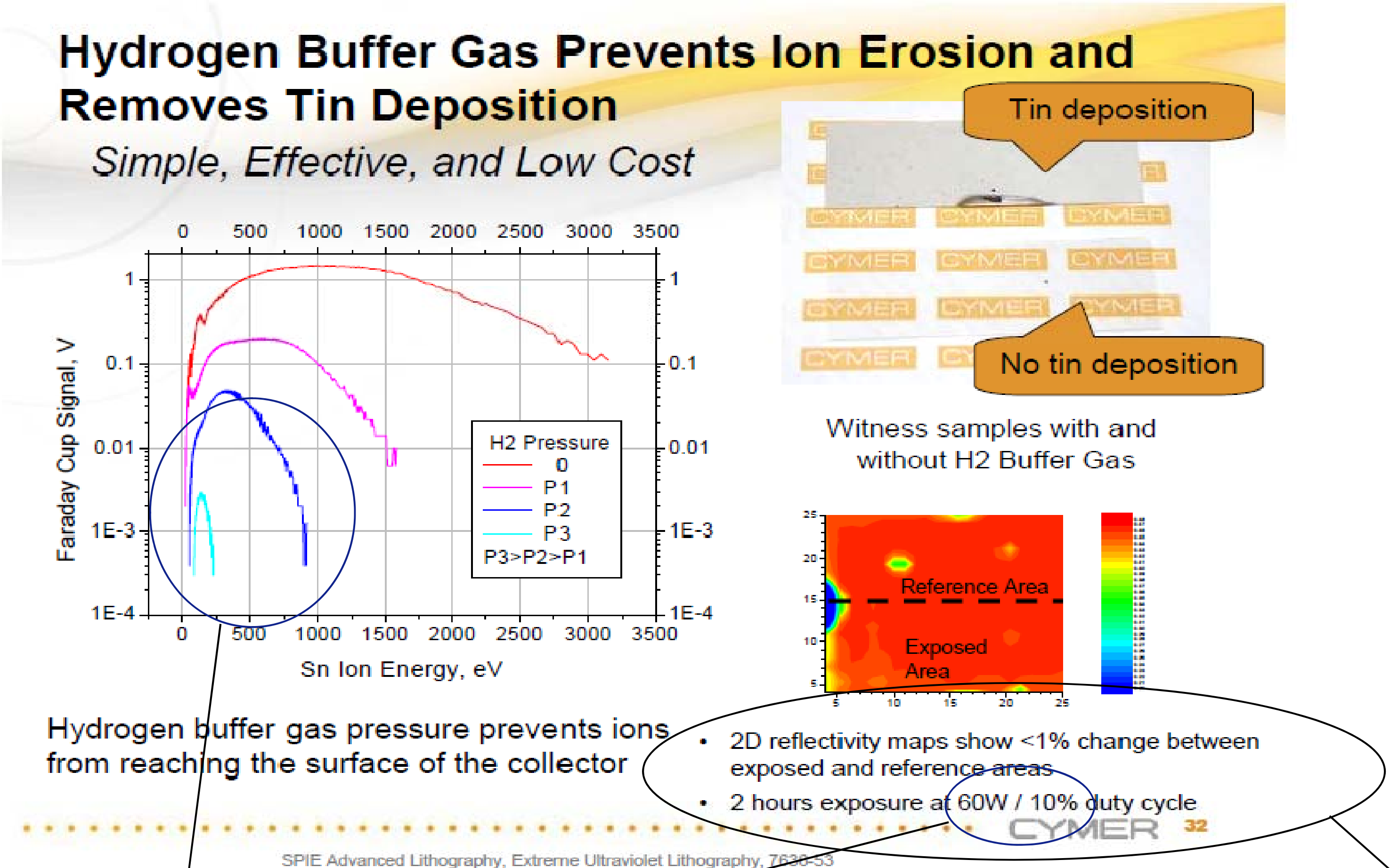
Collector lifetime must be ensured also at higher power levels



Lifetime demonstration of 1000x is needed

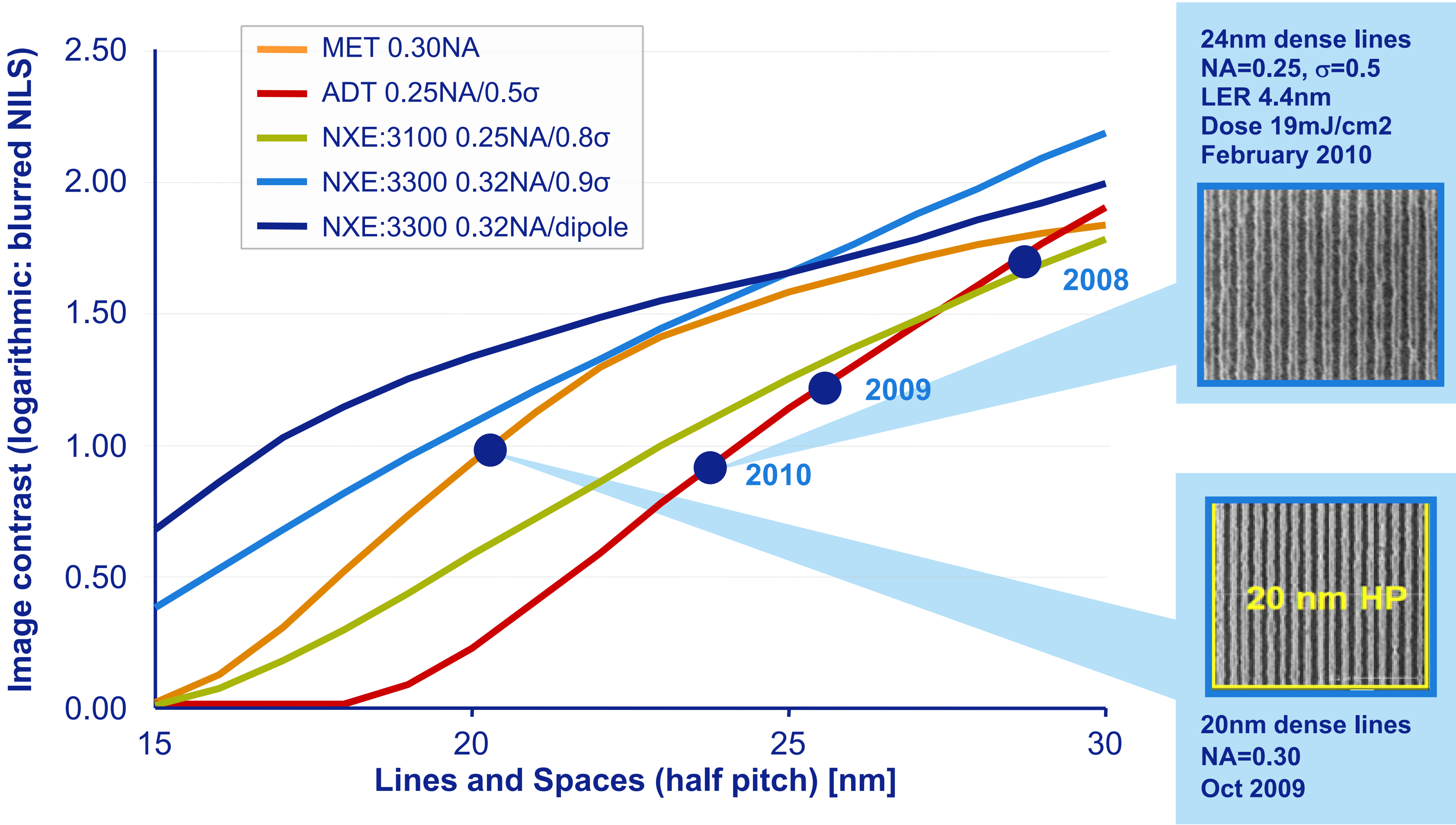
Maintaining debris suppression with power scaling of up to 100x is necessary

Resist critical issues

- Resolution
- Line edge roughness
- Sensitivity

Resist progress supports 16 nm resolution for NXE:3300

Calibrating champion 0.25NA full field and 0.3NA small field data

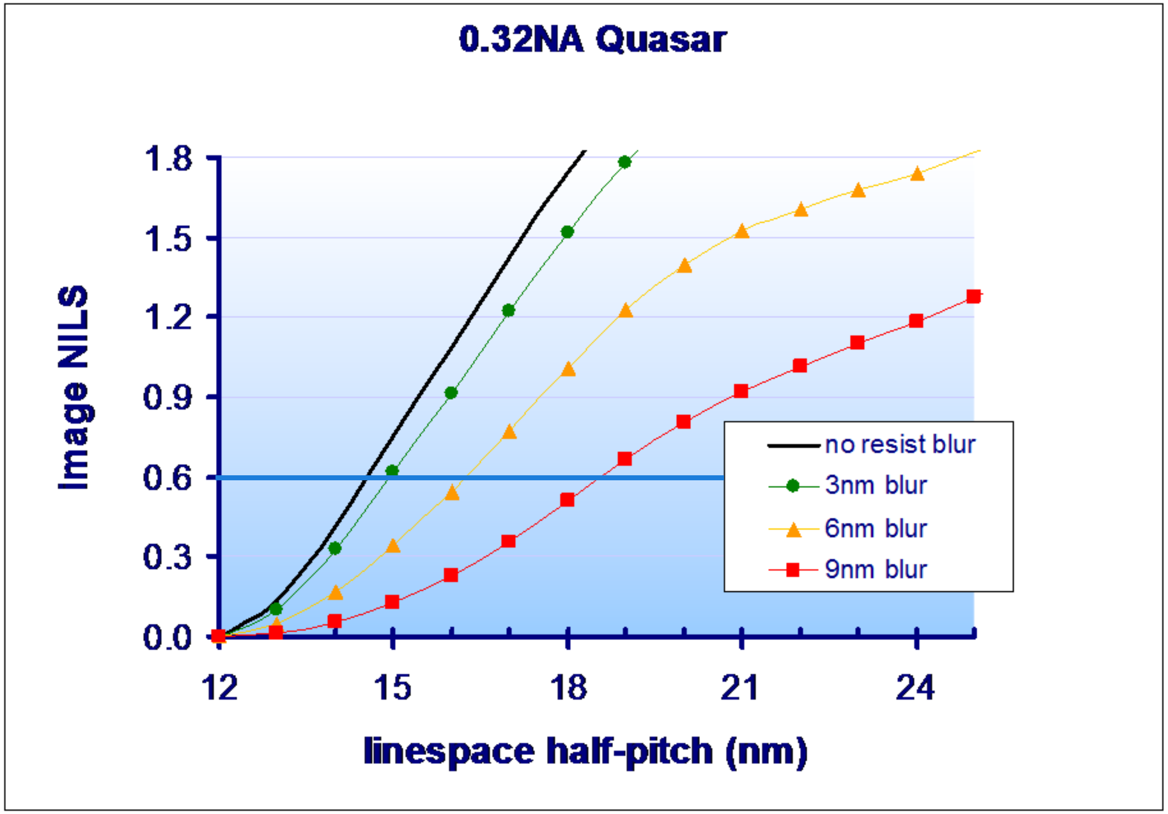


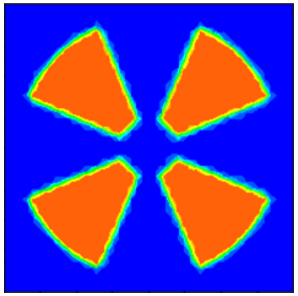
Source: 20nm data, Intel, EUVS, Oct 2009

Slide 40 | Public

Resolution and resist blur

- Resist blur degrades the projected image and limits resolution.
- Current lowest blur values (6-10nm) need reduction to less than 5nm to approach tool's optical limits.



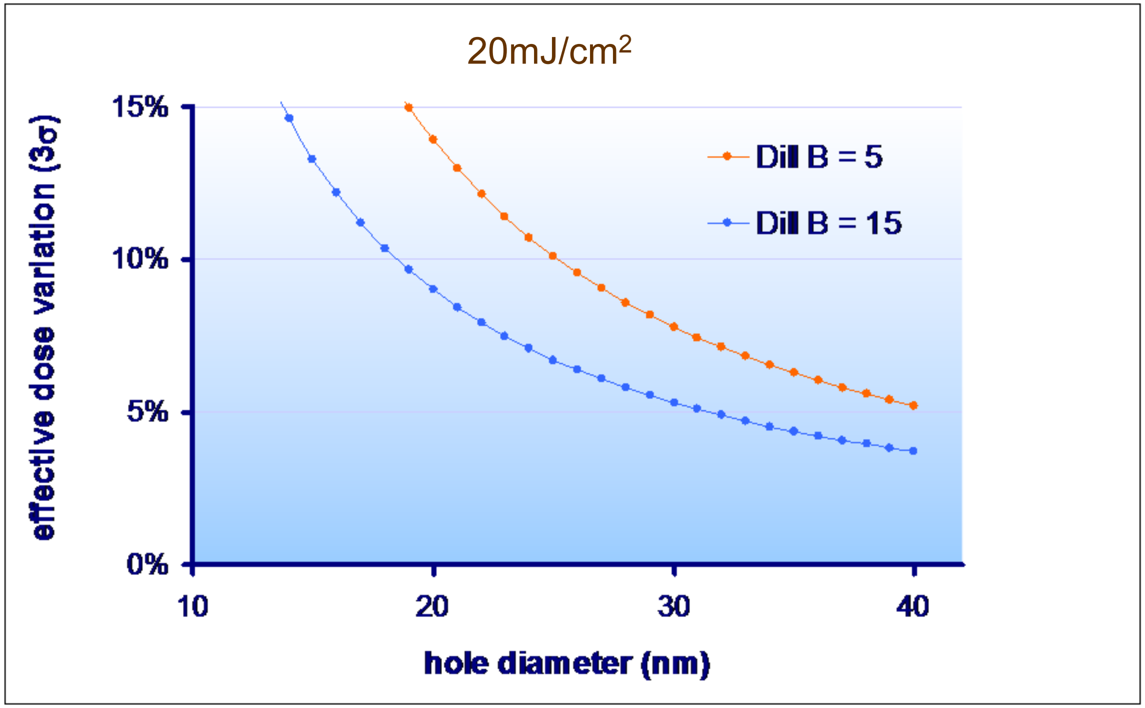


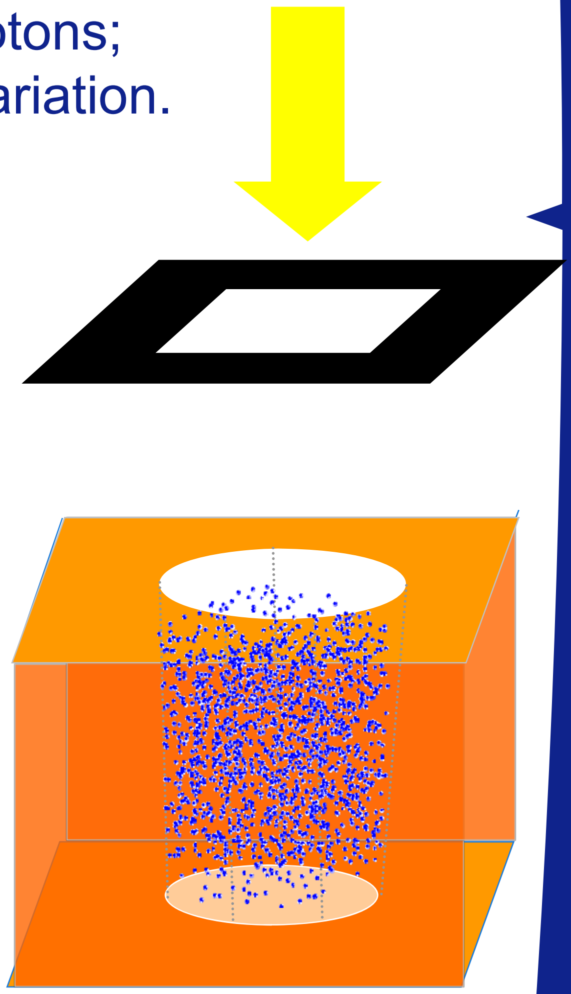
Printing limit can be estimated using a blurred image NILS cutoff, e.g. NILS=0.6 or 6% max dose latitude.

assumption: 0.9/0.2 Quasar, 3% flare, 3nm MSDxy

Shot noise limitations and resist

- Small features are imaged with relatively few photons; Statistical fluctuations create an effective dose variation.
- Resist can help by better absorbing the light.





$$\#\ photons = 0.67 * hole\ area * dose * image\ \ factor * (1 - \exp(-DillB * RT))$$

hole aspect ratio fixed at 2.5

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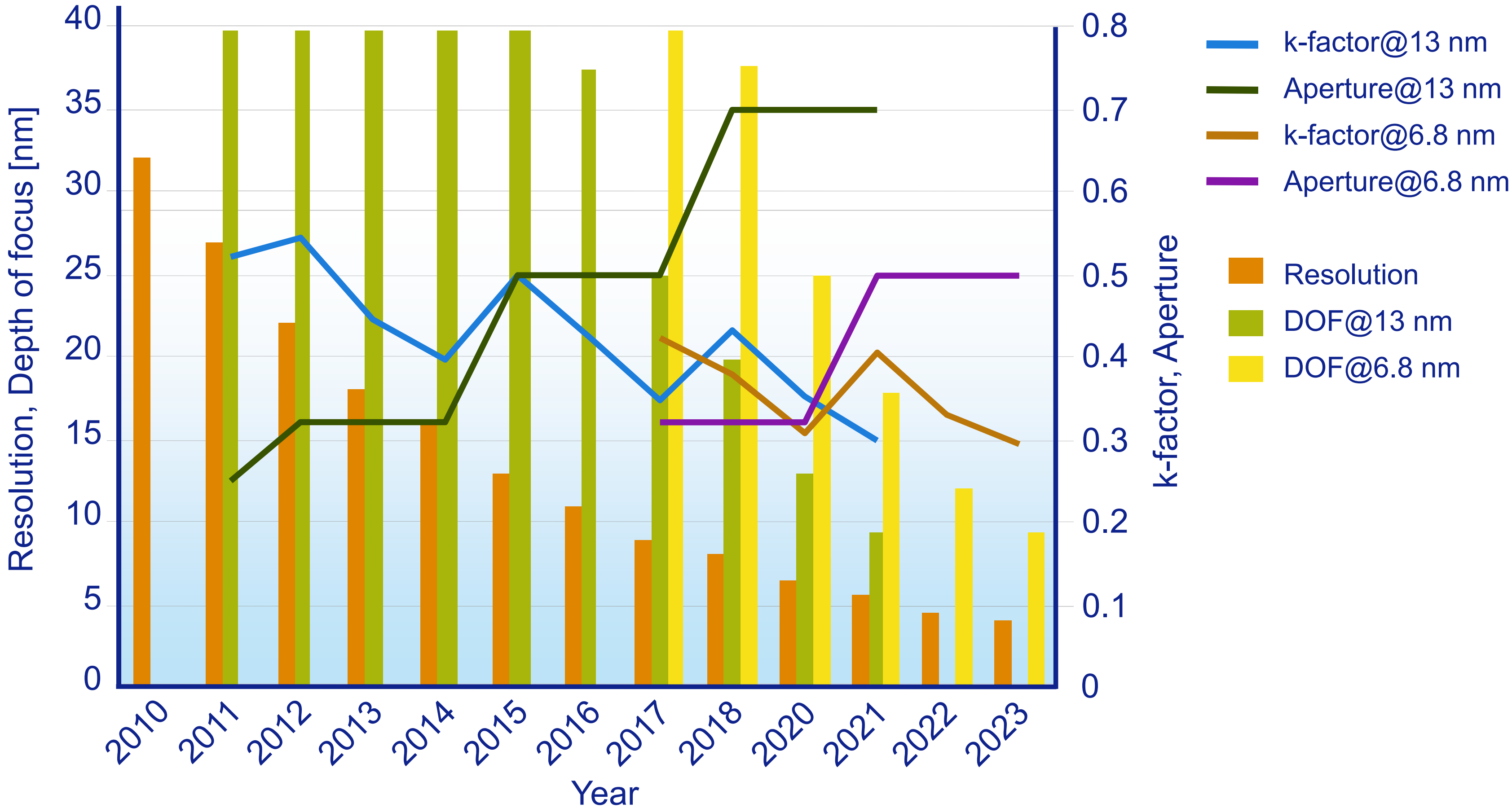
Agenda

- Roadmap
- Status
- Challenges
  - Critical issues
  - Extension of Shrink roadmap
- Summary & conclusion

Extendibility of EUV down to sub 5 nm possible

increasing apertures up to 0.7, wavelength reduction down to 6.8 nm using 13 nm compatible optics with depth of focus as the major challenge



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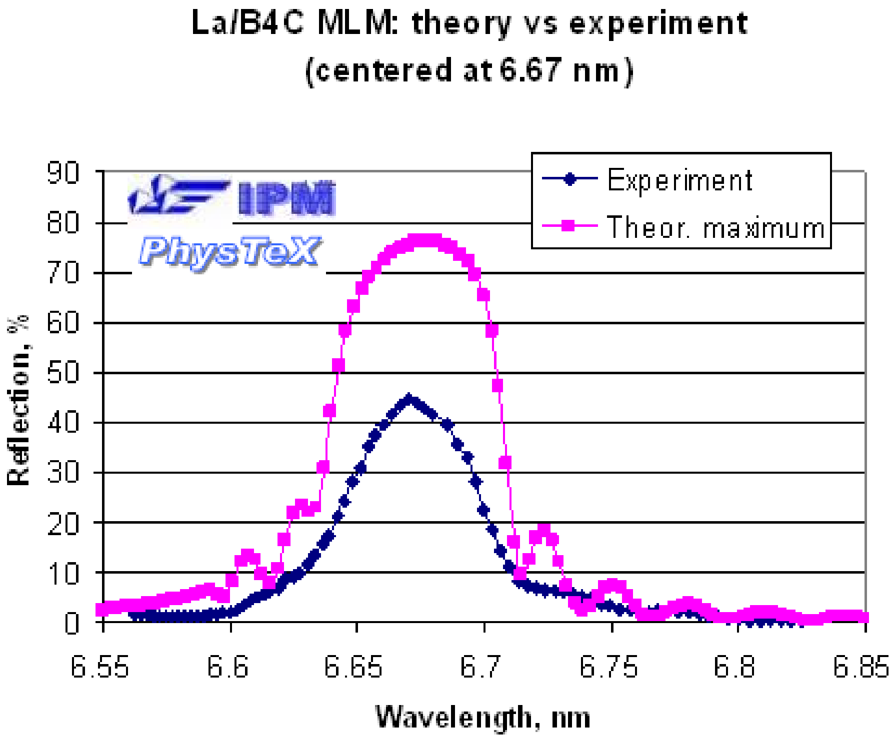
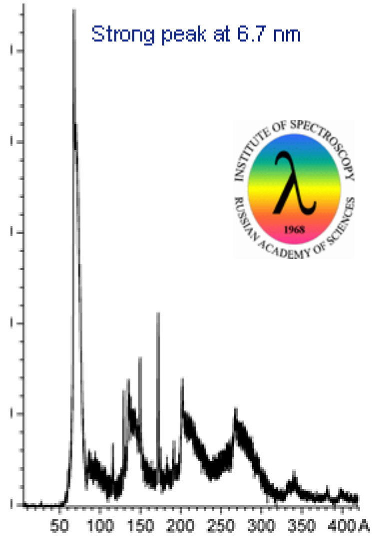
6.x nm wavelength would enable further shrink and/or increase depth-of-focus

- Shorter wavelengths have been investigated for lithography and other applications (e.g. water window microscopy).
- Criteria are
  - coating bandwidth and reflectivity
  - In-band source power,
  - resist sensitivity
- **Measured** source and coating performance





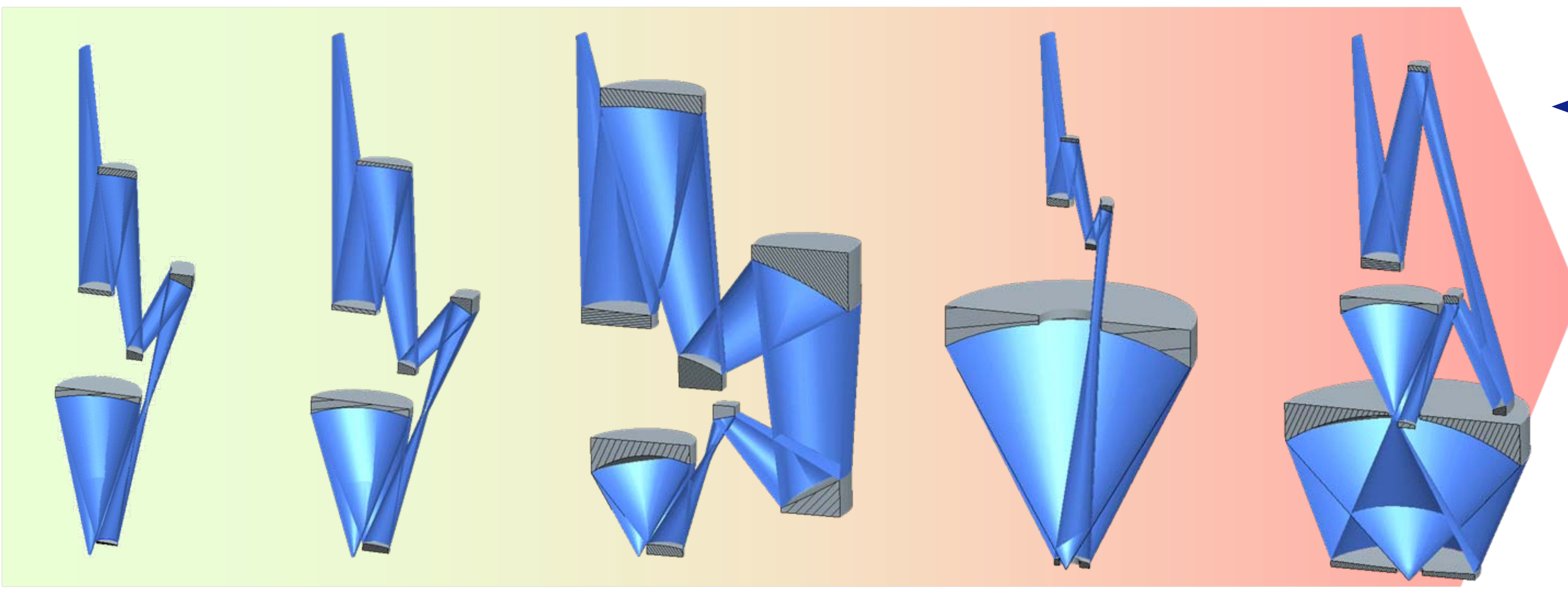
44.3% reflectivity is achieved
78% is theoretically possible

Achieved CE (in tool band) is 1.8%.
Further improvement to 3-5% is feasible

EUV extendibility possible beyond 10 nm resolution
trough increase the apertures up to 0.7

Apperture

•0.25 •0.35 •0.5 •0.7



6 mirror	6 mirror	8 mirror	6 mirror	8 mirror

● Unobscured ◎ Central obscuration

ZEISS

Reference: W.Kaiser et al, SPIE 2008 6924-4

Summary and conclusions

- EUV considered as the only cost effective way to continue Moore's Law.
- EUV has come a long way
    - 2 Alpha Demo tools used by customers since 2006
    - First tools on new production platform integrated and planned to ship before end 2010
- No new critical issues have surfaced which is good.
- Progress is steady however much more needs to be done in area of mask, source and resist.

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