Persistent Efforts to Overcome the Challenge of EUVL

Soichi Inoue
EUVL Infrastructure Development Center, Inc.
Trend of LSI Downscaling
Lithography Prospect
Technical Challenge for EUVL
Role of EIDEC
Persistent Efforts for Each Technology Development
  - Mask
  - Resist / Process
  - Source / Scanner
Summary
More Moore!

Number of transistors in a chip

- 1T
- 100B
- 10B
- 1B
- 0.1B

(Log₂)

(Log₁₀)

Intel CPU plots, except Ivy Bridge, are shown in http://www.intel.com/jp/technology/mooreslaw/index.htm?iid=jpIntel_tl+moores_law

- Intel CPU
- Ivy Bridge
  - 1.4B Tr.

- Fujitsu CPU
  - in Supercomputer "Kei"
  - 0.76B Tr.

- Panasonic DVD SoC
- Renesas Mobile SoC
- Rohm Graphic SoC

(Courtesy by JEITA)

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Trend of Downscaling

Gate length (nm)

- Planar Si-channel CMOS
- Dennard-scaling
- Booster-scaling
- 3D-scaling
- High-μ-scaling
- Quantum-scaling

SiON-base

High-k Low-k Metal G Strain

Fin SOI

Ge III-V

Nanowire Nanopillar Nanosheet

Cost Down

High Performance

Low Power Consumption

1nm = Four Si-atom length

Lg=6nm @2020

Lg=1nm @2030


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How About Is Millennial Roadmap?

Gold Stamp (AD100)
Dimension ~ 1mm

Microlithography in midlife crisis

Christopher P. Ausschnitt
IBM Advanced Semiconductor Technology Center
Hopewell Junction, New York

Minimum dimension (microns)

- Moore's Law
- We are here
- Industry roadmap
- Outlook

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Lithography Prospect

hp70nm  hp56nm  hp43nm  hp3xnm  hp2xnm  Next (=hp1xnm)

ArF (DRY)  ArF (Water Immersion)  EUVL

ArF Immersion Extendibility Double Patterning Technology

Nanoimprint

DSA

ML2

✓ Technology direction will be decided by development schedule, performance and economics.
✓ EUV lithography will be the main stream technology from cost and extendibility viewpoint.
Scenario of EUV Insertion

- EUV NA0.33
- EUV NA0.4x
- EUV NA0.6x ?

**Graph Details:**
- **x-axis:** Time (2010 to 2020)
- **y-axis:** Half Pitch [nm]
- **Markers:**
  - DRAM: Blue markers
  - Flash: Red markers
  - Logic-M1: Green markers

**Key Notes:**
- ArF imm + DPT
- ArF imm + QPT
- EUV NA0.33 + DPT
- EUV NA0.4x + RET
- EUV NA0.6x + RET
- λ = 6.x nm ?

**Legend:**
- DRAM
- Flash
- Logic-M1
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Technical Challenge for EUVL

**Source**
- High power: 250W @IF
- Stability
- Long Life of Collector Mirror

**Mask**
- Blank Inspection
- Patterned Mask Inspection
- Defect Review System
- Particle Free Handling

**Scanner**
- Field data
- Higher quality / Long lifetime of optical components

**Resist**
- Resolution < 20nmHP
- Sensitivity < 10mJ/cm²
- LER < 2nm
- Lower outgassing

Courtesy by EUVA
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**EIDEC Outlook**

- **Member Companies (16)**
  - Mask/Blank
  - AGC
  - DNP
  - HOYA
  - TOPPAN
  - Resist/Material
  - FUJIFILM
  - JSR
  - Nissan Chemical
  - Shin-ETSU Chemical
  - TOK
  - Device
  - Intel (USA)
  - Renesas Electronics
  - Samsung (Korea)
  - SanDisk (USA)
  - SK Hynix (Korea)
  - TOSHIBA
  - TSMC (Taiwan)

- **Focus Area**
  - Blank/Mask defect inspection
  - Resist development

- **Programs** *(EIDEC Project is supported by METI and NEDO)*
  1. Blank Inspection
  2. Patterned Mask Inspection
  3. Resist Materials
  4. Resist Outgassing Control

- **Phase Area**
  - Phase-1: hp 16nm
  - Phase-2: hp 11nm

- **Joining Companies (2)**
  - EBARA
  - Lasertec

- **Joining Research Institutes (3)**
  - AIST
  - Osaka University
  - University of Hyogo

*AIST: National Institute of Advanced Industrial Science and Technology

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Status of Mask Infrastructure

**Blank Inspector**
- EUV (Bright Field)
- EUV (Dark Field)
- 193 nm

**Patterned Mask Inspector**
- 199 nm
- EUV (13.5 nm)
- e-Beam (SEM, Projection)
- 193 nm

**Defect Reviewer**
- EUV-AIMS (13.5nm)

**Defect Repair Tool**
- GFIS
Challenges for “Effective” Phase Defect-free Blank

Defect Reduction

CD Impact (Real Defect Traceability)

Defect Inspection

Defect Review & Characterization

Defect Mitigation

- 24 nm L/S patterns
- Defect size: 90 nm, 60 nm, 50 nm
- Bump defect vs. Pit defect
- Multilayers vs. Substrate
- Fiducial mark & Defect compensation
- Fiducial mark vs. Defect mark
- Key issues: Reliable fiducial mark process, Defect coordinates accuracy, E-beam alignment
- SEMI standard meeting during SEMICON West (2009)

- Key issues: Defect review infra, Printing image estimation
- PML defect: Compensation for local intensity drop by local removal of absorber pattern

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LOVE Workshop 2012, June 4, 2012
Dark Field Actinic Blank Inspector (ABI)

- Bump defect
- Pit defect
- Multilayers
- Substrate

- Principle of Phase Defect Detection
- 2D-CCD
- EUV
- ML-Blank

- Wavelengths: 13.5nm, 193nm, 266nm, 488nm
Progress of Actinic Blank Inspector (ABI)

Higher sensitivity and throughput (16 and 11nm hp)

- 11nm hp W:35nm H:0.7nm
- 16nm hp W:50nm H:1.0nm
- >22nm hp W:55nm H:1.0nm

EIDEC ABI tool
MIRAI ABI tool

Inspection Time (Min)

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Current Status of Phase Defect

2-2. LTEM-ML blank defect trend @50nm SiO2

This is the updated defect trend of the LTEM-ML blank (LTEM substrate flatness <150nm). “NEW CHAMPION” defect density is 0.12/cm² (21 defects/plate) at 50nm SiO₂ w/M7360. The defect density at yield XX% has also been continuously decreased.

New Champion 21 defects/plate

* Courtesy: Intel for M7360 inspection

2011 International Symposium on Extreme Ultraviolet Lithography
Oct./19/2011
Requirement: Defect Hiding Process

- It takes a long time to achieve perfect blanks (no phase defect) with high yield.
- Industry requires to identify precise location of phase defects to mitigate them by shifting patterns and hiding them.
New Feature: Defect Review Mode

✓ Review optics enables to demagnify the corresponding pixel size of image sensor on wafer and to identify the position of phase defect with higher accuracy.
Patterned Mask Inspector (PMI) with EB Projection Optics

Basic Concept
- EB Projection Optics
- High Resolution
- High Throughput

Sensitivity of EBeyeM for Proto-type and 2Xnm with PDs on hp100nmLS Pattern

Previous Generation
- Program Defect Mask
- Sensitivity: < 30nm

The 24 nm-sized edge extension defect was successfully identified.
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Metric & Infrastructure for Resist Development

Infrastructure

SFET

Source \hspace{1cm} \text{Illuminator}

Resist Development

Resolution \hspace{4cm} \text{Sensitivity}

LER \hspace{4cm} \text{Outgassing}

All performance improvement are necessary

Outgas Test Setup

High Power EUV light

Resist Film

Contamination Film

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Small Field Exposure Tool: SFET

- Resolution $< 20\text{nmHP}$
- Sensitivity $< 10\text{mJ/cm}^2$
- LER $< 2\text{nm}$
- Low Outgassing

**Source** (Xe DPP)

**Exposure chamber**

**SFET**

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<table>
<thead>
<tr>
<th>Items</th>
<th>Spec</th>
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<tbody>
<tr>
<td>NA</td>
<td>0.3</td>
</tr>
<tr>
<td>Field size: mm</td>
<td>0.2 x 0.6</td>
</tr>
<tr>
<td>Magnification</td>
<td>1/5</td>
</tr>
<tr>
<td>Source power</td>
<td>0.5W @IF</td>
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</table>
Ultimate Resolution (Aggressive Dipole Illum.)

16nm L/S was resolved.

Exposure
- Tool: Canon SFET
- NA: 0.3
- Illumination: X-dipole
- Track: TEL ACT12
- Evaluation
- SEM: Hitachi CG4000
- Resist: 35nm Thickness


Proc. of SPIE Vol. 7696 79690Q-6
Outgassing from resist material generates contamination film on WS.

The outgas amount for cleanable (carbon) components is quantified by measuring the thickness of the contamination film.

Non-cleanable components can be characterized by XPS after cleaning the carbon contaminant by H₂ radical.
Outgas Evaluation Infrastructure in EIDEC

- EB-based Tool
  EUVOM-9000 (LTJ)

- EUV-based Tool
  HERC (Univ. of Hyogo)

- New SUBARU

- Spectroscopic Ellipsometer
  M-2000X (J.A.Woollam)

- H₂ Cleaner
  (EUVT)

- XPS
  Versa Probe II (ULVAC PHI)

✓ EB-based Outgas Evaluation Tool has been installed in Mar. 2012.
✓ EUV-based Tool also has been installed as a reference of EB-based tool.
✓ The metrology tools, i.e. Spectroscopic Ellipsometer (SE) and XPS, was certificated by exposure tool supplier.
Carbon Contamination

- Linear correlation for carbon contamination between EUV and EB was clearly observed.
- The carbon contamination was decreasing with increase in degree of polarity of the de-protected groups and polymer platforms. Polarity control is one of the key design parameters to reduce outgassing.
Contamination at Unexposed Area after Cleaning

Witness Sample (WS)

Unexposed Area
Exposed Area

TOF-SIMS Result

Unexposed Area
Exposed Area

C₄F₉SO₃ Concentration

High
Low

Fluorine was detected by XPS only at unexposed area of EUV sample.
TOF-SIMS indicated it was PAG anion compounds outgassed from resist.
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### EUV Focus Areas 2006-2010: 22 nm half-pitch insertion target

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<tr>
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</thead>
<tbody>
<tr>
<td>1. Reliable high power source &amp; collector module</td>
<td>1. Long-term source operation with 100 W at IF and 5MJ/day</td>
<td>1. Mask yield &amp; defect inspection/review infrastructure</td>
<td>1. Mask yield &amp; defect inspection/review infrastructure</td>
<td>1. Long-term reliable source operation with 200 W at IF*</td>
</tr>
<tr>
<td>4. Reticle protection during storage, handling and use</td>
<td>• Reticle protection during storage, handling and use</td>
<td>• EUVL manufacturing integration</td>
<td>• EUVL manufacturing integration</td>
<td>• EUVL manufacturing integration</td>
</tr>
<tr>
<td>5. Projection and illuminator optics quality &amp; lifetime</td>
<td>• Projection / illuminator optics and mask lifetime</td>
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*) This requires a 20 X improvement from current source power status

HVM introduction in late 2013 if productivity challenge can be met
EUV Light Source

LPP: Laser Produced Plasma
CO₂ Laser with Pre-Pulse Debris Mitigation
Magnetic Field (Gigaphoton)
Gas curtain (Cymer)

LDP: Discharge Produced Plasma
Laser Assisted Trigger
Rotating Electrodes for Heat Dissipation

EUVA/Komatsu/GIGAPHOTON
EUVA/USHIO/XTREME

Courtesy of Dr. Shinji Okazaki
New champion data of CE = 3.8% (Aug.2011)

- After CE optimization
  - 3.3% → 3.8% (@ pilot condition)

Results Summary

- Sn molecule measurement results
  - pre-pulse laser + CO2 laser irradiation: ionized 93% of Sn
  - Only pre-pulse laser irradiation: ionized 3% of Sn

Effect of Pre-pulse laser

- CE improvement
- Effective debris mitigation

The scanner supplier has already shipped 6 tools.
Basic performance, i.e. CD, OL has been validated.

Rudy Peeters, “EUV lithography: NXE:3100 is in use at customer sites and building of NXE:3300B has started,” EUVL Symposium Oct. 2011
## Status, Target & Persistent Effort

<table>
<thead>
<tr>
<th>Core Element</th>
<th>Current Status</th>
<th>Target</th>
<th>Persistent Effort</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source</td>
<td>~10W @IF</td>
<td>250W @IF</td>
<td>- Laser stability</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Droplet generator stability</td>
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<td></td>
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<td>- Debris mitigation</td>
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<td></td>
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<td>- OoB reduction</td>
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<tr>
<td>Scanner</td>
<td>- NXE3100 / CDU: 1.4nm, DCOL: &lt;1nm</td>
<td>Place NA0.33 to market in 2013</td>
<td>- Productivity</td>
</tr>
<tr>
<td></td>
<td>- φ-defect: 20-30/plate (&gt;50nm)</td>
<td></td>
<td>- φ-defect mitigation</td>
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<tr>
<td></td>
<td>- Particle:</td>
<td></td>
<td>- To establish ABI</td>
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<td></td>
<td></td>
<td></td>
<td>- Handling/cleaning/pellicle</td>
</tr>
<tr>
<td>Mask</td>
<td>- Resolution:16nm</td>
<td>Ideally: 0</td>
<td>- Thinner resist thickness</td>
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<tr>
<td></td>
<td>- Sensitivity: 30~mJ/cm²</td>
<td></td>
<td>- Hardmask process, bias control</td>
</tr>
<tr>
<td></td>
<td>- LWR: ~ 5 nm</td>
<td>- 11nm</td>
<td>- LWR: build up consensus</td>
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<tr>
<td></td>
<td></td>
<td>- 10mJ/cm²</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>~ 1.1 nm</td>
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<tr>
<td>Resist/Process</td>
<td>Small experience</td>
<td>Ready for HVM</td>
<td>Learn more</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>- Defectivity</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>- Total CD control</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>- Total OL control</td>
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<tr>
<td>Litho Integration</td>
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</table>
Summary

- Downscaling of LSI still makes sense for the cost reduction, performance improvement and power consumption.
- EUV lithography will be the main stream technology from cost and extendibility viewpoint.
- However, some key technologies still have fundamental issues. Persistent efforts are necessary to overcome the challenge for realizing EUVL.
- The source no doubt needs to increase in power dramatically and reach the set targets (main & pre-pulse laser, debris mitigation, droplet generation, IR reduction) with sufficient stability.
- The development of EUVL infrastructure, i.e. mask inspection, resist, etc. in consortia is a reasonable approach for reducing cost of pre-competitive technology development.
- The persistent efforts including the EUVL infrastructure development will definitely ensure the realization of EUV lithography.
The part of this work was supported by New Energy and Industrial Technology Development Organization (NEDO).
Thank you for your attention !!