EUVL Challenges for Next Generation Devices

Center for Semiconductor Research & Development
Advanced Lithography Process Technology Dept.

Tatsuhiko Higashiki
Contents

- Device Roadmap and Lithography
- Extendibility toward 1x nm hp and beyond with New Lithography
  - SAxP
  - EUVL
  - EUVL+DSA
- Conclusion
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Rapid Increase of Information Volume Demand

All information that is created, captured, replicated and/or consumed by all human on the planet.

All information is not fully stored, but partially stored.
⇒ Need for larger-capacity memory in the future.
Roadmap of the Memory

BiCS

Cross Point

NAND

Continue the FG technology to the limit.

Introduction of the super high capacity die with small die size.
Lithography Challenges

More Moore

hp56nm  hp43nm  hp32nm  hp2xnm  hp1xnm  hp0xnm

ArF im

NA > 1 ~ 1.35

EUVL

NA 0.32 → > 0.4x ?

EUVL + SADP

Resist, Mask, Inspection, etc

EUVL + DSA

Cost

ArF im SADP

ArF im SAQP/SAOP ?

ArF im SAQP + DSA

NIL

NIL + DSA

ML2

ML2 + DSA

SADP: self-aligned double patterning
SAQP: self-aligned quadruple patterning
SAOP: self-aligned octuplet patterning
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More than Moore

ArF im SADP

Defect

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Performance & Economics

NIL + DSA

ML2 + DSA

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SADP : self-aligned double patterning
SAQP : self-aligned quadruple patterning
SAOP : self-aligned octuplet patterning
Single Exposure by Mask Technology Revolution

**SADP**

Exposed

**Mask (Template)**

Processed

Litho.

Slimming

Film depo.

etching

etching

single

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Cycle time can not be described on CoO

Single Exposure

DPT

DPT Economical Problems

- Investment Cost (LP, Etching, M&I, etc.)
- Mask Cost
- Opportunity Cost (“Time is money”)
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EUVL Challenges for NAND Memory

Mask Defect Control DD<0.1/cm²
✓ Inspection
- ABI (Actinic Blanks Inspection)
- PI (Pattern Inspection)
- Inspection after Pattern Repairing

Resist Performance
Resolution<16nm, LWR<2nm, Photo Speed<20mj/cm², Defectivity<0.1/cm²

Light Source Performance
Enough Power for Throughput>150wph
Operational Cost (Mirror, E Power, DMT, etc)
EUV Source Power Progress reaching 55 W
Supporting 43 Wafers/hr, 250 W target to be reached in 2015

At 55 W, 1 run:
97.5% of the dies < 0.5% dose

At 40 W, 6 runs:
99.99 of the dies < 0.2% dose,
7 one hour runs total representing ~ 250 exposed wafers @ 15 mJ/cm²
EUV Collaboration

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Device & design

Si Process

Lithography
  - Pattern Layout Tech. (OPC/DFM)
  - Specification Design for Tools
  - Mask process
  - Resist process

Advanced EUVL

Mask Quality
Mask Inspections
 Resist Quality
High NA Exposure
EUVL+DSA

Suppliers

Exposure Tool EDA
Resist Material Mask
Metrology and Inspection
Structure of EUVL Mask

EUV Mask Section and Defects

- Absorber
- Phase Defect
- Pattern Defect
- Damage after repairing
- Reflective Multilayer

Ref T.Higashiki  ConFab2010(June)
ABI Chronicle

- TDI camera
- SS optics
- EUV light
- EUV blank
- Scattering ray by defect
- Bump defect
- Pit defect
- Multilayers
- Substrate
- Substrate

ABI coherent development strategy

HVM by EIDEC (2011-)
ABI for hp16nm HVM
w/ Lasertec

Proto by MIRAI-Selete (2006-2010)
Full mask area ABI inspection

POC by MIRAI I,II (2001-2005)
Feasibility of ABI,
dark field ABI by AIST

Ref H.Watanabe, EIDEC Symposium 2013
EB inspection tool

Sensitivity: Similar to SEM

- Electron Gun
- Detector
- EUV Mask

Throughput: Similar to Optical

- 19Xnm Laser
- EUV Mask
- Objective Lense
- Sensor

EBeyeM

- Continuous Moving (Y)
- Stepping (X)
Quality assurance of hotspot & repaired pattern

- EUV AIMS operation will be difficult in 2012.
- 3D SEM + Litho. Simulation will be applied.

- Top-down & tilted SEM images of mask pattern
- Prediction of wafer image
- Lithography simulation
- 3D mask image
# Toshiba Technology Scenario for EUV Mask

<table>
<thead>
<tr>
<th></th>
<th>HP 2Xnm</th>
<th>HP 1Xnm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Multilayer defect inspection</strong></td>
<td>DUV inspection</td>
<td>Actinic inspection</td>
</tr>
<tr>
<td><strong>Patterned mask inspection</strong></td>
<td>DUV inspection</td>
<td>EB inspection</td>
</tr>
<tr>
<td><strong>Defect repair</strong></td>
<td>EB repair</td>
<td></td>
</tr>
<tr>
<td><strong>Hotspot &amp; repaired pattern assurance</strong></td>
<td>Litho. Sim. w/ 3D mask image</td>
<td>EUV-AIMS</td>
</tr>
<tr>
<td><strong>Particle inspection</strong></td>
<td>EB inspection</td>
<td></td>
</tr>
</tbody>
</table>

*ready*

*under developing*
Absorber Pattern Generation

EB writer: "EBM8000"
(NuFlare)

Dry Etching Equipment: "ARES™"
(Shibaura Mechatronics)

Iino, et al. (BACUS2010)

Scanning-type Developer: "PGSD"
Proximity-Gap-Suction-Development System
(Tokyo Electron)

- Slit and scan type development
- Narrow gap
- Suction slits for removing dissolution products

Etched absorber pattern has capability for scaling down to hp1x EUVL single exposure.
“SMRAT Network of Mask & Lithography”

Toshiba R&D Center
- DTF
  - Mask House

NuFLARE
- EB Writer
- Inspection
- Cleaning Tech.
- Etching

Toshiba Advanced Litho.& Mask Dept.
- Advance Mask & Litho
- Computational Litho
- OPC/DFM
- Next Emerging Litho.

(EUVL Infrastructure Development Center)
- Mask Inspections
- High Performance Resist
- Sub-10nm DSA material

Toshiba Confidential
Resolution Limit of EUVL

Depend on Resist Performance

 hp32nm
 hp25nm
 hp22nm
 hp17nm
 hp16nm
 hp9nm

HP nm

NA

K1=0.41
K1=0.6
K1=0.41/2 (Spacer)
hp14nm Exposure was Realized by EUVL + SADP

Y. Watanabe et al, Photomask Japan 2010(April)
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Si Process

Advanced EUVL
- Mask Quality
- Mask Inspections
- Resist Quality
- High NA Exposure
- EUVL+DSA

Suppliers
- Exposure Tool EDA
- Resist Material Mask
- Metrology and Inspection
**DSA (Directed Self Assembly)**

- **Composition**
  - Spherical
  - Cylindrical
  - Bicontinuous
  - Lamella

- **Change in Size**
  - Molecular Weight

- **Change in Structure**
  - Hydrophilic
  - Hydrophobic
  - Chemical bond

**Micro-Phase Separated Structures of Block-copolymer**

DSA (Directed Self Assembly)

BCP: Block copolymer

Line & Space

Contact Hole
Grapho-Epitaxy & Chemo-Epitaxy


Tada, Macromol.41,9267(2008)
Guide Hole vs. DSA Hole

Guide hole

Ave. CD 72.1nm
3sigma 7.6nm

DSA hole

Ave. CD 28.5nm
3sigma 1.3nm

Ref. Y. Seino, SPIE Advanced Lithography 2012 8323-33
### DSA Simulation Model

#### Prediction vs. Accuracy

<table>
<thead>
<tr>
<th>Model</th>
<th>Self Consistent mean Field</th>
<th>Dissipative Particle Dynamics</th>
</tr>
</thead>
<tbody>
<tr>
<td>methodology</td>
<td>Based on statistical field theory</td>
<td>Based on Newton's motion equation</td>
</tr>
<tr>
<td>Challenge</td>
<td>Modeling of thermal fluctuations</td>
<td>Difficult to fit to a measured data</td>
</tr>
</tbody>
</table>

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**Impractical model**

- Shroedinger's Equation etc
- Rigorous Model
- Scattering

**Target**

- TAT (1m/10μm²)
- (<0.25nm)

**Needs drastic improvement!!**

- SCF
- DPD
- TAT (5h/10μm²)
- (5nm)

- TAT (? years/10μm²)

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34
**DSA Simulation Model**

- **Molecular Dynamics based**
  - Coarse Grained MD
  - DPD (Dissipative Particle Dynamics)

Available Free Software Tools are:

- LAMMPS
- GROMAX
- OCTA-COGNAC

**Equation:**

\[
m_i \frac{d^2 r_i}{dt^2} = F_i = \sum_{j \neq i} (F_{ij}^S + F_{ij}^C + F_{ij}^D + F_{ij}^R)
\]

- Coarse Graining
- Dissipative Force
- Repulsive Force
- Beads
- Spring Force
- Brownian Motion
- Solvent
- Δ velocity
Challenges for DSA Lithography

- **High performance DSA material**
  - High $\chi$ material
  - Resolution, LWR/LER, Etching
- **Long term stability**
  - Robust material and tool for environmental control such as surface energy stability, temperature, humidity, pressure and PH, etc.
  - Defectivity, CD and overlay accuracy
- **Development of molecular dynamics based DSA simulator**
  - More accurate simulation model
    - BCP and related molecular design
    - Microphase separation (2D/3D)
  - TAT / accuracy trade-off
- **DSA OPC/DFM technology**
  - Design rule verification
  - DSA and guide patterning (litho/wet/dry)
- **Metrology & Inspection**
  - Metrology for 3D profile
  - Inspection technology for 1xnmp and beyond needs to overcome throughput / accuracy / sensitivity trade-off.
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- Economical factor is dominant criteria for a lithography strategy
  - For Memory Device; Throughput, Investment & Si Process Cost
  - For Logic Device ; Mask Cost, Cycle Time

- EUVL
  - Moving from R&D phase to production
  - Light source performance is improving, but a significant concern.

- DSA
  - DSA will be a complementary technology for all other lithography
  - EUVL+DSA will be one of candidates for sub 10nm lithography.

◆ Next Challenges
  - Next generation lithography will depend on innovation of infrastructure technologies such as OPC, DFM, M&I, etching and cleaning.
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