2015 International Workshop on EUVL

Keynote Presenter

Mark Phillips

Mark Phillips is a Senior Principal Engineer in Intel's Logic Technology Development group in Hillsboro, Oregon. After completing a PhD in Physics from the California Institute of Technology, he joined Intel 21 years ago to work on development of the 0.35 micron process node. For the last 12 years, he has been the primary technical interface to Intel's exposure tool suppliers, and has worked on the introduction of every new generation of exposure tool into technology development and manufacturing. In the last few years, Mark has also been responsible for defining the roadmap for the factory automation systems that support Intel's lithography tools, and has worked on introduction of new metrology techniques to support lithography.

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