Continued Scaling in Semiconductor Manufacturing with Extreme-UV Lithography

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As EUV lithography goes into high-volume manufacturing in 2019, the focus of the lithography community is shifting from "if and when" to "how well" EUV will enable the continued scaling of integrated circuits. For semiconductor manufacturing with EUV lithography beyond the first generation, several fundamental topics are being addressed to enable single-patterning EUV lithography at lower k1 values. Such topics include resolution and etch-resistance of the photoresist, the stochastic nature of the photon-resist interaction, the three-dimensional nature of the photomask, the mask-side non-telecentricity of the reflective imaging optics, etc. Mitigation of the side effects produced by the aforementioned aspects of the EUV lithography will allow it to extend into the initial years of the next decade with minimal use of double patterning. Minimization of these effects is also essential for the adoption of the high-NA (0.55) EUV exposure system, which is presently under development at ASML and whose goal is to enable EUV lithography to provide continued scaling in semiconductor manufacturing well into the next decade.

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Anthony (Tony) Yen is ASML's VP and Head of Technology Development Centers Worldwide. Prior to the current position, he was with TSMC (2006 – 2017) where he led the development of EUV lithography, including its mask technology, for high-volume manufacturing. Earlier in his career, he was a researcher with Texas Instruments (1991 – 1997) where he worked on various techniques, including early work on optical proximity correction, to enhance the practical resolution of microlithography. From 1997 to 2003, he was with TSMC where he led the group that developed lithography processes for TSMC's 0.25, 0.18, 0.15, and 0.13 micron generations of logic integrated circuits and then co-led infrastructure building for next-generation lithography technologies at SEMATECH. From 2003 to 2006 he was with Cymer where he headed its marketing organization. Tony graduated from Purdue University with a BS degree in electrical engineering and furthered his education at MIT, earning his SM, EE, PhD , and MBA degrees there. He has over 100 US patents and 90 publications. He is a fellow of SPIE and of IEEE.