EUV Lithography at the Threshold of High Volume Manufacturing

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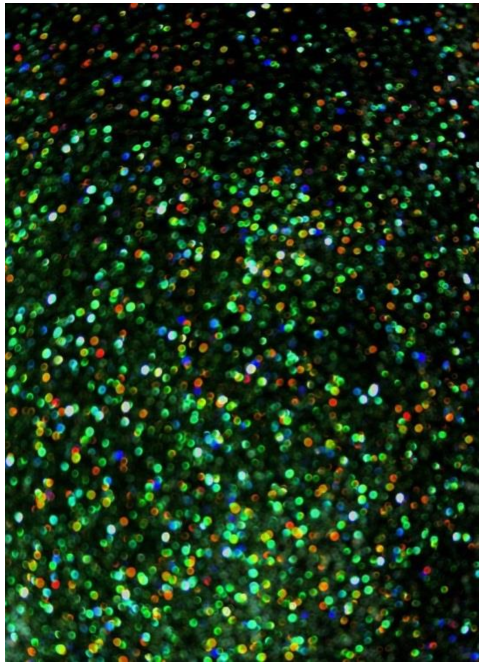
GLOBALFOUNDRIES®

My first lithographic process

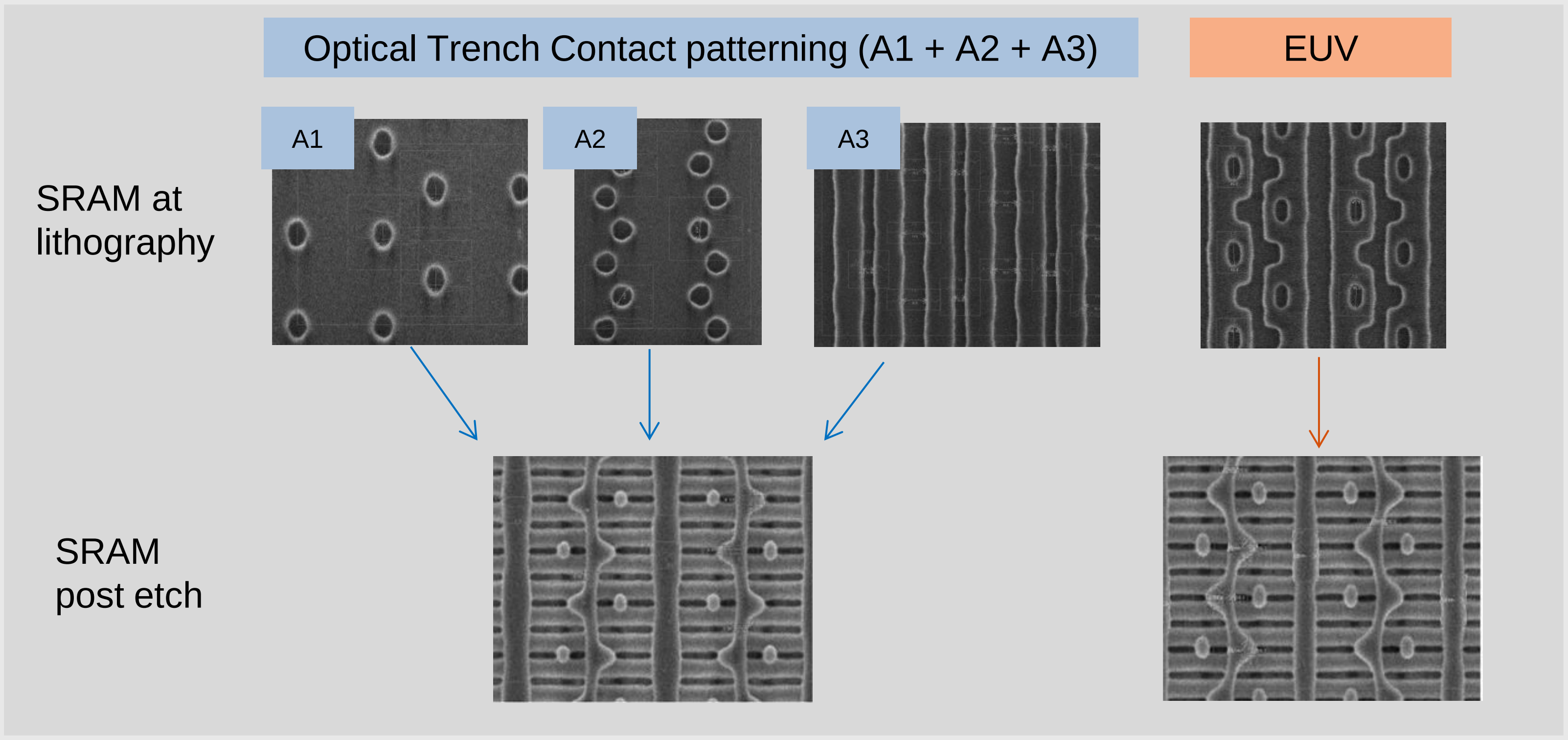
Prior to patterning the first lot of integrated wafers:

- ✓ Optimized a high resolution resist process
- ✓ Film stack made more lithography-friendly using Abeles transfer-matrices
  - ✓ Included design of anti-reflection coatings to metal layers
- ✓ Simulated process windows
  - ✓ Optimized mask bias



A theoretically sound lithographic process can be derailed by a broken valve

Most recent lithographic process



Optical Trench Contact patterning (A1 + A2 + A3)

EUV

A1

A2

A3

SRAM at lithography

SRAM post etch

- Trench contact
  - Optical 193i LE^3 approach was replaced with a single exposure EUV and a single etch
- Results from the two patterning approaches are similar
  - Electrical performance
  - Yield

Considerations for HVM

- As we start-up EUV lithography in HVM, focus will be on practical issues
  - Equipment reliability
  - Other factors that affect die costs
  - Yield
  - Particles on masks
  - Process control

Equipment reliability is critical, significantly affecting:

Capital efficiency

Maintenance costs

Rework

Cycle time

Fab capacity

Equipment reliability is critical, significantly affecting:

Capital efficiency

$$\text{Contribution of capital to wafer costs} = \frac{\text{Capital depreciation}}{\text{Throughput x Uptime}}$$

Uptime ↑ = Costs ↓

Time is money

Length of time	Capital cost
5 years	€100M

Time is money

Length of time	Capital cost
5 years	$116.6M

Time is money

Length of time	Capital cost
5 years	$116.6M
1 year	$23.3M
1 month	$1.94M
1 week	$448k
1 day	$64k
1 hour	$2.7k
My 40 min. talk	$1.8k

Equipment reliability is critical, significantly affecting:

Maintenance costs

- Maintenance technicians
- Replacements for components that break
- Components that degrade
  - Collector mirrors
- Inventory costs for spare parts

Equipment reliability is critical, significantly affecting:

Wafers require rework when processed on malfunctioning equipment

Rework

Equipment reliability is critical, significantly affecting:

Cycle time

- Re-queue
- Particularly problematic if tool dedication is required

Equipment reliability is critical, significantly affecting:

Downtime limits productivity of bottleneck tools

Fab capacity

Equipment reliability is critical, significantly affecting:

Capital efficiency

Maintenance costs

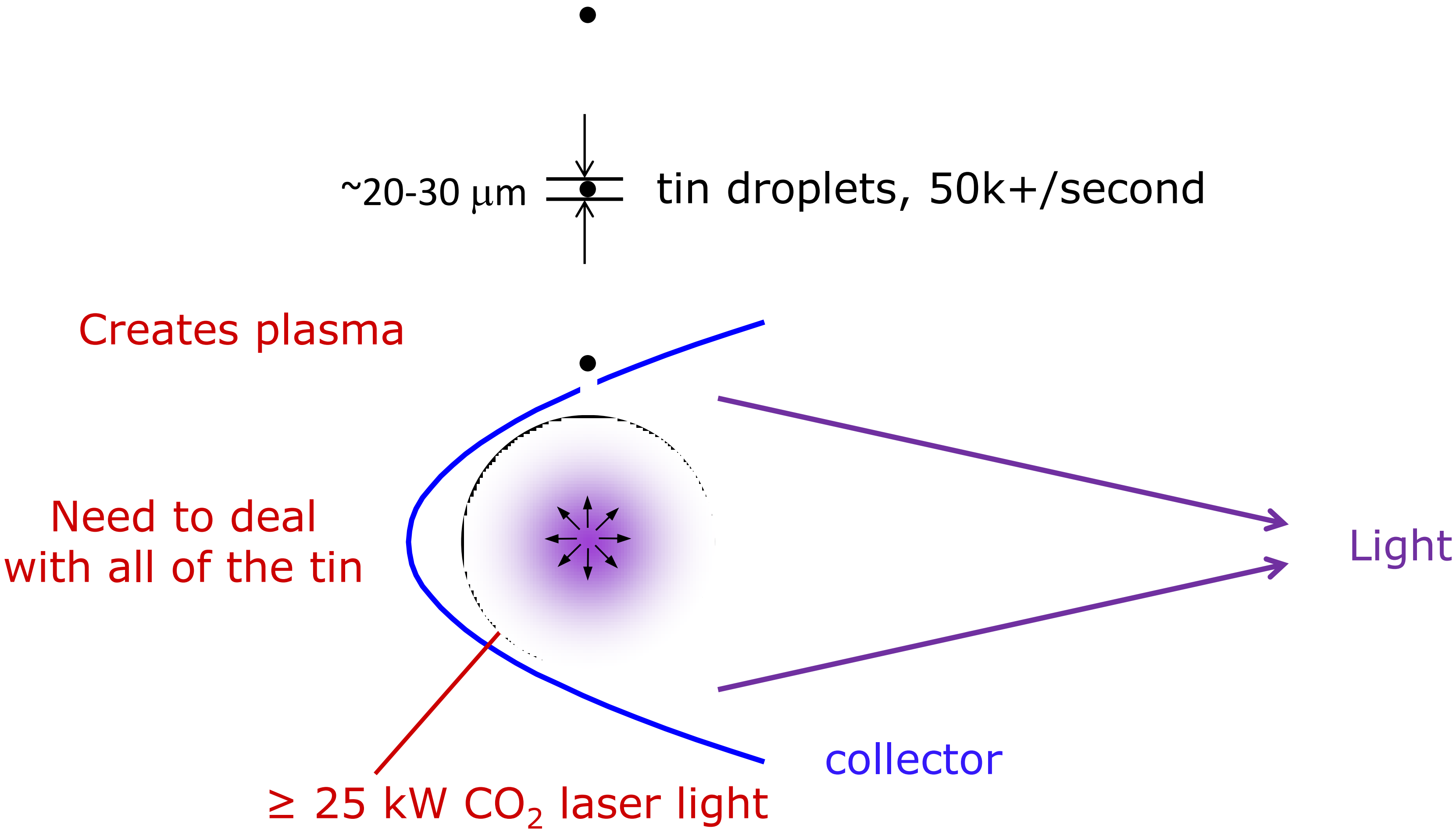
Rework

Cycle time

Fab capacity

Between invention and reliability is a lot of work

The biggest problem is the light source



Equipment reliability

Source type	Repetition rate
Excimer laser	6 kHz
EUV laser-produced plasma source	50 kHz

8.3×

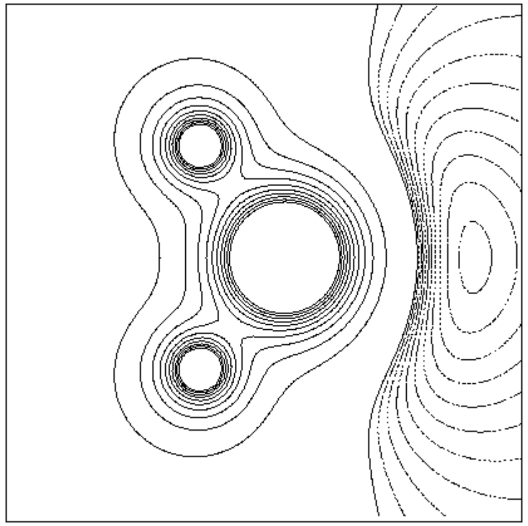
"Now, here, you see, it takes all the running you can do, to keep in the same place.

“If you want to get somewhere else, you must run at least ~~twice~~ as fast…!"

8.3×

The Red Queen
in *Alice Through the Looking Glass*

EUVL equipment reliability: vacuum



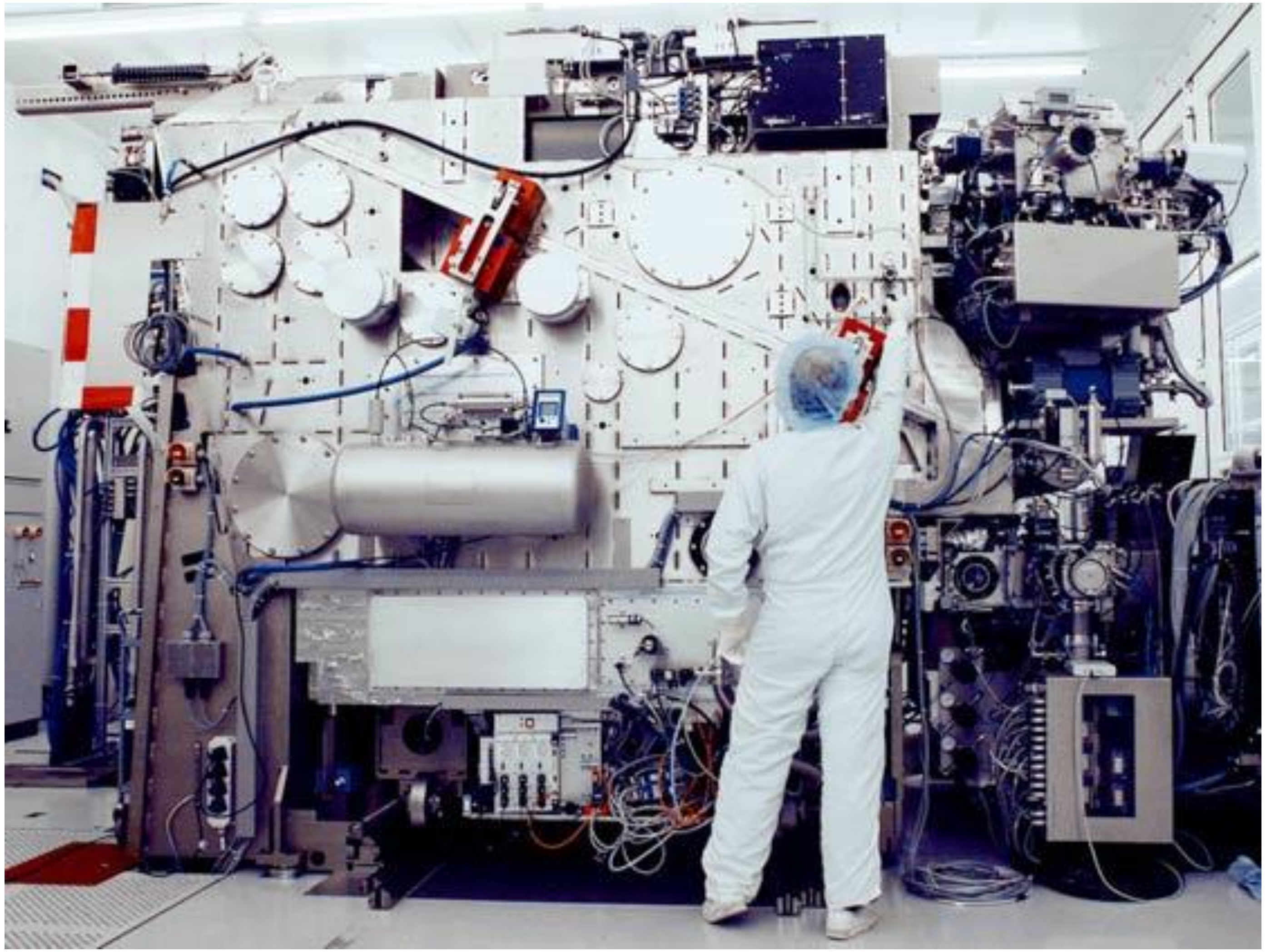
Water and carbon monoxide are polarized molecules that stick to walls and parts, but not strongly.

⇒ It takes a long time to achieve ultra-high vacuum.

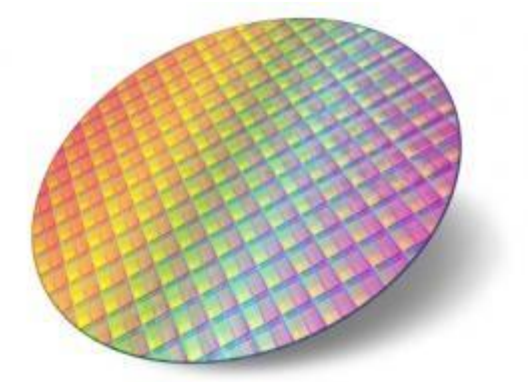
Several hours required to re-establish vacuum every time the chamber is opened.

time = $$$

Optics, wafers, and masks are in a vacuum



Vacuum causes headaches for process control



Coefficient of thermal expansion of silicon $= 2.6 \times 10^{-6}/^{o}C$

For $0.1^{o}C$ temperature increase, length change across 20 mm = 5 nm

Heat (q) per area (A) transferred by air flowing at velocity v across a surface:

$$\frac{q}{A} = h_c \Delta T$$

$$\approx (10.45 - v + 10\sqrt{v})\Delta T$$

$\approx 2\ \mathrm{W/cm^2}$ for v = 1 m/s and $\Delta T = 0.1^{o}$ C

Radiative heat transfer:

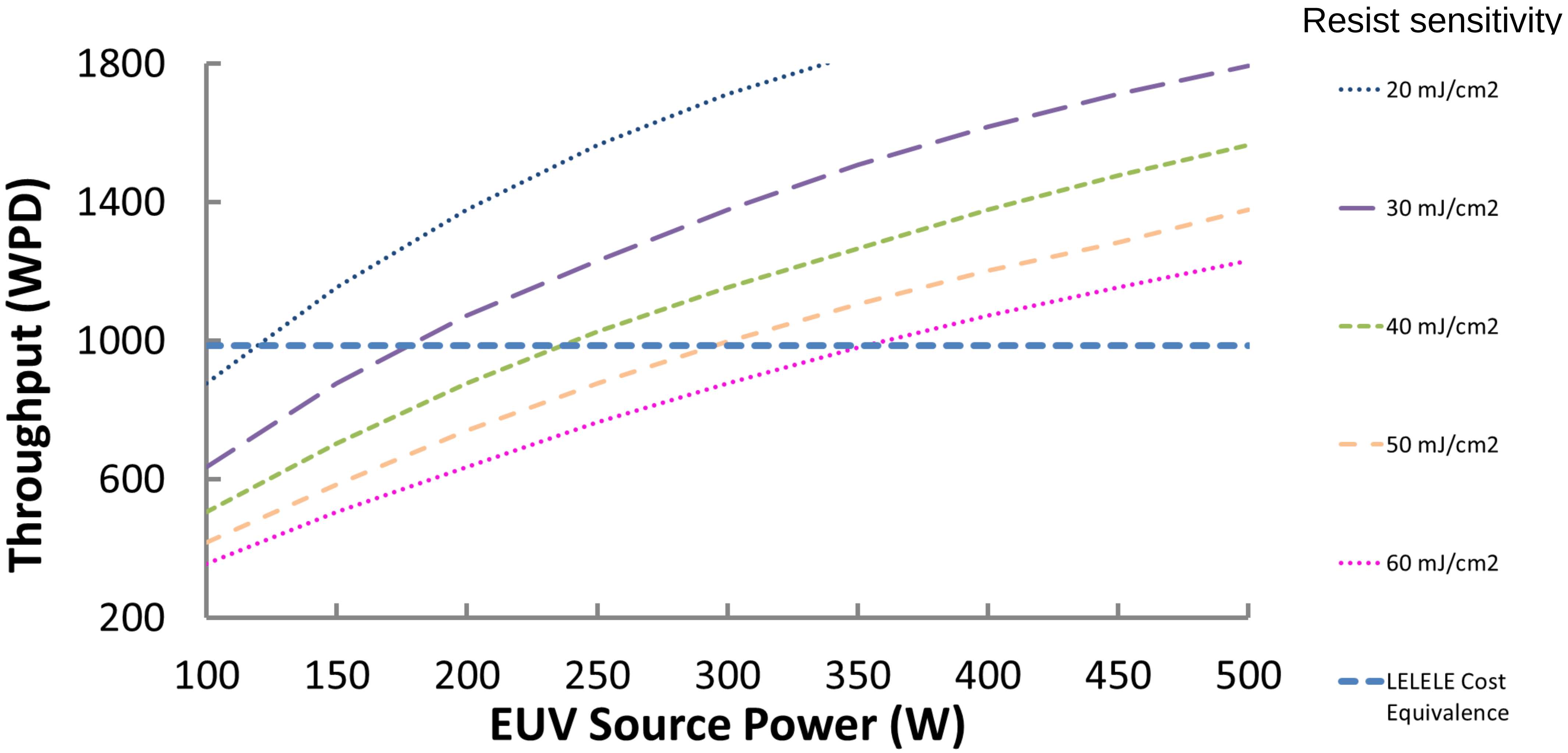
$$\frac{q}{A} = \frac{\sigma\left(T_1^4 - T_2^4\right)}{\frac{1}{\varepsilon_1} + \frac{1}{\varepsilon_2} - 1} \approx 0.2\ \mathrm{W/cm^2}$$

Silicon (ε_1) Anodized aluminum (ε_2)

Reliability is just part of productivity

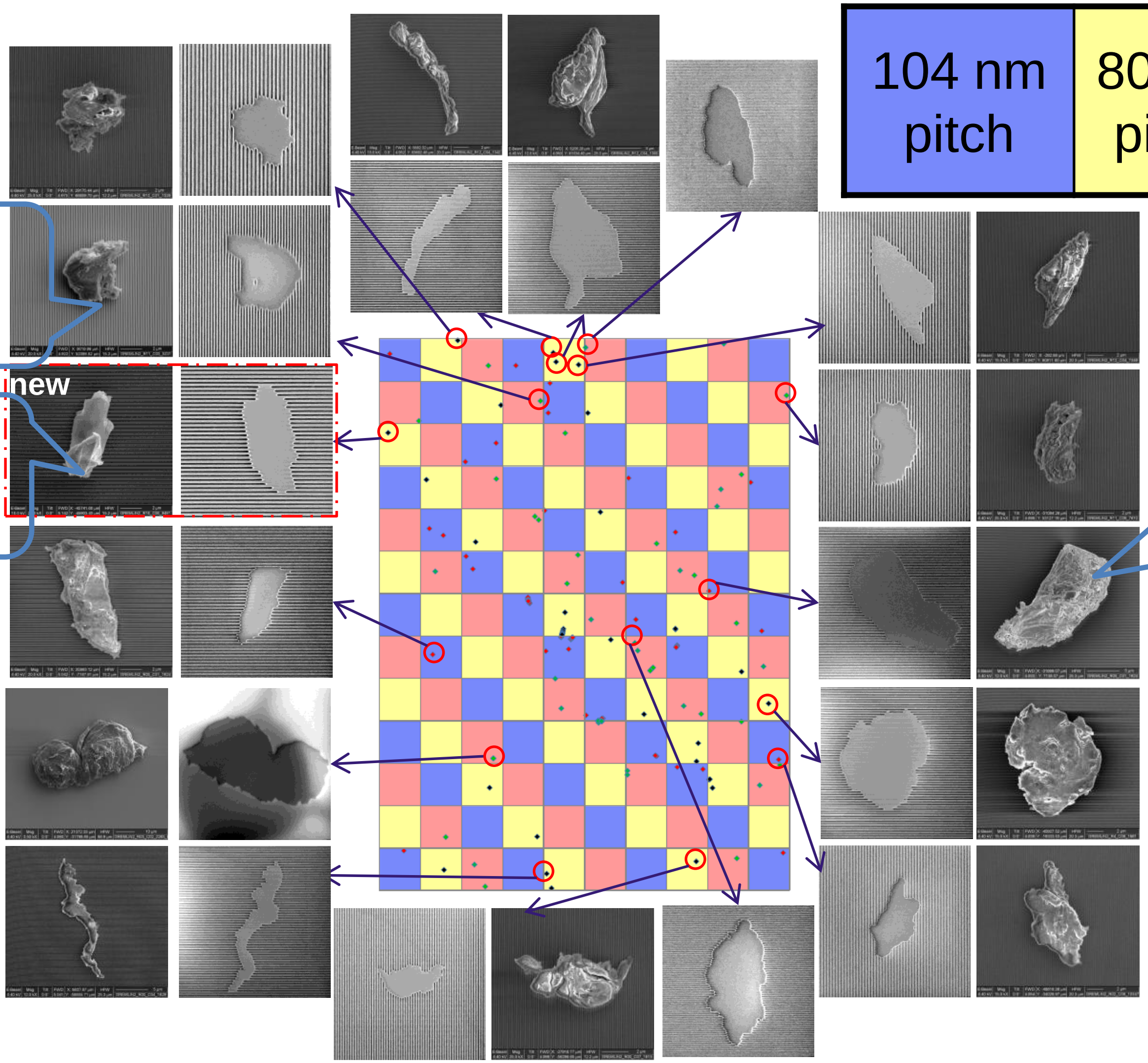
Today: 50 mJ/cm^2

2016: 120 mJ/cm^2



Graph courtesy of Erik Hosler

Mask contamination from Alpha Demo Tool (ADT)



104 nm pitch

80 nm pitch

56 nm pitch

AlO$_x$ with trace Fe, Zn, Mg

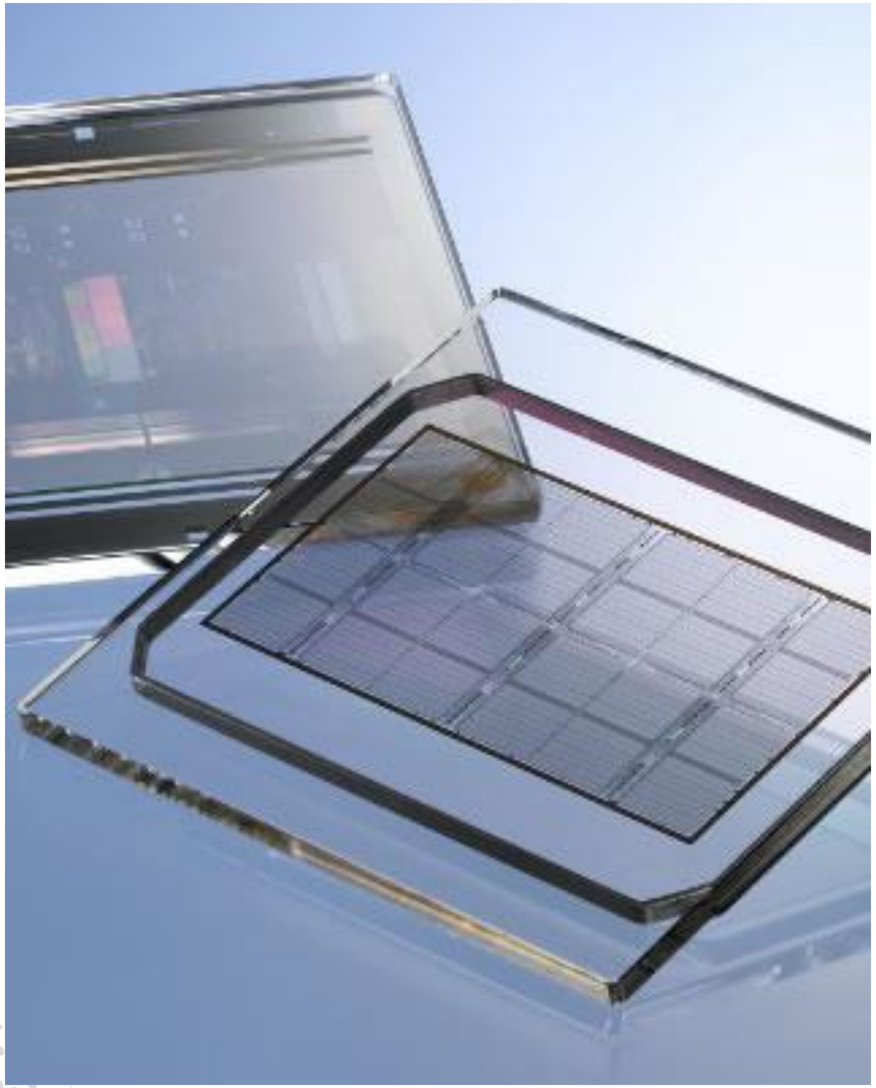
Mo with S, C, Si, O

Mo with S, C, O

From defect study by Dr. Xuelian Zhu, GLOBALFOUNDRIES

Mask contamination

Pellicles (and lack thereof)



- The lack of an HVM-worthy pellicle has significant impact on
  - Process flow
    - Wafers need to be held while masks are being qualified
      - Significant impact for low to medium volume products
    - Situation is particularly problematic when masks have defects
      - Rework
      - Interrupted production while masks are being cleaned or greater masks costs incurred for duplicate masks

Pellicles (and lack thereof)

- Additional costs
  - Inspection tools
  - Mask cleaner

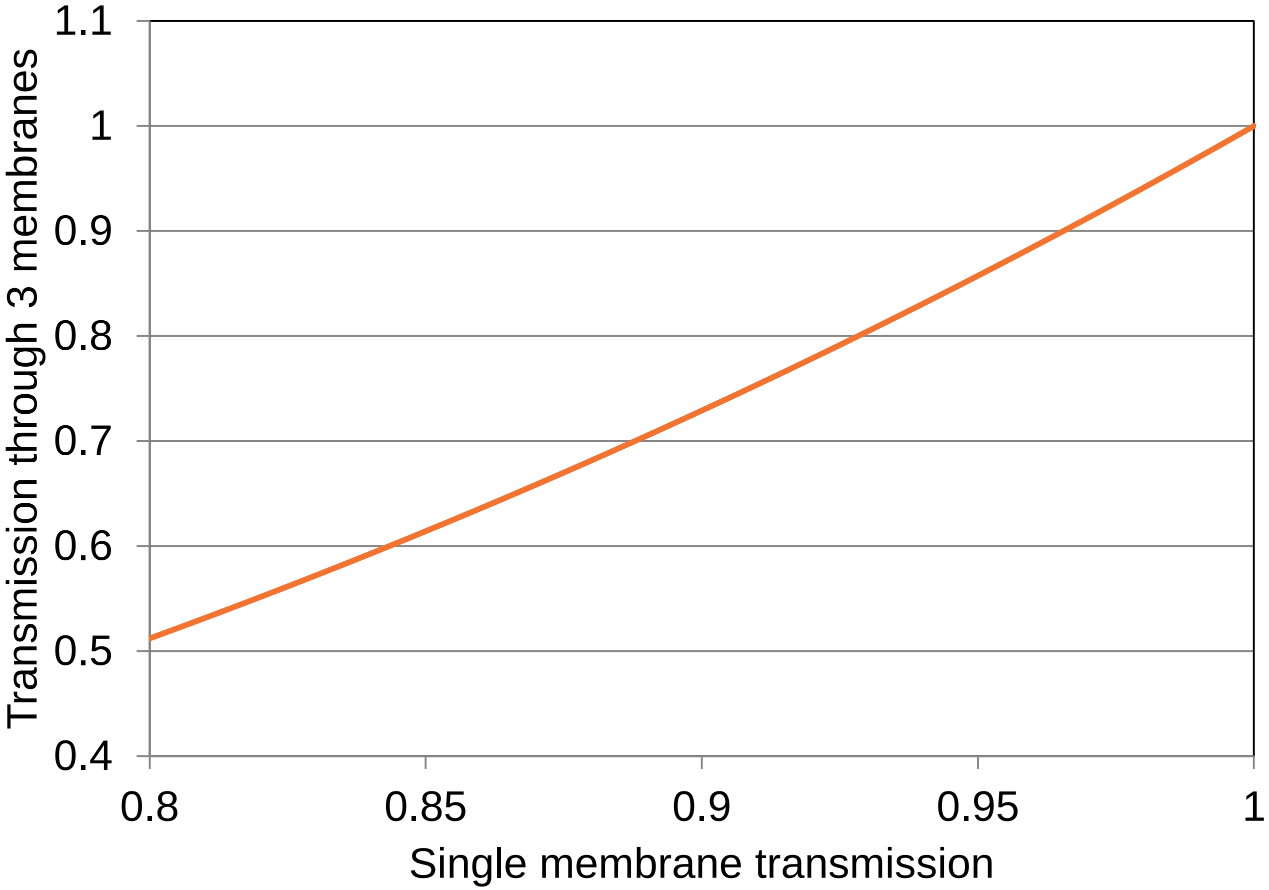
Cycle time and masks

- Suppose that we replace 10 layers triple-patterned with optical lithography with 10 single exposure EUV lithography steps.
    - 20 fewer lithography operations
        - Reduction of thin film depositions, etches, cleans, …
- At 1.5 days between masking steps, total process time is reduced by nearly one month by using EUV lithography!

- But what happens if we lose the cycle-time advantage of fewer operations by holding wafers while masks are qualified?

What constitutes an HVM-worthy pellicle

- Transmission mean > 90%
- Transmission non-uniformity < 1% range
- Durability
  - During normal handling
    - Shipping g-forces
  - g-forces while scanning
  - During pumping and venting cycles
  - Thermal stresses
- Lifetime
  - Cost ≤ $1/wafer
    - Example: > 10k wafers @ $10k/pellicle



The challenge of mask contamination

- No pellicle
  - Regular reticle qualifications
  - Disruption of manufacturing flow
  - Cost of inspection and clean tools
  - Risk of repeating defects

- Pellicle
  - Transmission loss
  - Cost of pellicles

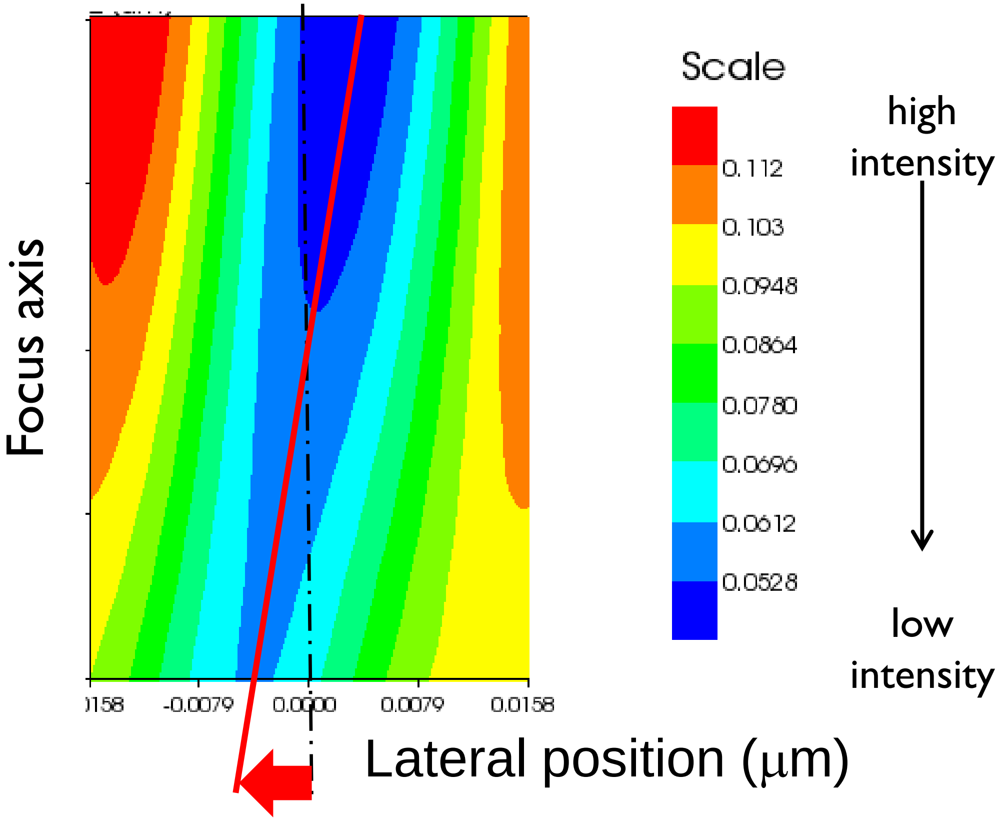
Process control

In R&D, there are hurdles

In manufacturing, the bar is much higher

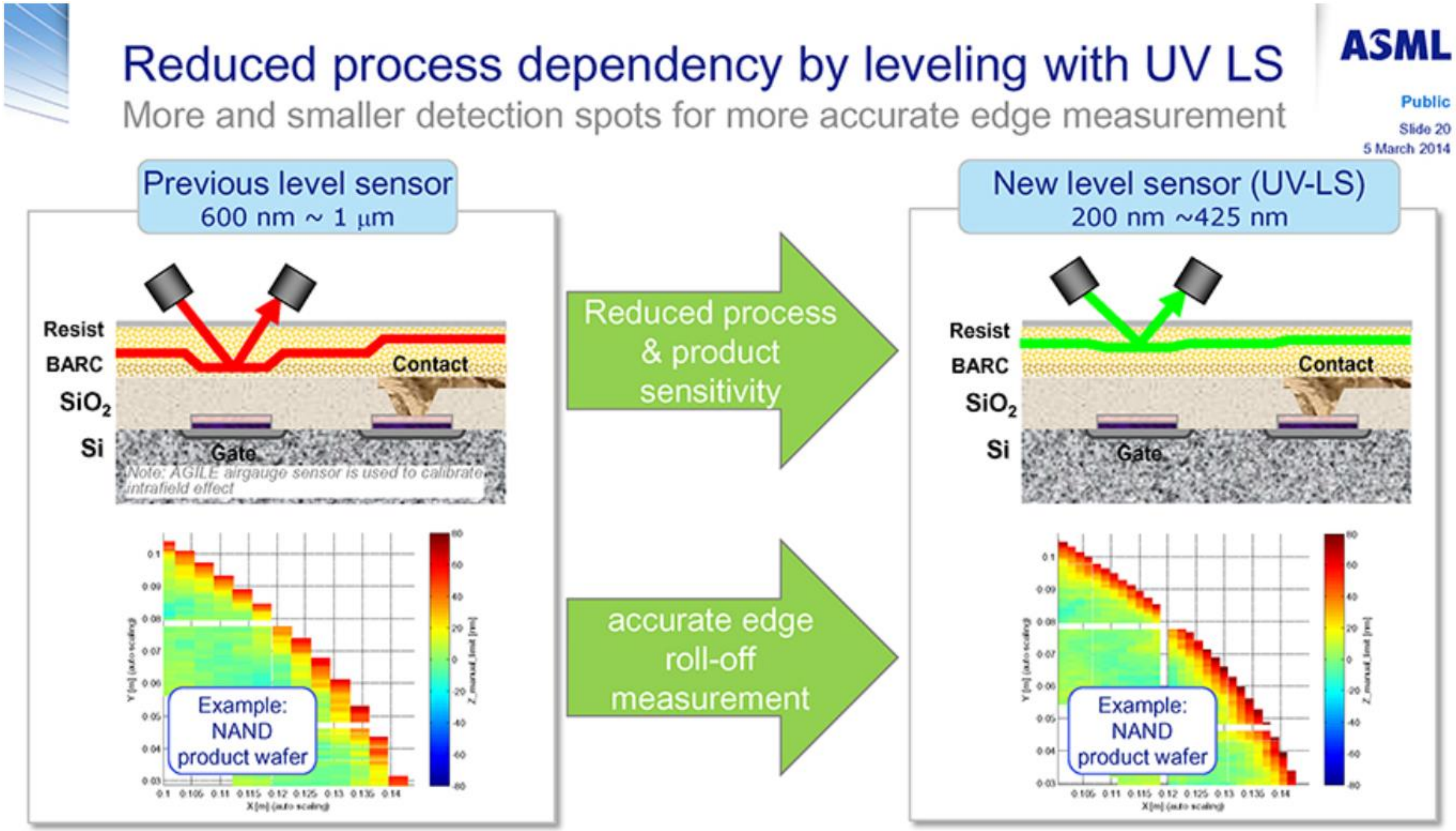
Process control for EUVL: focus control

- Simulations of conventional focus-exposure windows show large depths-of-focus for EUV lithography
- Unfortunately, little about EUV lithography is conventional



S. Raghunathan, et al., “Characterization of Telecentricity Errors in High-Numerical-Aperture Extreme Ultraviolet Mask Images,” 3-beams (2014)

Process control for EUVL



Reduced process dependency by leveling with UV LS

More and smaller detection spots for more accurate edge measurement

ASML

Public

Slide 20

5 March 2014

Previous level sensor
600 nm ~ 1 µm

Note: AGILE airgauge sensor is used to calibrate intrafield effect

Example:
NAND
product wafer

Reduced process & product sensitivity

accurate edge roll-off measurement

New level sensor (UV-LS)
200 nm ~425 nm

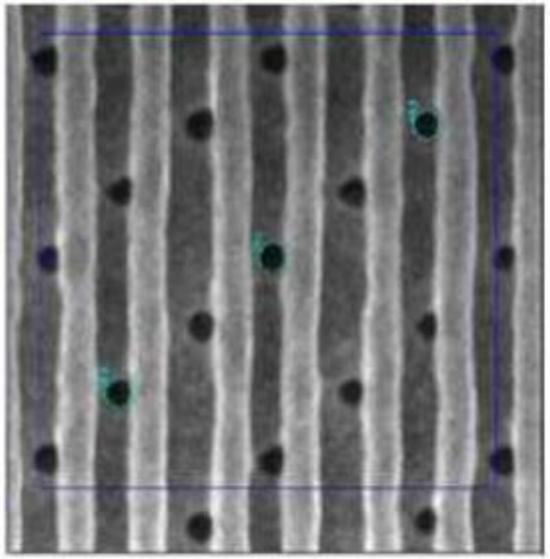
Example:
NAND
product wafer

Process Control: Overlay

Angstrom

↓

3.67 nm overlay



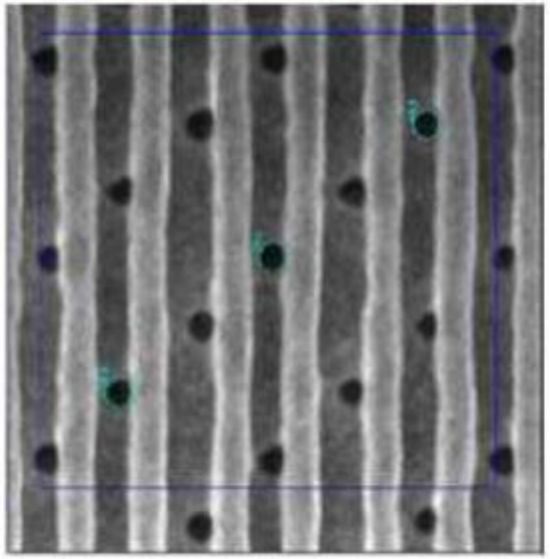
Carbon-carbon bond	1.2-1.5 Å
Silicon-silicon bond	1.1 Å

Process Control: Overlay

0.1’s Angstroms

↓

3.67 nm overlay



Carbon atom radius	0.70 Å
Bohr radius	0.53 Å

LWR: Resist Requirements Table from 2013 ITRS

Values were based on CDU requirements for microprocessors with planar transistors

Device performance

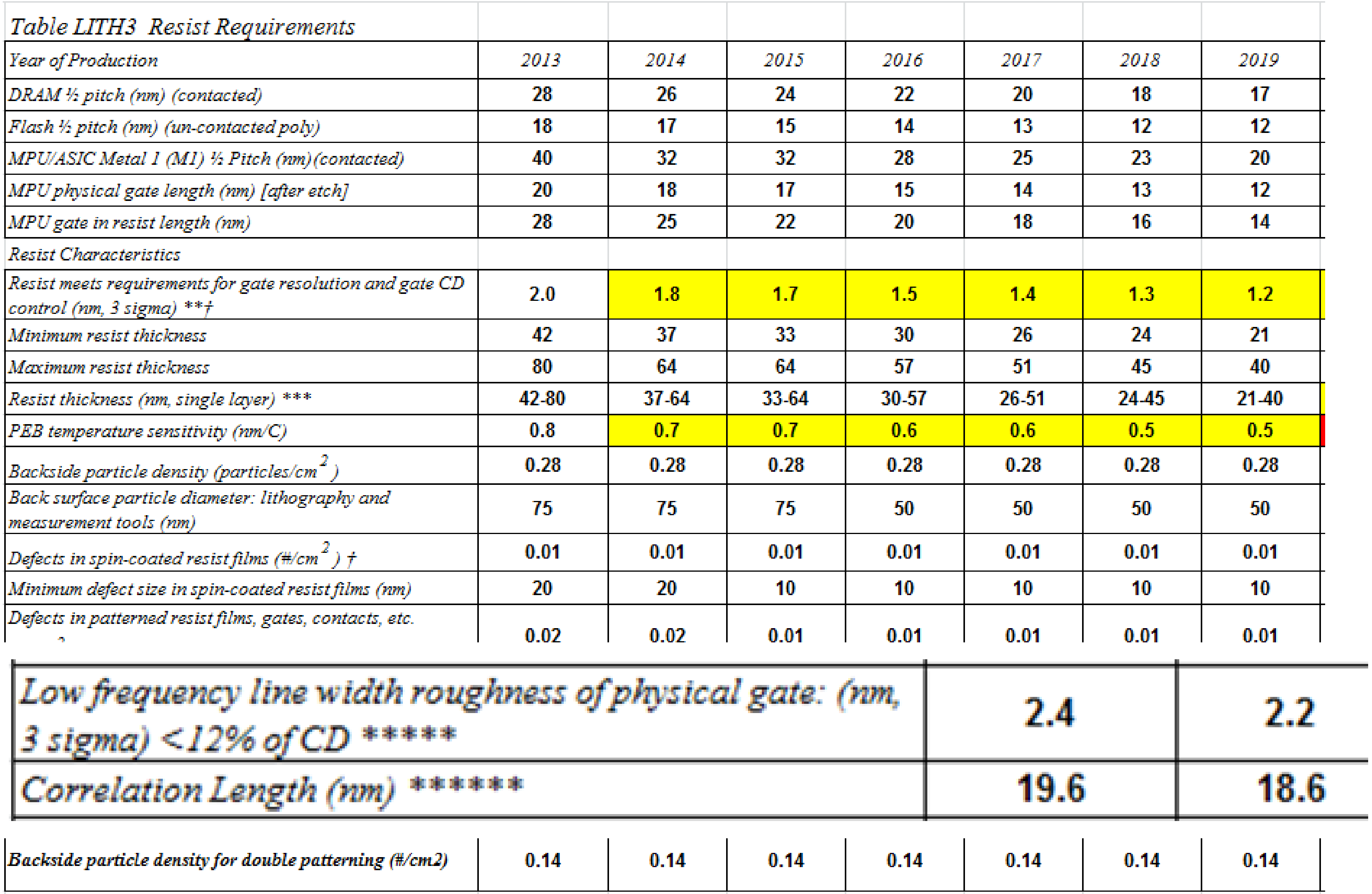


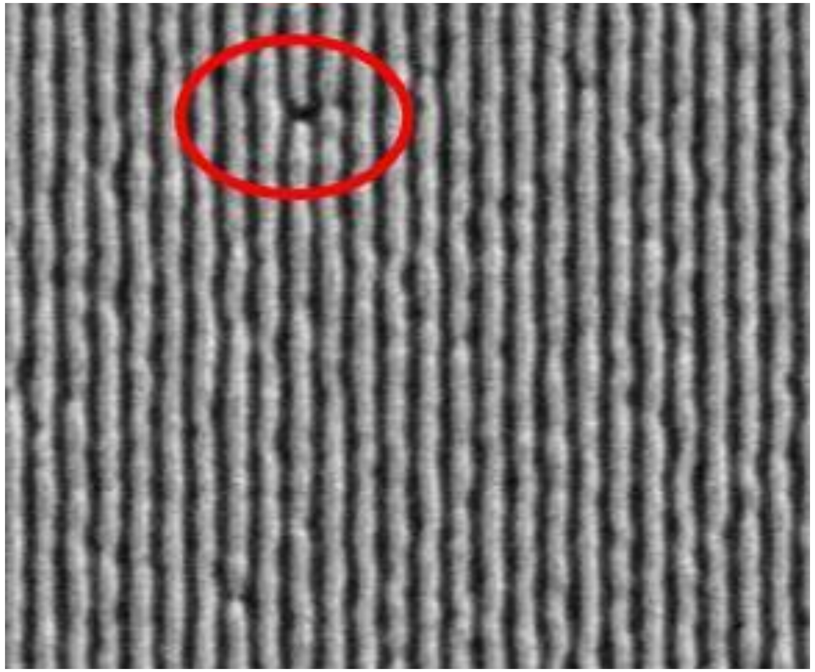
Table LITH3 Resist Requirements							
Year of Production	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*
DRAM ½ pitch (nm) (contacted)	28	26	24	22	20	18	17
Flash ½ pitch (nm) (un-contacted poly)	18	17	15	14	13	12	12
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	40	32	32	28	25	23	20
MPU physical gate length (nm) [after etch]	20	18	17	15	14	13	12
MPU gate in resist length (nm)	28	25	22	20	18	16	14
Resist Characteristics							
*Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) **†*	2.0	1.8	1.7	1.5	1.4	1.3	1.2
Minimum resist thickness	42	37	33	30	26	24	21
Maximum resist thickness	80	64	64	57	51	45	40
*Resist thickness (nm, single layer) ****	42-80	37-64	33-64	30-57	26-51	24-45	21-40
PEB temperature sensitivity (nm/C)	0.8	0.7	0.7	0.6	0.6	0.5	0.5
Backside particle density (particles/cm^2)	0.28	0.28	0.28	0.28	0.28	0.28	0.28
Back surface particle diameter: lithography and measurement tools (nm)	75	75	75	50	50	50	50
Defects in spin-coated resist films (#/cm^2) †	0.01	0.01	0.01	0.01	0.01	0.01	0.01
Minimum defect size in spin-coated resist films (nm)	20	20	10	10	10	10	10
Defects in patterned resist films, gates, contacts, etc.	0.02	0.02	0.01	0.01	0.01	0.01	0.01

*Low frequency line width roughness of physical gate: (nm, 3 sigma) <12% of CD ******	2.4	2.2
*Correlation Length (nm) *******	19.6	18.6

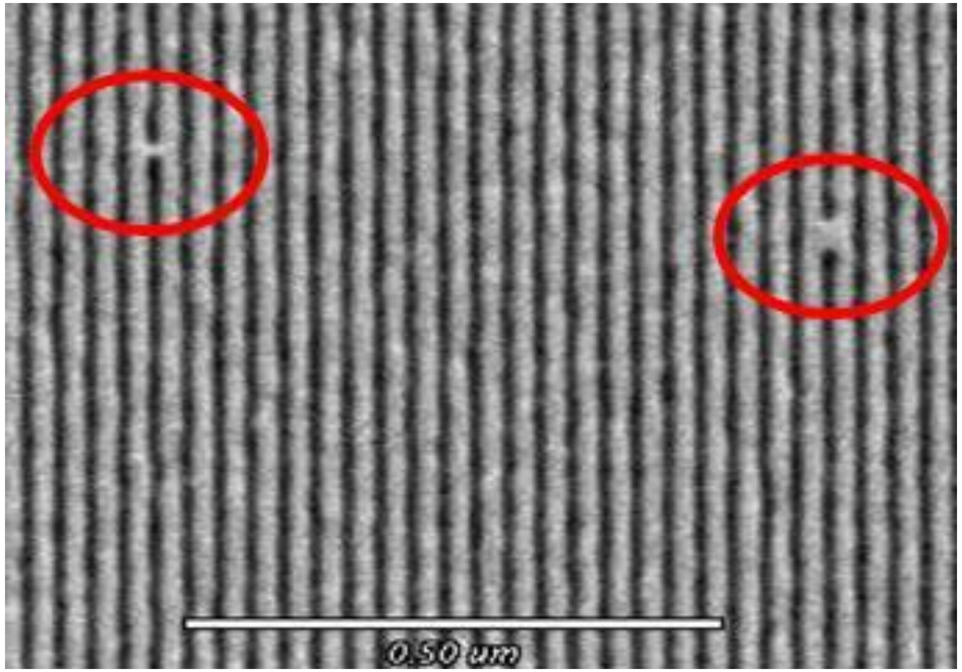
Backside particle density for double patterning (#/cm2)	0.14	0.14	0.14	0.14	0.14	0.14	0.14

LER concerns → yield concerns

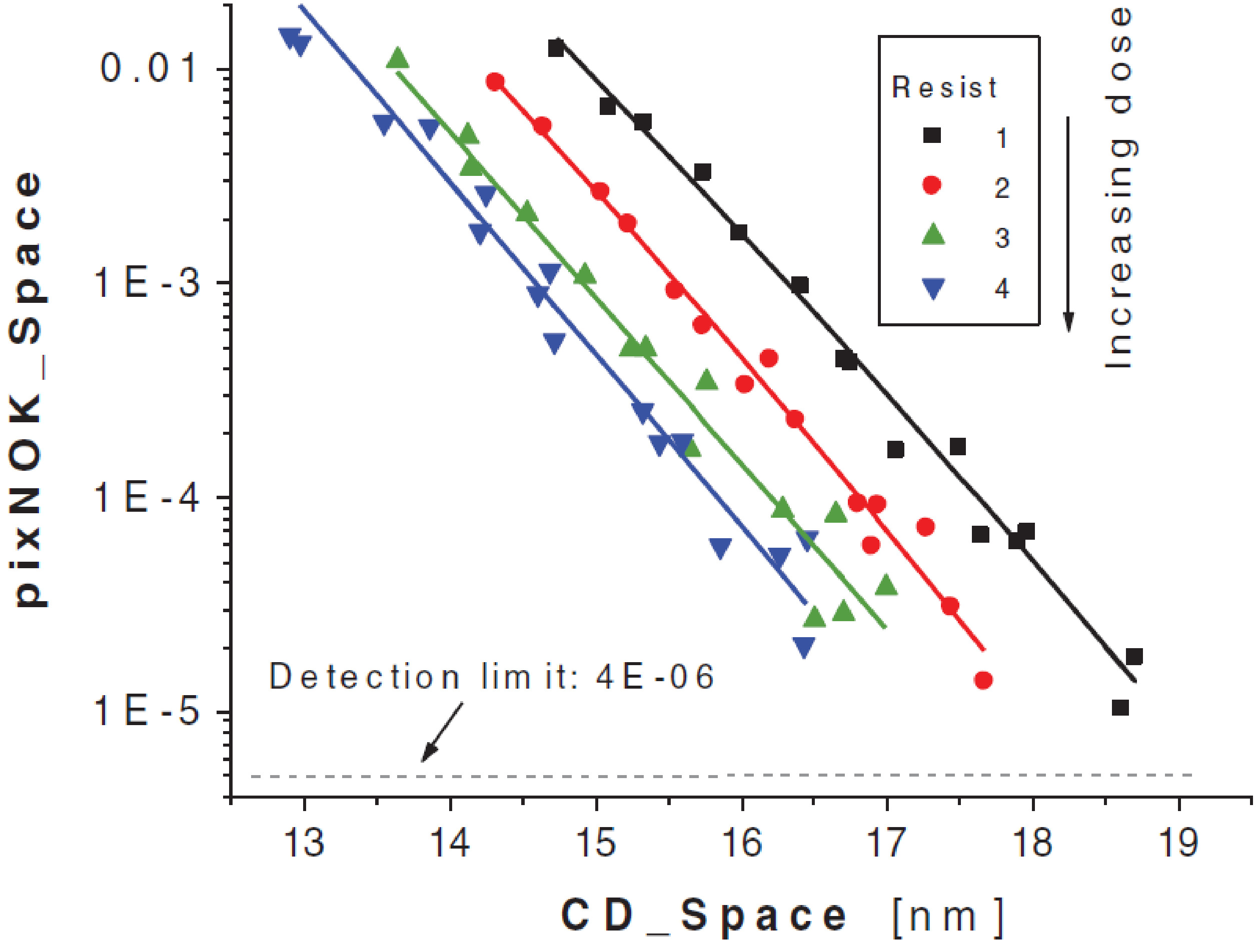
Line Break



Micro-bridging



LER concerns → yield concerns



From Peter De Bisschop, “Stochastic effects in EUV lithography: random, local CD variability, and printing failures,” JM3 (2017)

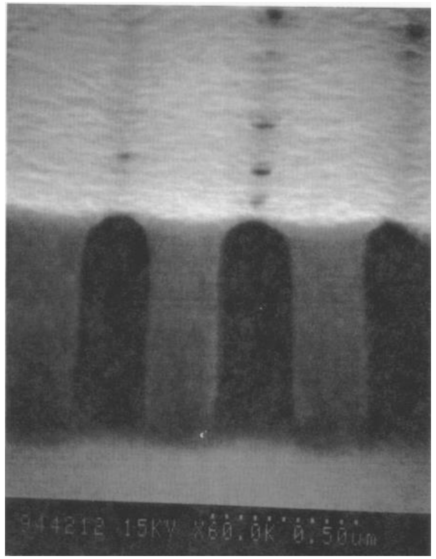
Inserting EUVL into manufacturing will drive improvements

- Many improvements are best made in a manufacturing environment
  - Yield
  - Process control
- Greater urgency for repairing equipment

First generation → second generation lithographic technologies

- Consider the i-line to KrF transition
  - Introduction of chemically amplified resists
    - Needed to learn how to handle resist poisoning
  - Arc lamps → excimer lasers
  - New materials for pellicles

Disruptive



- The transition to the second generation of KrF lithography was more evolutionary
  - A bit easier

First generation → second generation EUV lithography

λ and NA will not change soon

large k_1

$$20\text{ nm half-pitch} = 0.49\frac{13.5}{0.33}\text{ nm}$$

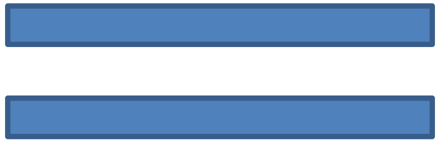
Next node = 0.7x linear shrink:

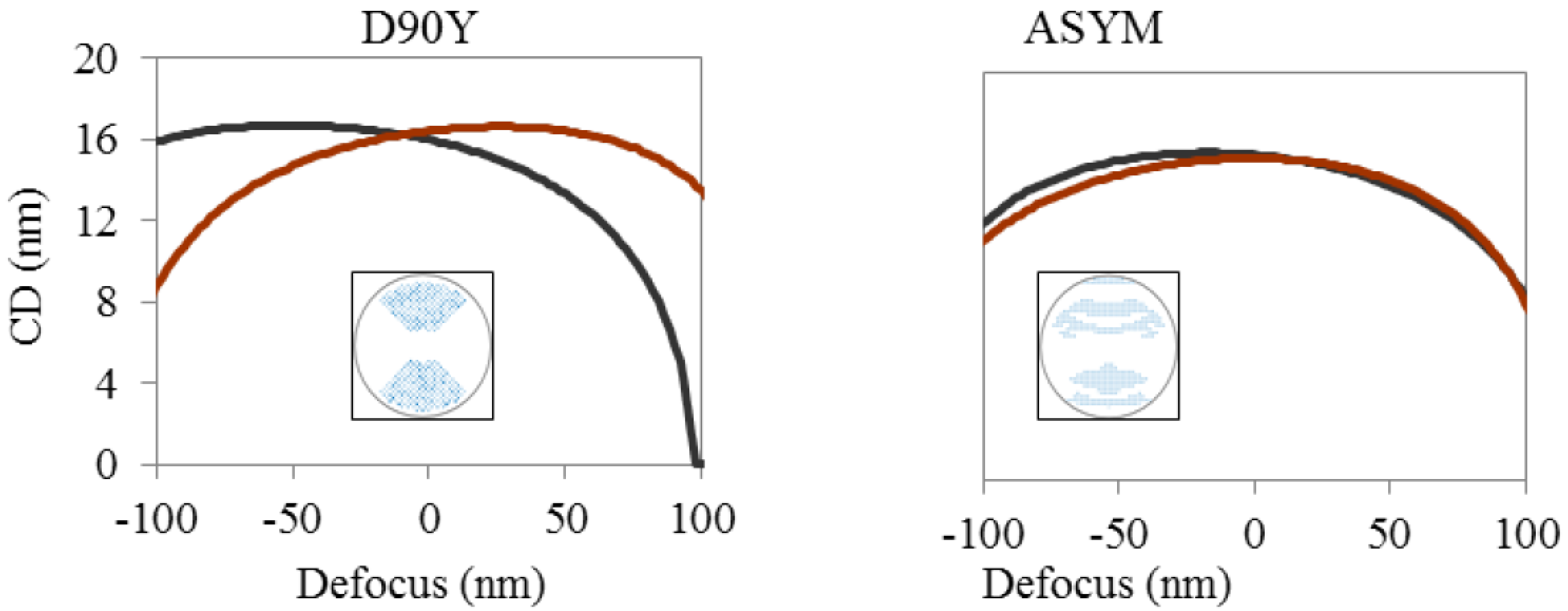
$$14\text{ nm half-pitch} = 0.34\frac{13.5}{0.33}\text{ nm}$$

The technical challenges of second generation EUV lithography are formidable

Mask 3D effects

CD versus focus for 2-bar structures, 32 nm pitch:





T. Last, et al. “Illumination pupil optimization in 0.33-NA extreme ultraviolet lithography by intensity balancing for semi-isolated dark field two-bar M1 building blocks,” JM3

Process control for EUVL

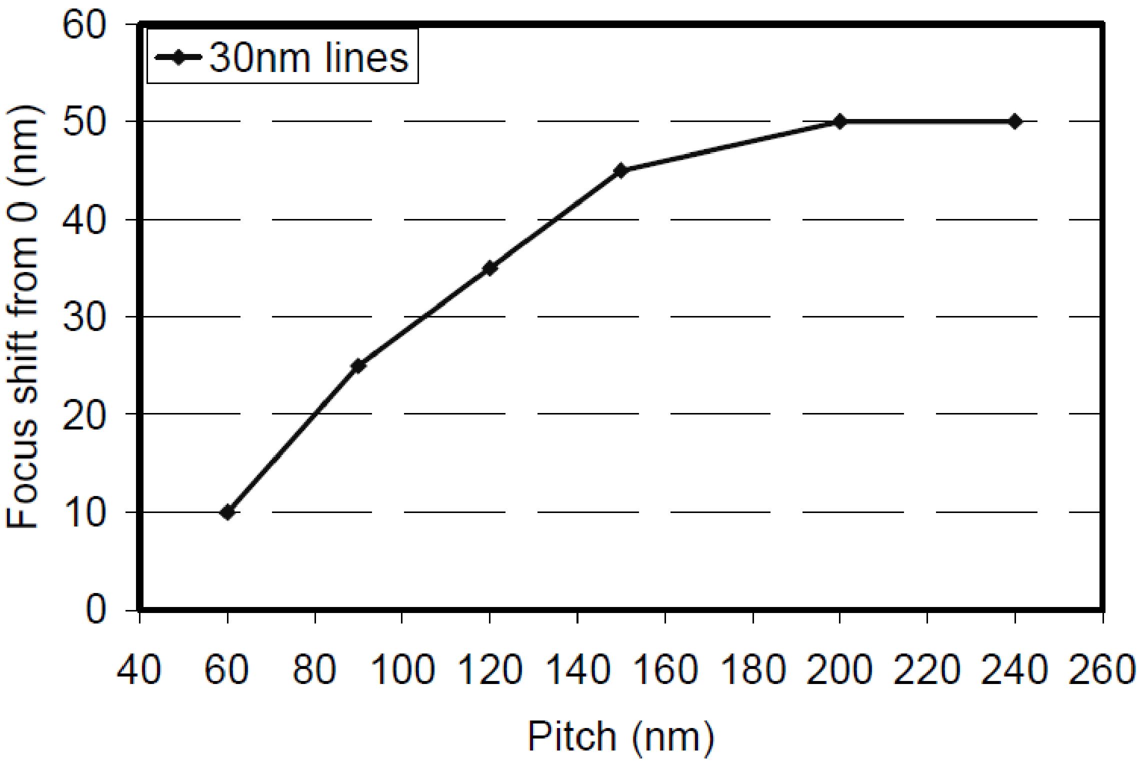
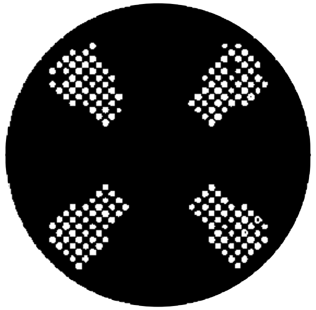
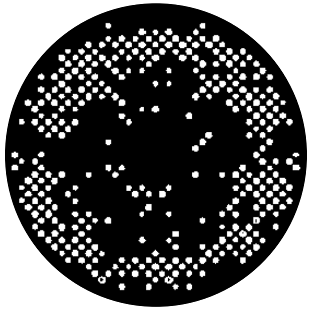


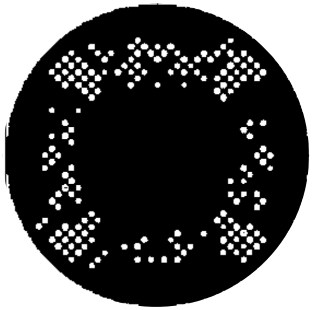
Fig. 2. Focus shift as a function of pitch for 30nm lines.
The light incident angle is 5-degree.

Pei-Yang Yan, “Understanding Bossung Curve Asymmetry and Focus Shift Effect in EUV Lithography,” BACUS Symposium on Photomask Technology, 2001

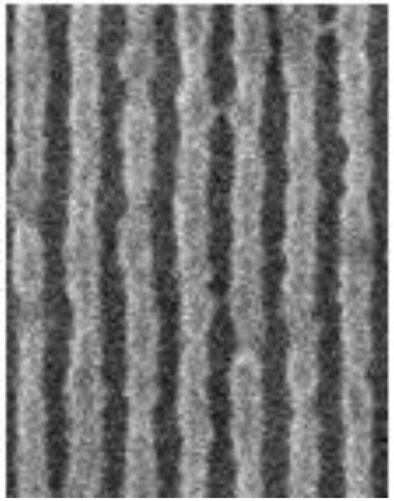
Source-mask optimization (SMO) for EUV


Quadrupole illumination

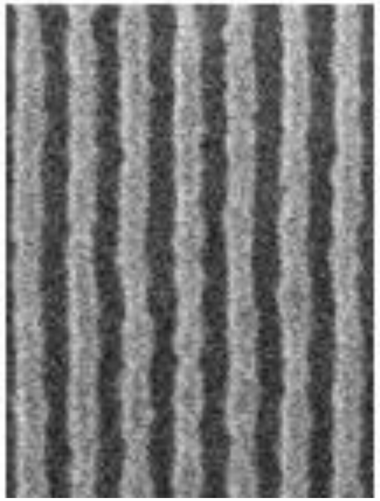

SMO standard solution


SMO NILS optimized

32 nm lines/spaces


NILS = 1.61
LER = 3.6nm


NILS = 1.57
LER = 3.7nm

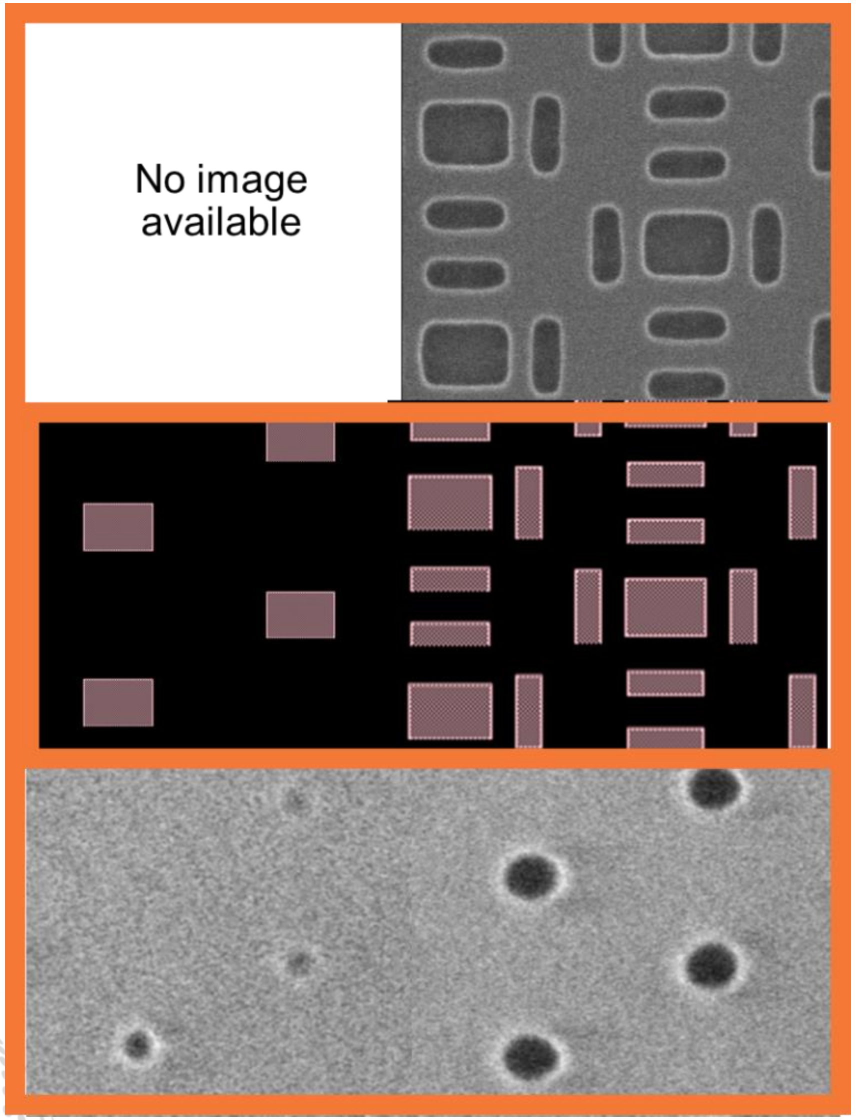

NILS = 2.05
LER = 2.6nm

"Application of EUV resolution enhancement techniques (RET) to optimize and extend single exposure bi-directional patterning for 7nm and beyond logic designs"

Ryoung-Han Kim et. al.,

SPIE Advanced Lithography Symposium (2016)

OPC/RET for EUV



Mask SEM image

Design layout

Developed resist on-wafer SEM image

Deniz Civay, et al.,
“Subresolution assist features in extreme ultraviolet lithography,”
JM3 (2015)

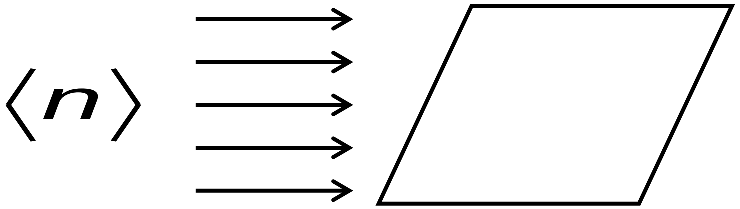
Second generation EUV lithography will require OPC on steroids

- OPC/RET needs to balance:
  - Conventional focus-exposure windows based on CD variation
  - Constraints on MEEF
  - Mask 3D effects
    - Loss of depth-of-focus (without compensation)
    - Image placement errors
      - Including that which induces image blur
  - Avoidance of small image log-slopes to control LER
- Will need SRAFs
- Aberrations are significant for EUV lithography

All needed before incorporating stochastics directly into our modeling

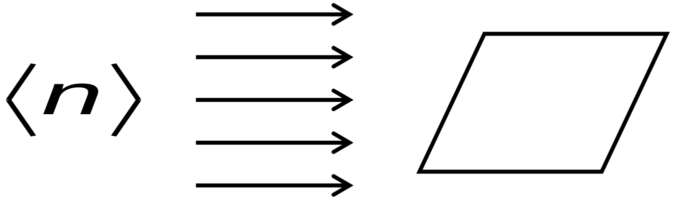
- Model-based implementation of SRAFs has proven difficult in optical lithography
  - Without the complications of pattern placement and shifts of best focus

Stochastics – will need more photons



$$\frac{\sigma}{\langle n \rangle} = \frac{1}{\sqrt{\langle n \rangle}}$$

Stochastics – will need more photons



$$\frac{\sigma}{\langle n \rangle} = \frac{1}{\sqrt{\langle n \rangle}}$$

To keep a constant level of variation per pixel, the beam dose will need to scale as $\frac{1}{\text{area}}$

$\Longrightarrow$ Effective dose will need to double every node

↑ Can be mitigated to some extent by increasing resist absorption

Node	Dose
7 nm	40 mJ/cm^2
5 nm	60 mJ/cm^2
3 nm	120 mJ/cm^2

Process control for EUV

Hypothetical overlay budget

Component	Error (nm)
Exposure tool	1.8
Reticle pattern placement	0.6
Reticle flatness	0.6
Wafer distortion	0.6
Wafer/mask heating	0.6
Mask 3D effects	0.6
Aberrations	0.6
Metrology	0.6
Total	2.4

Components need to be determined to Å level

1 Å = 4% of 2.4 nm

Process control for EUV

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It is a quantum world

Carbon-carbon bond	1.2-1.5 Å
Silicon-silicon bond	1.1 Å

Carbon atom radius	0.70 Å
Bohr radius	0.53 Å

It is a quantum world

Carbon-carbon bond	1.2-1.5 Å
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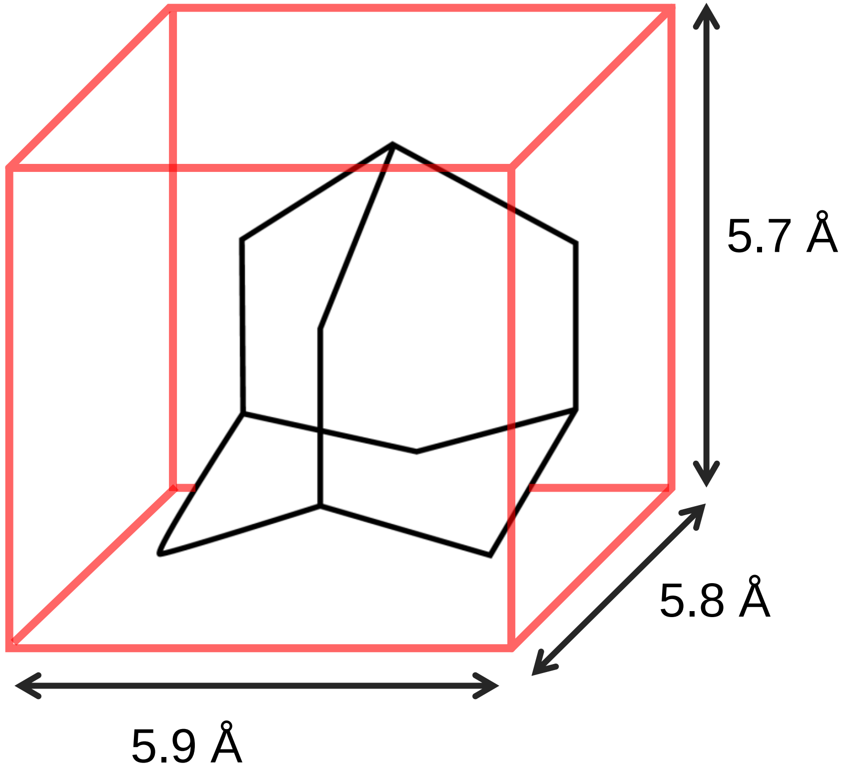
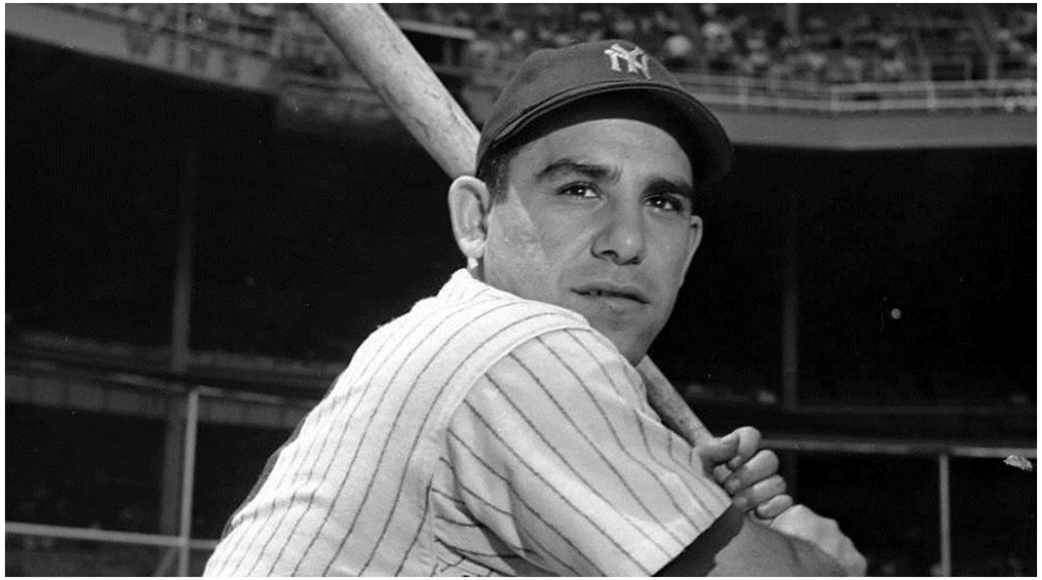
Adamantane molecule



Summary

- As we start-up EUV lithography in HVM, focus will be on practical issues
  - Equipment reliability
  - Particles on masks
  - Yield
    - Must take priority over scanner throughput
  - Other factors that affect die costs
  - Process control
- Second generation EUV lithography - no rest for the weary
  - OPC challenges
  - Will need more photons
  - Future scaling requires accounting for molecular size



"In theory there is no difference between theory and practice. In practice there is."

Yogi Berra,

Hall of Fame catcher for the
New York Yankees

Acknowledgements

- I would like to thank the following people.
  - Dr. Erik Hosler of GLOBALFOUNDRIES for the graph of EUV photocluster output
  - Dr. Michael Lercel of ASML for photography of NXE:3400
  - Dr. Moshe Preil of KLA-Tencor for picture of Teron 640e