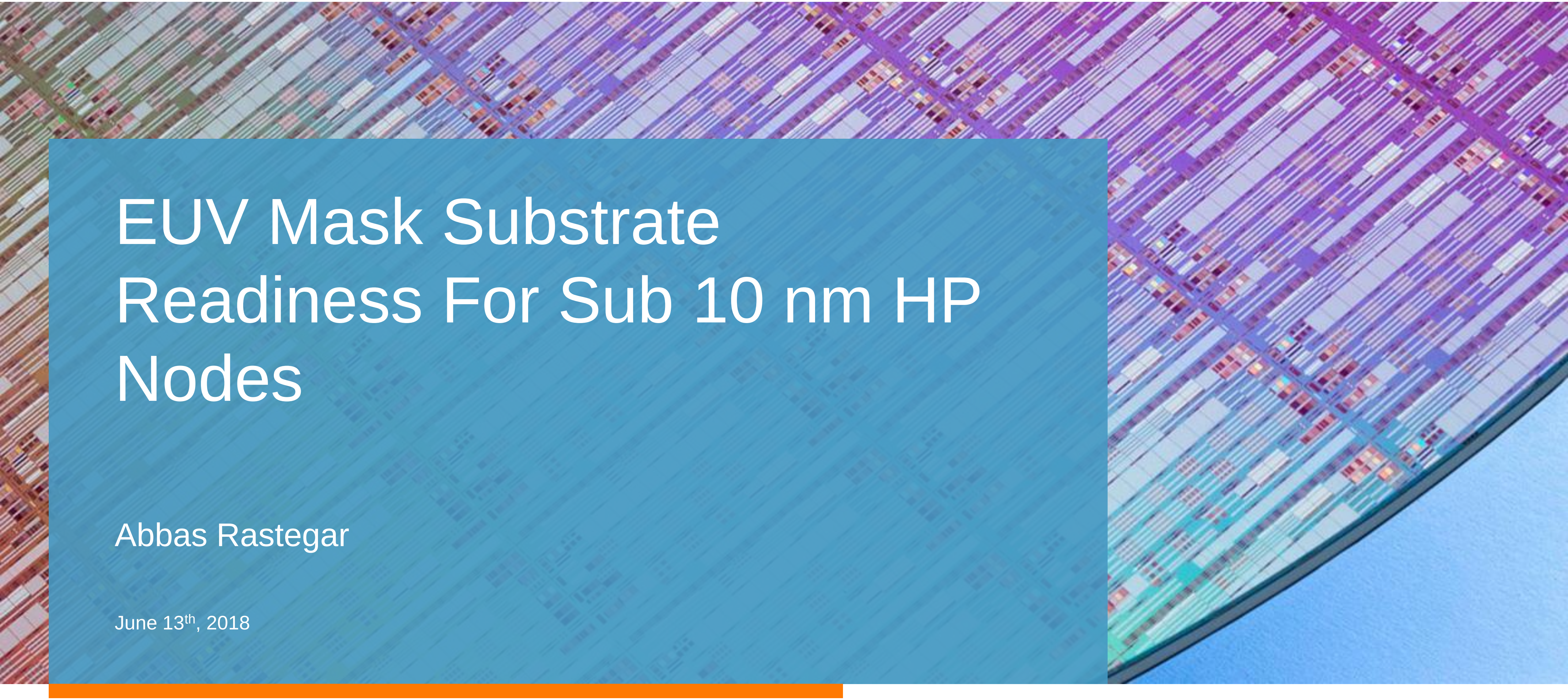


EUV Mask Substrate Readiness For Sub 10 nm HP Nodes

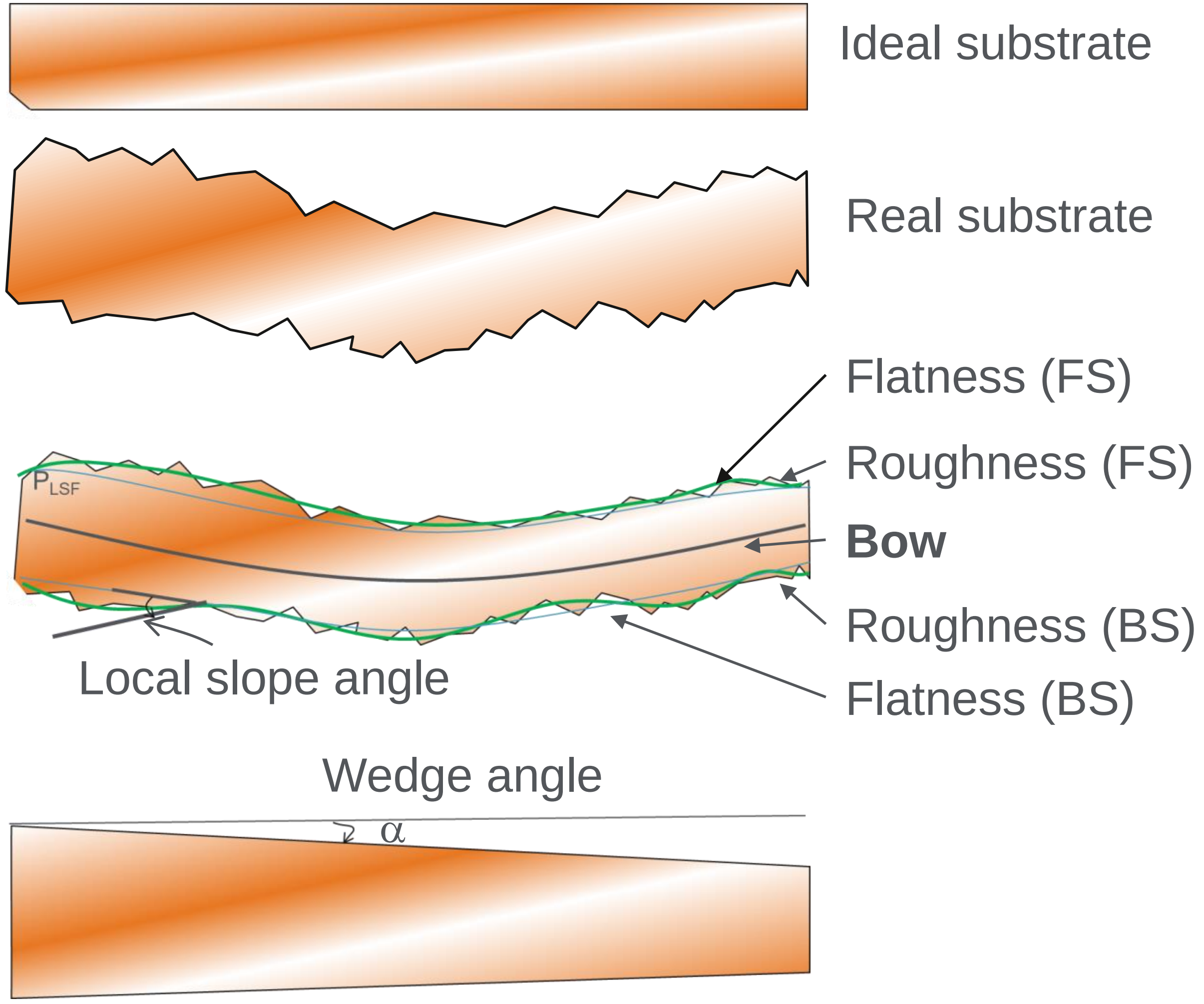
Abbas Rastegar

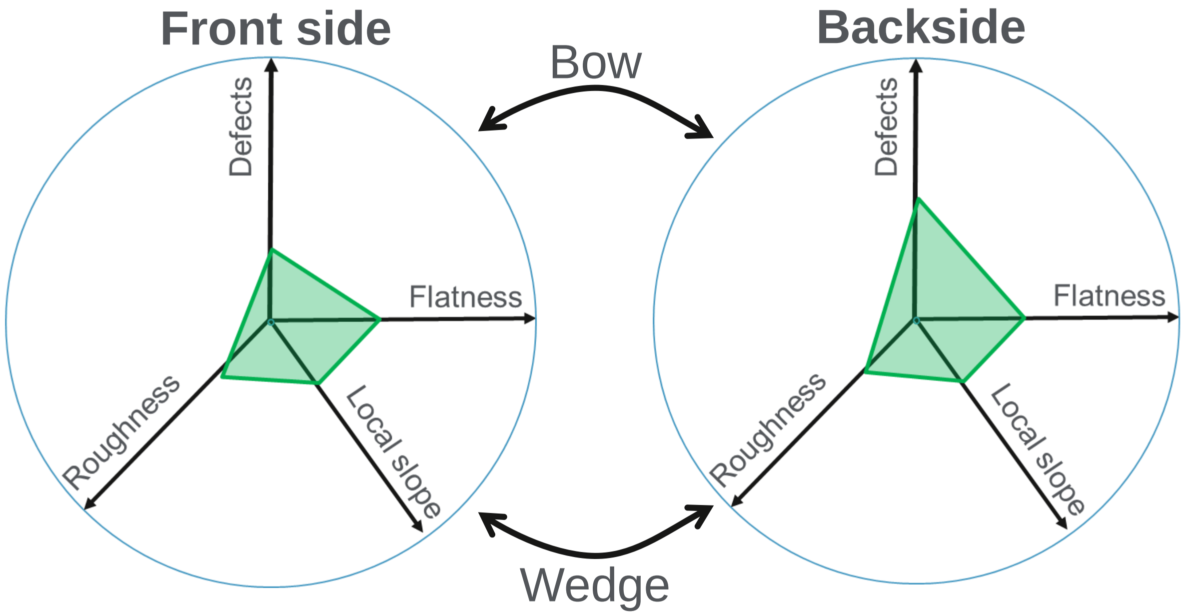
June 13th, 2018

Outline

- EUV mask substrate requirements
  - Flatness
  - Roughness
  - Defects
- EUV mask substrate manufacturing
- Progress in EUV mask substrate in Applied Materials
- EUV mask substrates for sub 10 nm nodes

Substrate Requirements: Critical Parameters

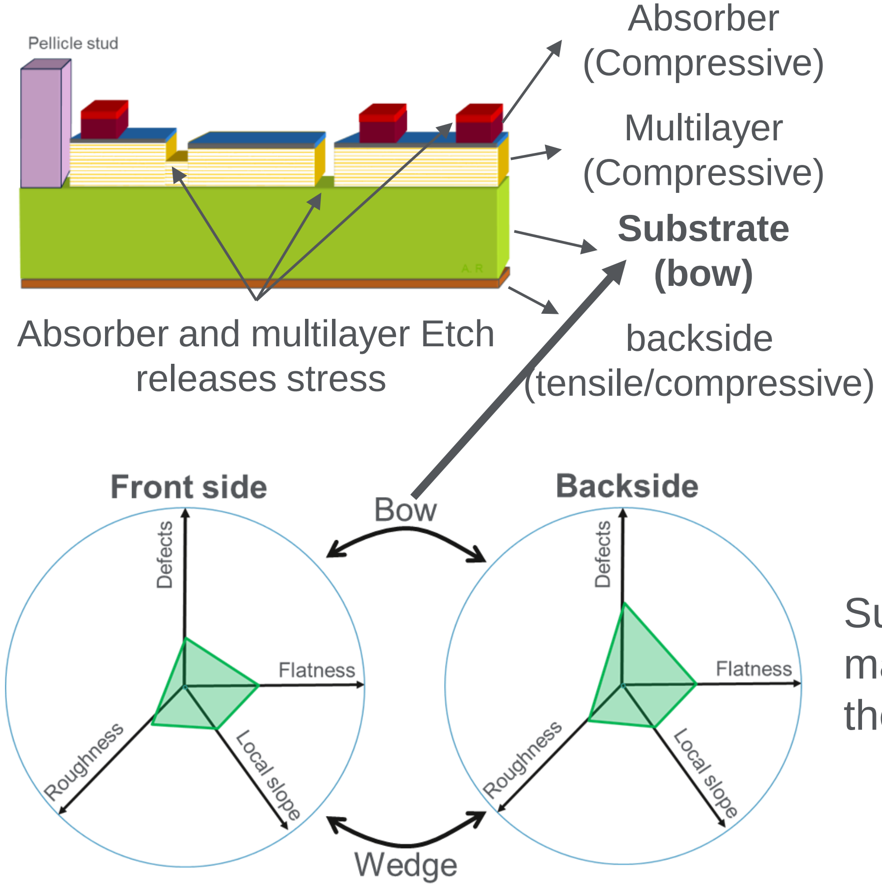




- Multiple parameters should be controlled both in the front an back surface
- All parameters are interdependent within each surface and between both surfaces

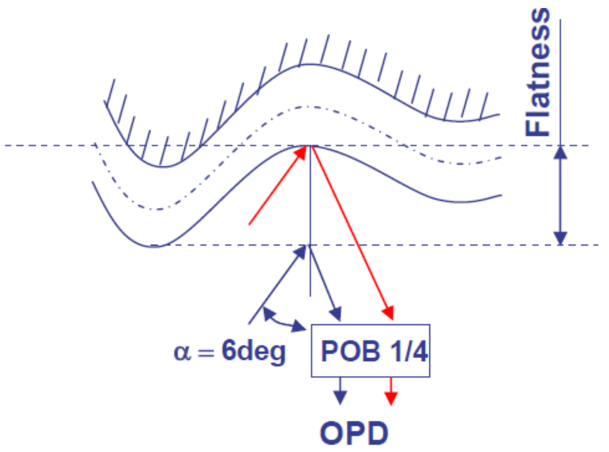
Substrate Flatness & Bow Contribution to Overlay Errors

Mask bow

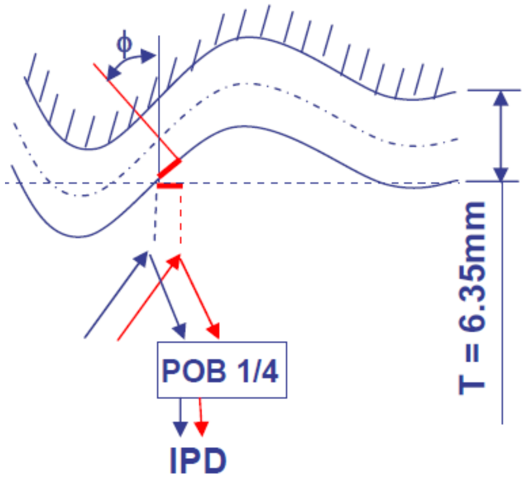


Substrate bow is the main contributor to the mask bow

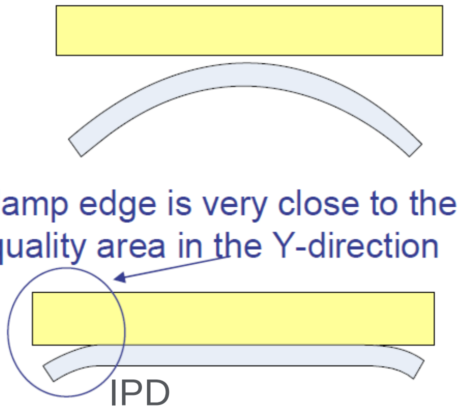
Out of Plane Distortion(OPD)



In Plane Distortion(IPD)



N.Harned et.al. ASML-EUVL 2007

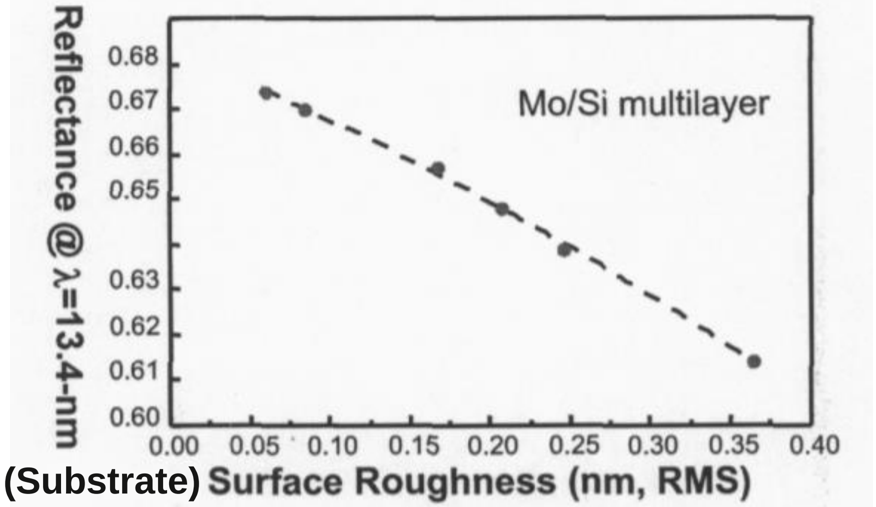


Clamp edge is very close to the quality area in the Y-direction

- Mask bow and flatness can lead to IPD and OPD errors some of which can NOT be corrected by scanner
- Substrate is the main contributor to mask flatness and bow

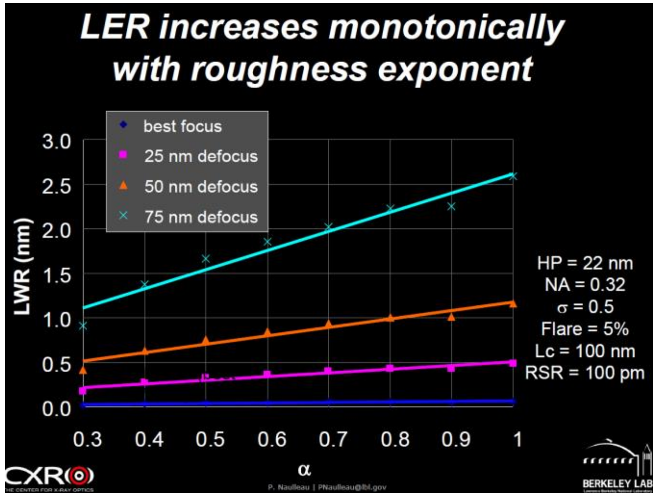
Substrate Roughness Contribution to EUV Mask

Impact on EUV reflectivity



Paul Mirkarimi *et.al.* Applied Optics,V39,p1617 (2000)

Impact on LER



Patrick Naulleau –*CXRO-*
α is roughness exponent (tangent to PSD curve)

Impact on defects

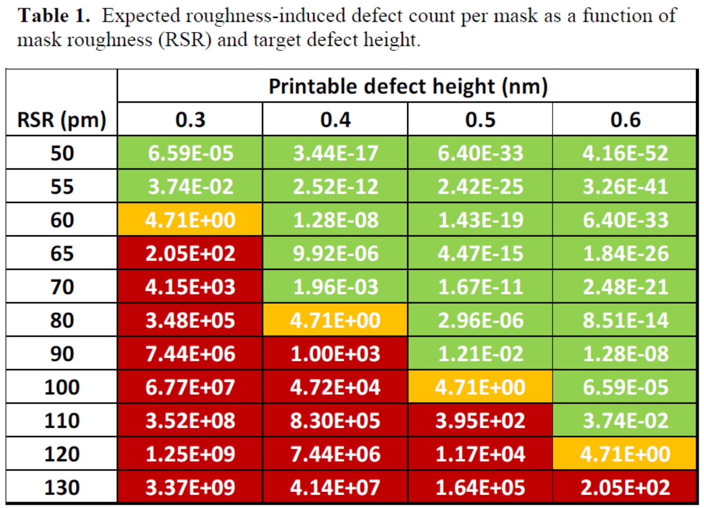
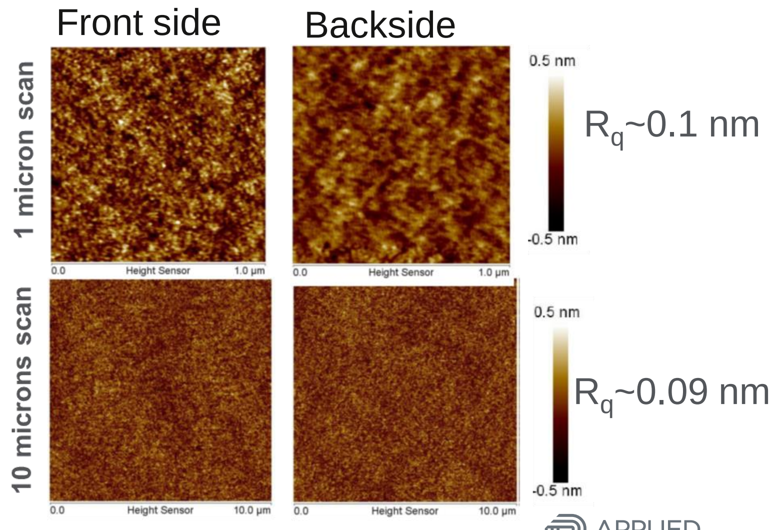


Table 1. Expected roughness-induced defect count per mask as a function of mask roughness (RSR) and target defect height.

RSR (pm)	Printable defect height (nm)			
	0.3	0.4	0.5	0.6
50	6.59E-05	3.44E-17	6.40E-33	4.16E-52
55	3.74E-02	2.52E-12	2.42E-25	3.26E-41
60	4.71E+00	1.28E-08	1.43E-19	6.40E-33
65	2.05E+02	9.92E-06	4.47E-15	1.84E-26
70	4.15E+03	1.96E-03	1.67E-11	2.48E-21
80	3.48E+05	4.71E+00	2.96E-06	8.51E-14
90	7.44E+06	1.00E+03	1.21E-02	1.28E-08
100	6.77E+07	4.72E+04	4.71E+00	6.59E-05
110	3.52E+08	8.30E+05	3.95E+02	3.74E-02
120	1.25E+09	7.44E+06	1.17E+04	4.71E+00
130	3.37E+09	4.14E+07	1.64E+05	2.05E+02

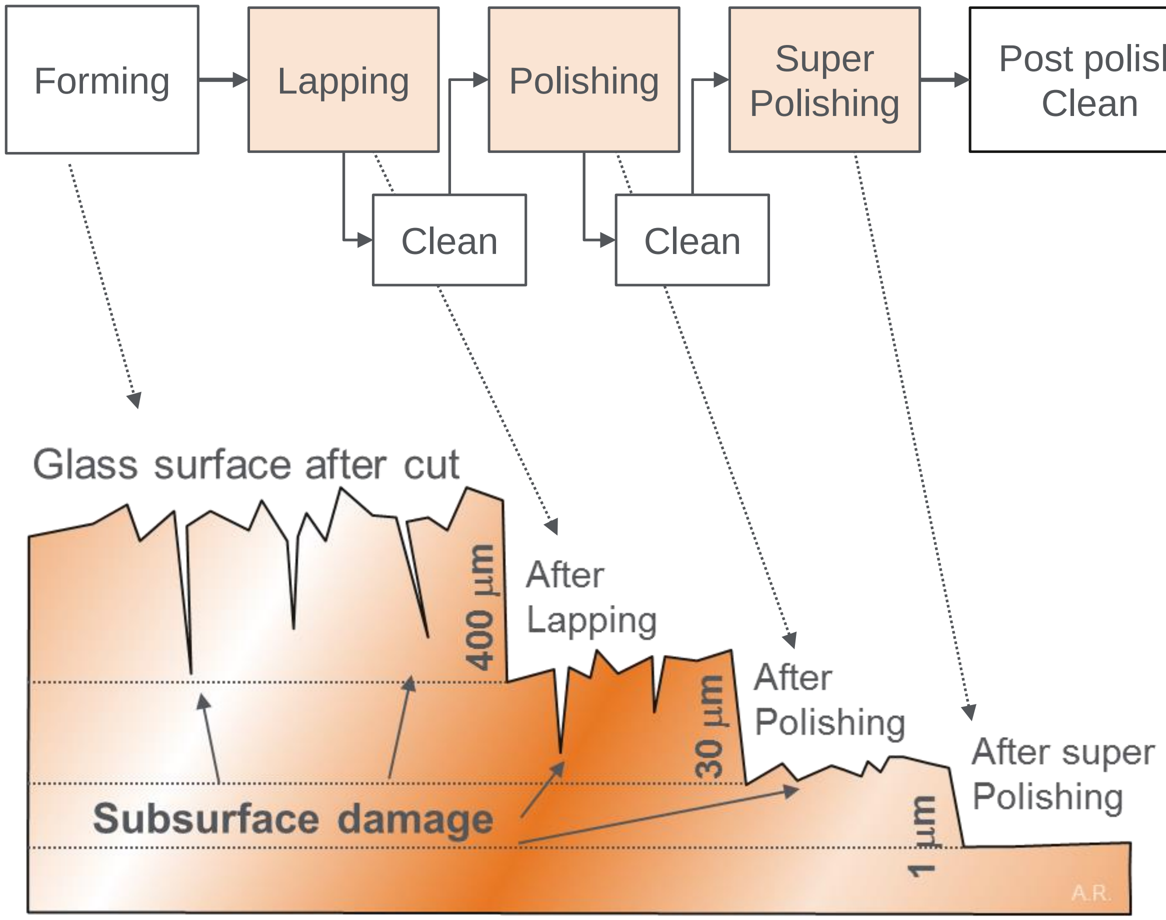
Patrick Naulleau *et.al.* Proc. of SPIE,9256(2014)

- EUV reflectivity is reducing by increasing substrate surface roughness
- Line edge roughness is increasing by increasing replicated substrate surface roughness
- Defect count is increasing by increasing substrate roughness due to dependency of inspection tools to the surface roughness



Typical ULE roughness

Manufacturing of EUV Mask Blank Substrates

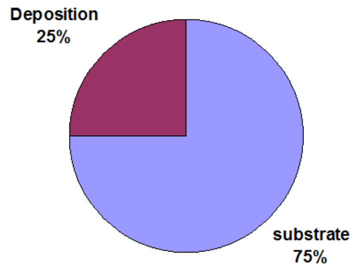


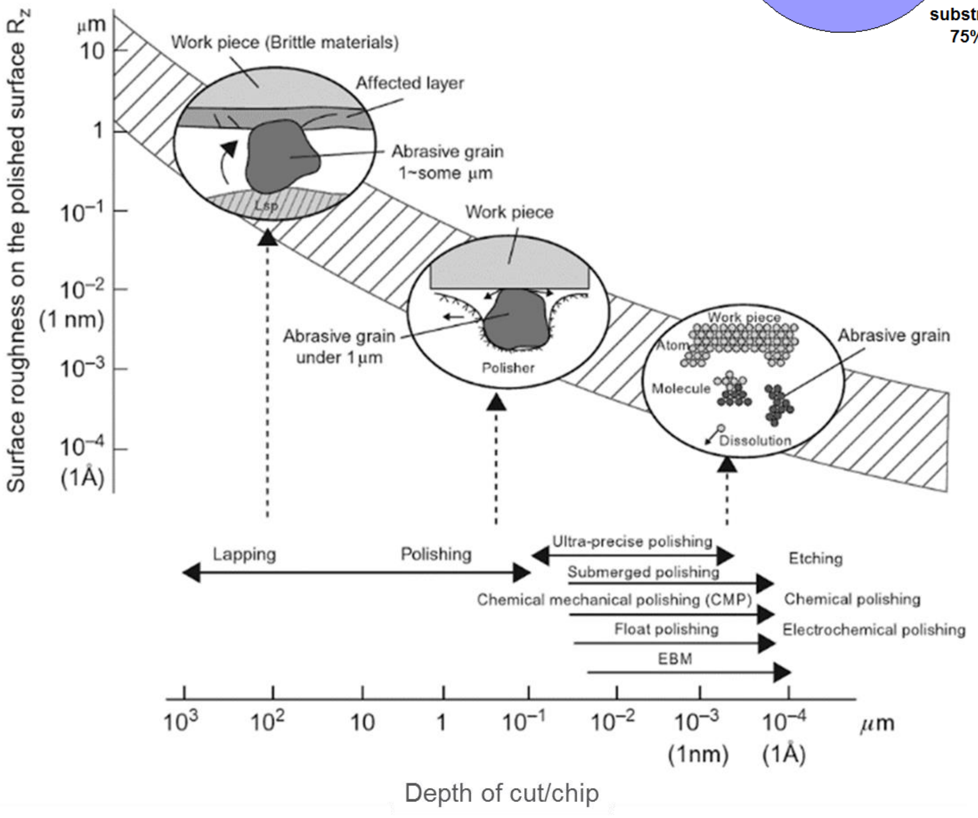
Forming → Lapping → Polishing → Super Polishing → Post polish Clean → Final Clean → Inspection → Multilayer Deposition

Lapping → Clean → Polishing

Polishing → Clean → Super Polishing

Typical blank defectivity



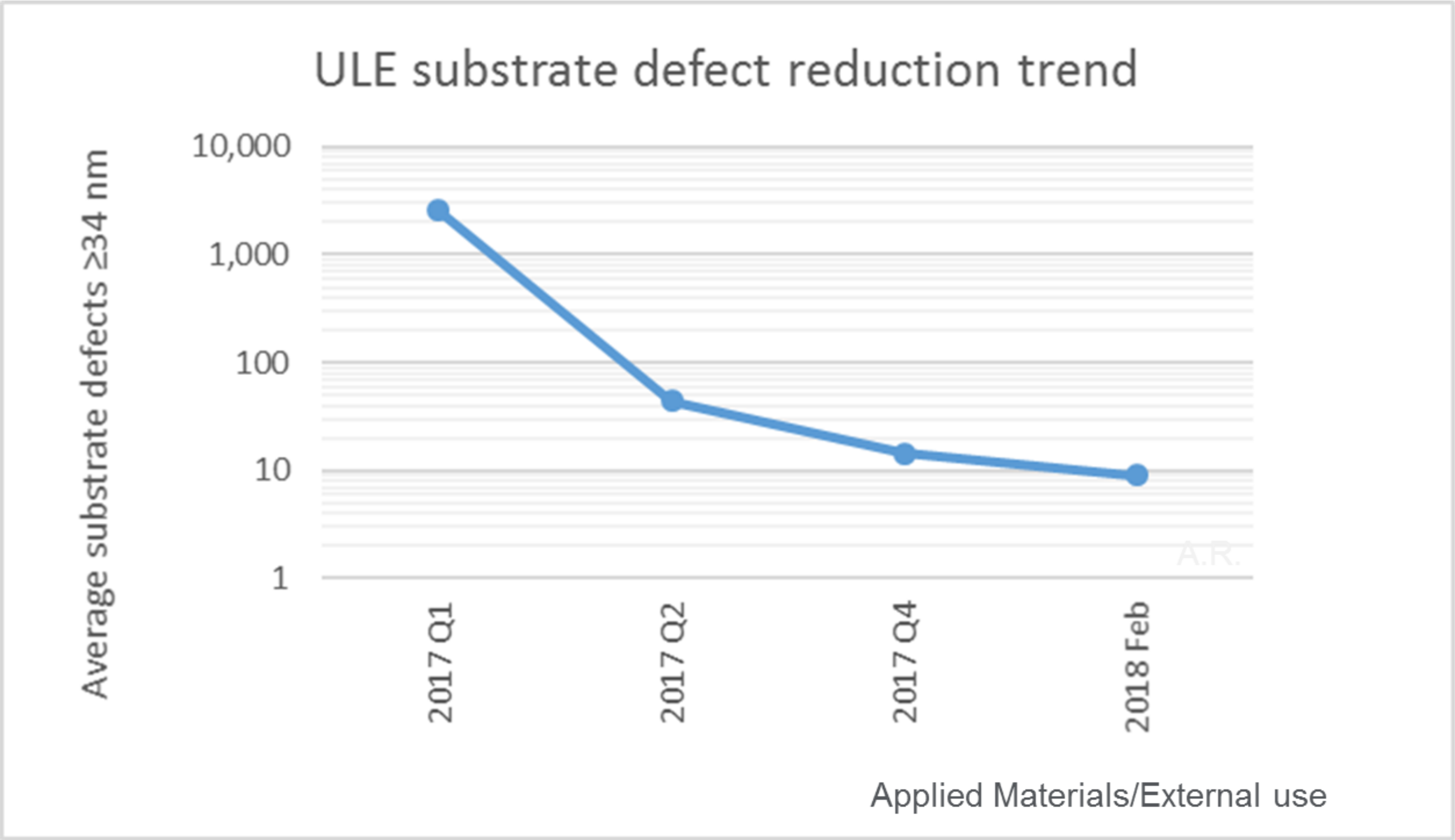


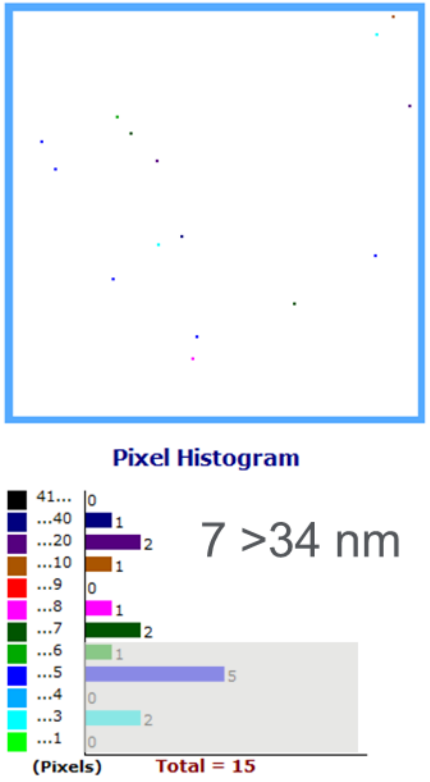
Advances in CMP/Polishing technologies, T.K Doi, et al

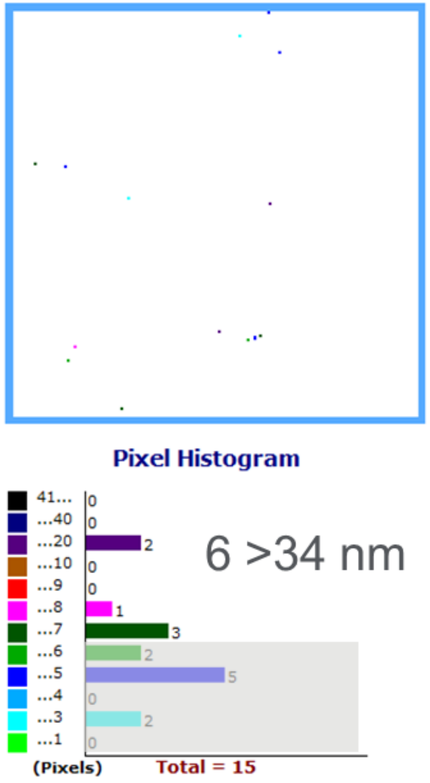
Each polishing step removes and creates subsurface damage

Remaining subsurface damage results in pit and scratches

Progress In ULE Substrate Defect Reduction In Applied Materials

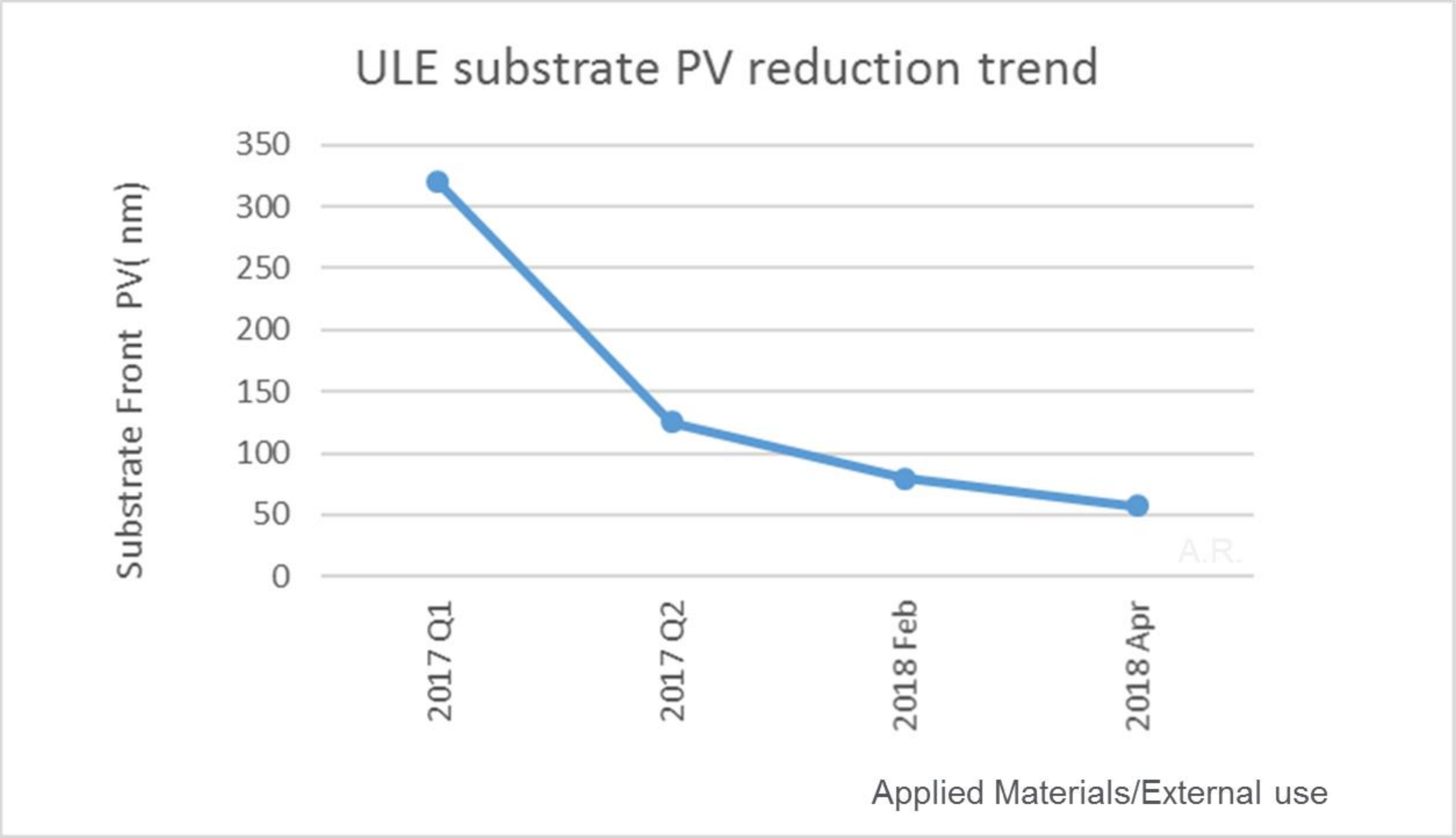






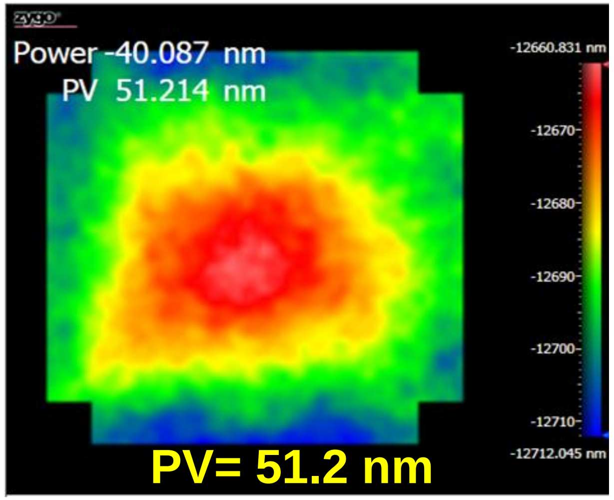
- Substrate defectivity has improved by 3 orders of magnitude within a year without sacrificing substrate flatness (i.e. PV)

Progress In ULE Substrate Flatness Reduction In Applied Materials

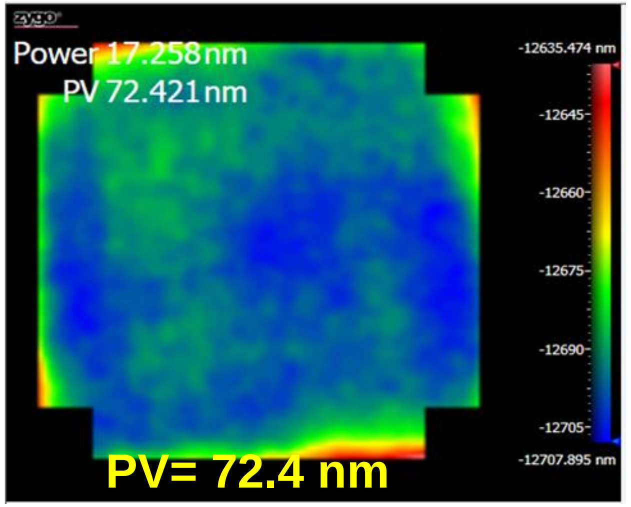


- Substrate flatness has improved by ~6x within a year without sacrificing defectivity

Front side Flatness

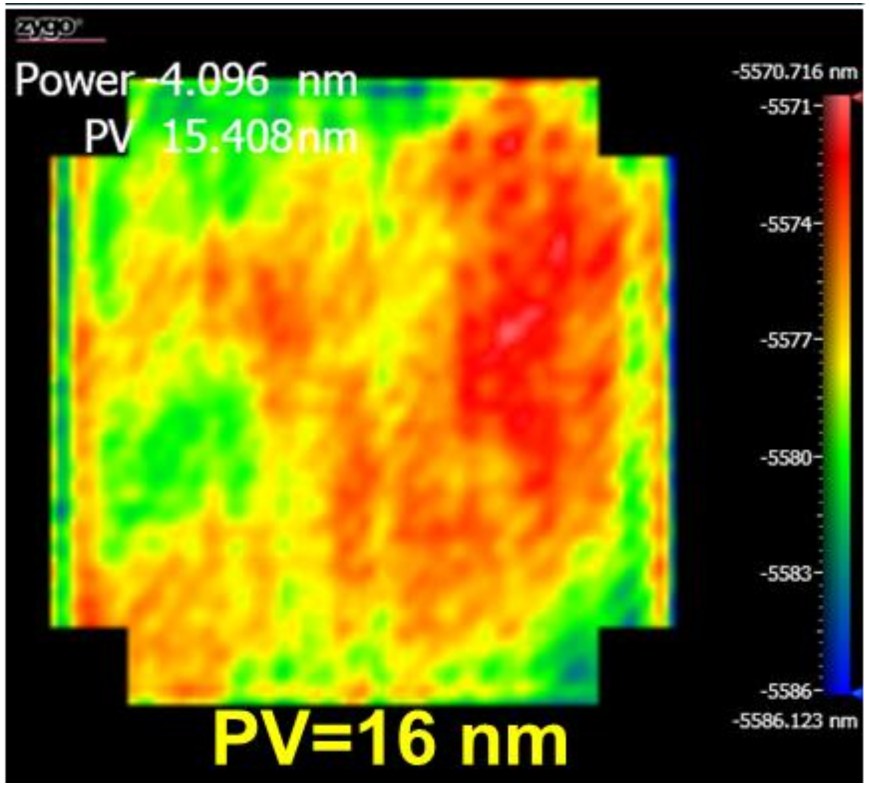


Backside Flatness

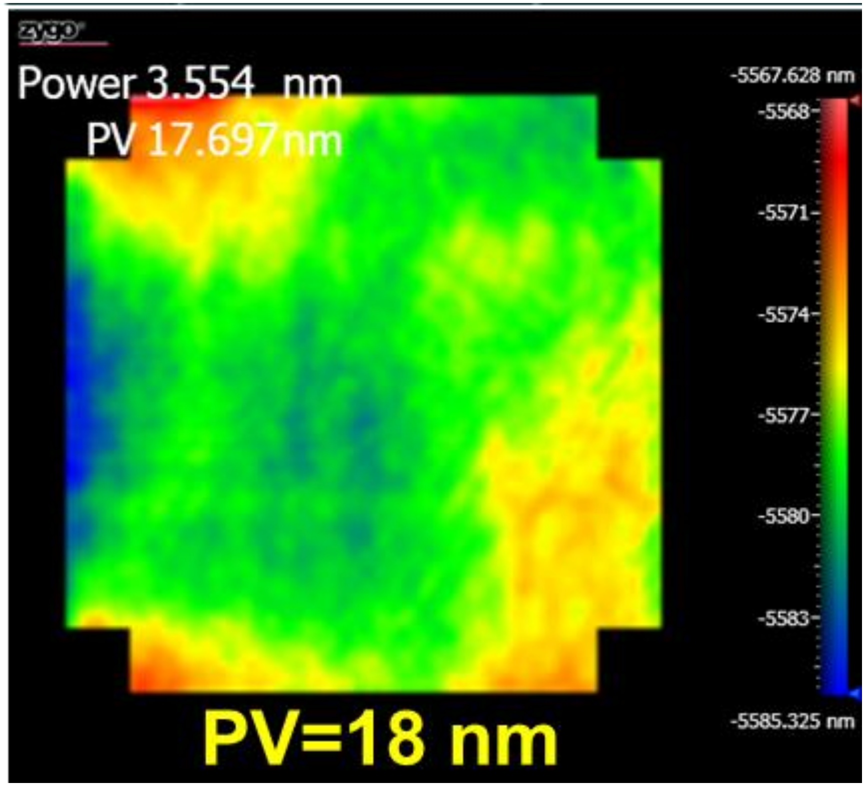


Progress In ULE Substrate Flatness Reduction (Advanced Polishing)

Front side

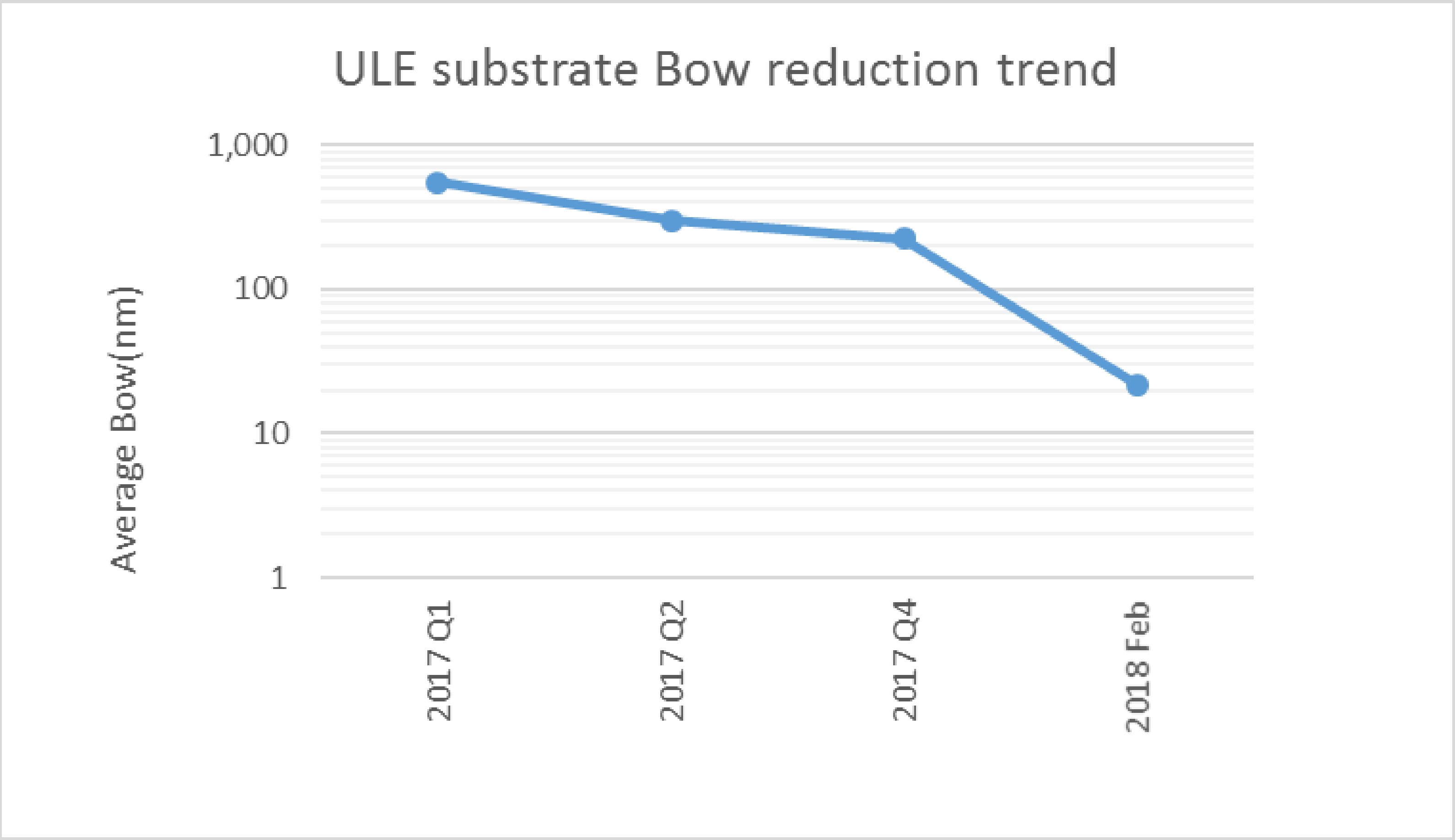


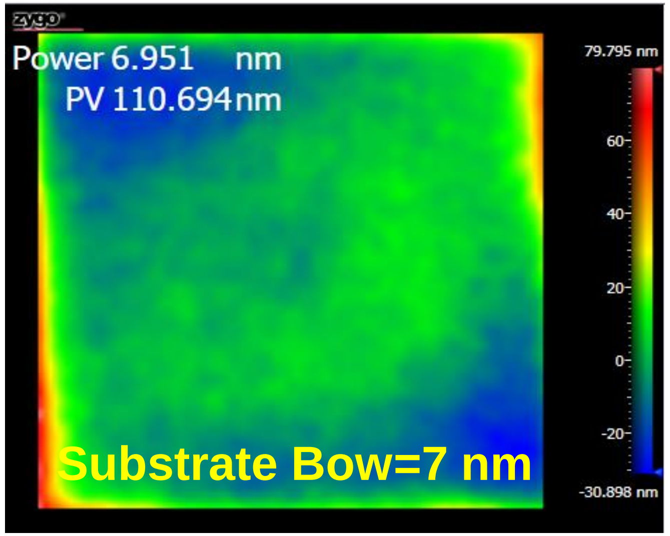
Backside

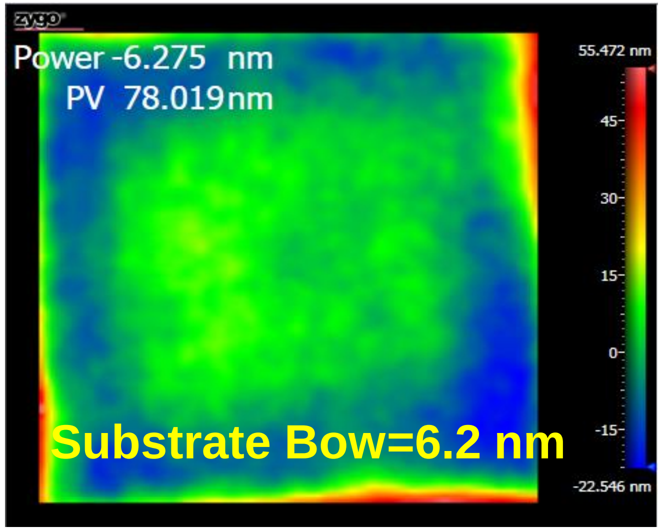


- Advanced polishing techniques were used to achieve PV=16 nm

Progress In ULE Substrate Bow Reduction In Applied Materials



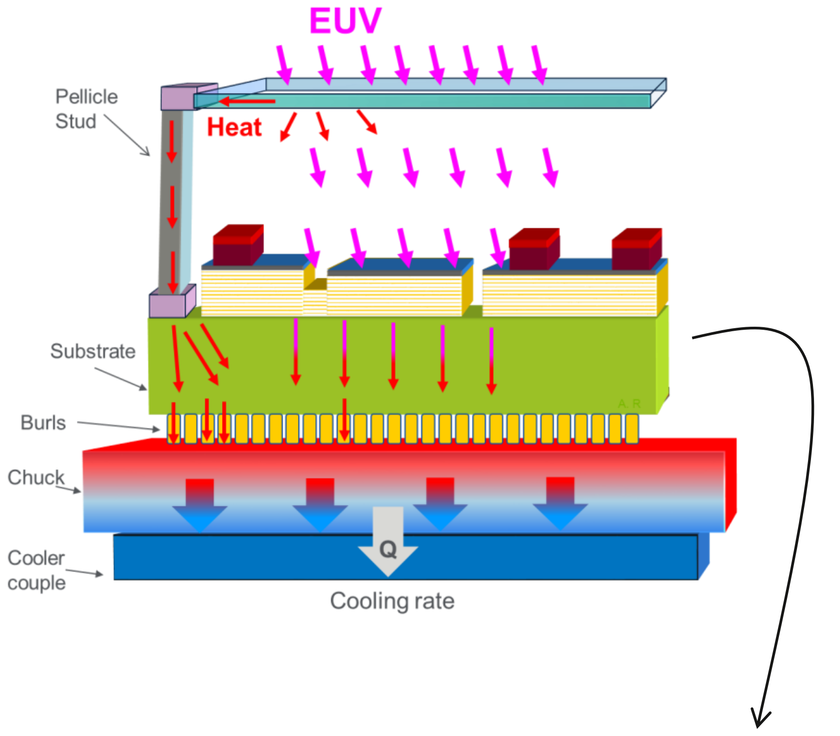


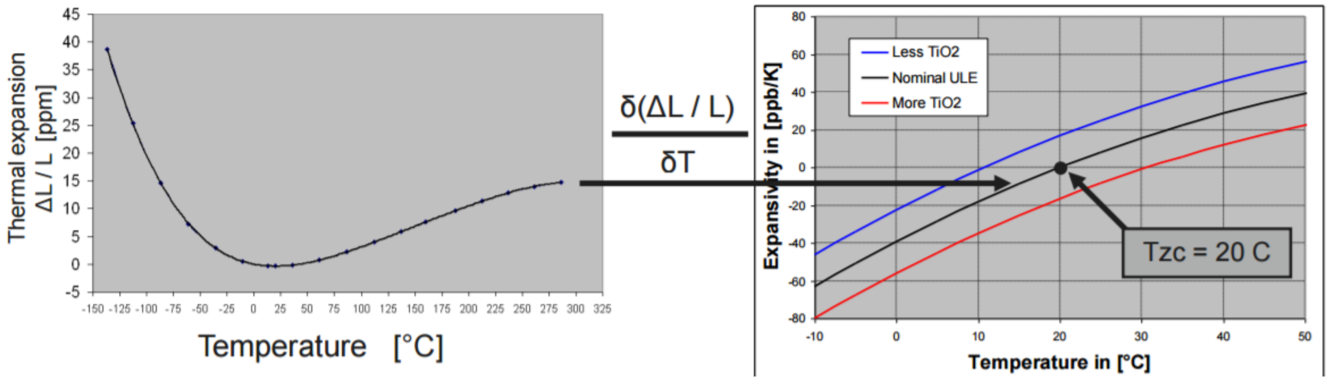


- Substrate bow was reduced by 25x within a year without sacrificing defectivity

EUV mask substrates for sub 10 nm HP nodes

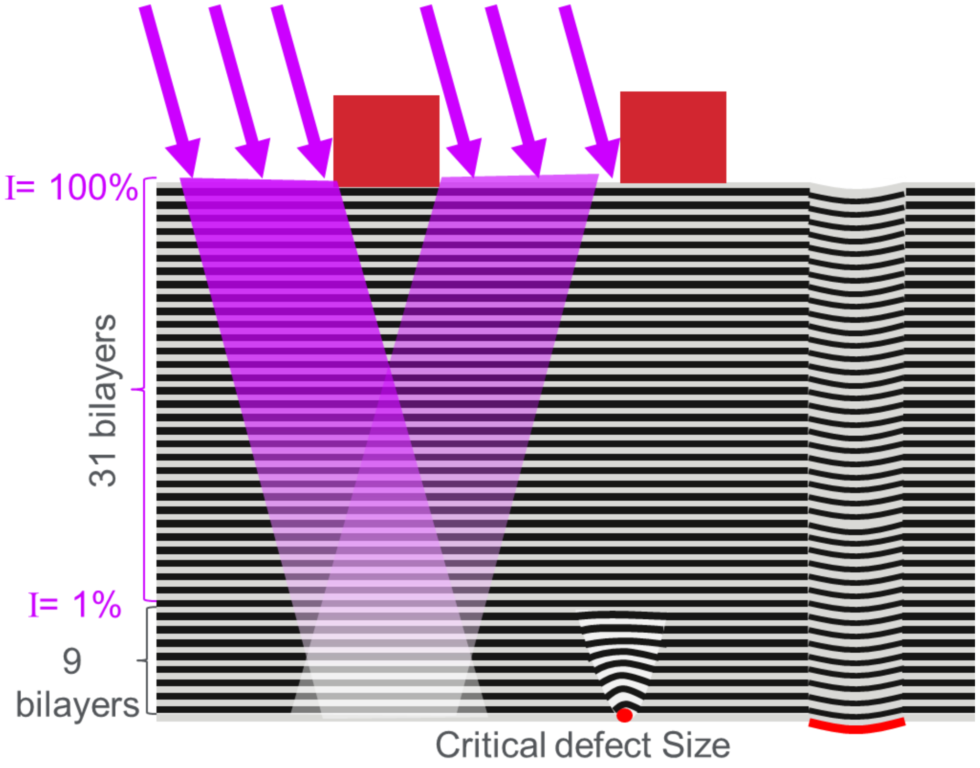
- Increase in EUV source power (>250 W)
  - More heat should be dissipated by substrate
  - Depending on cooling rate higher T_{zc} LTEM material may required
- Substrate roughness
  - Should be about 50 pm (HFSR) for inspection and defectivity
- Substrate flatness
  - PV < 10 nm may required to reduce overlay errors
- Substrate defectivity
  - Critical defect size of defect on substrate may not change

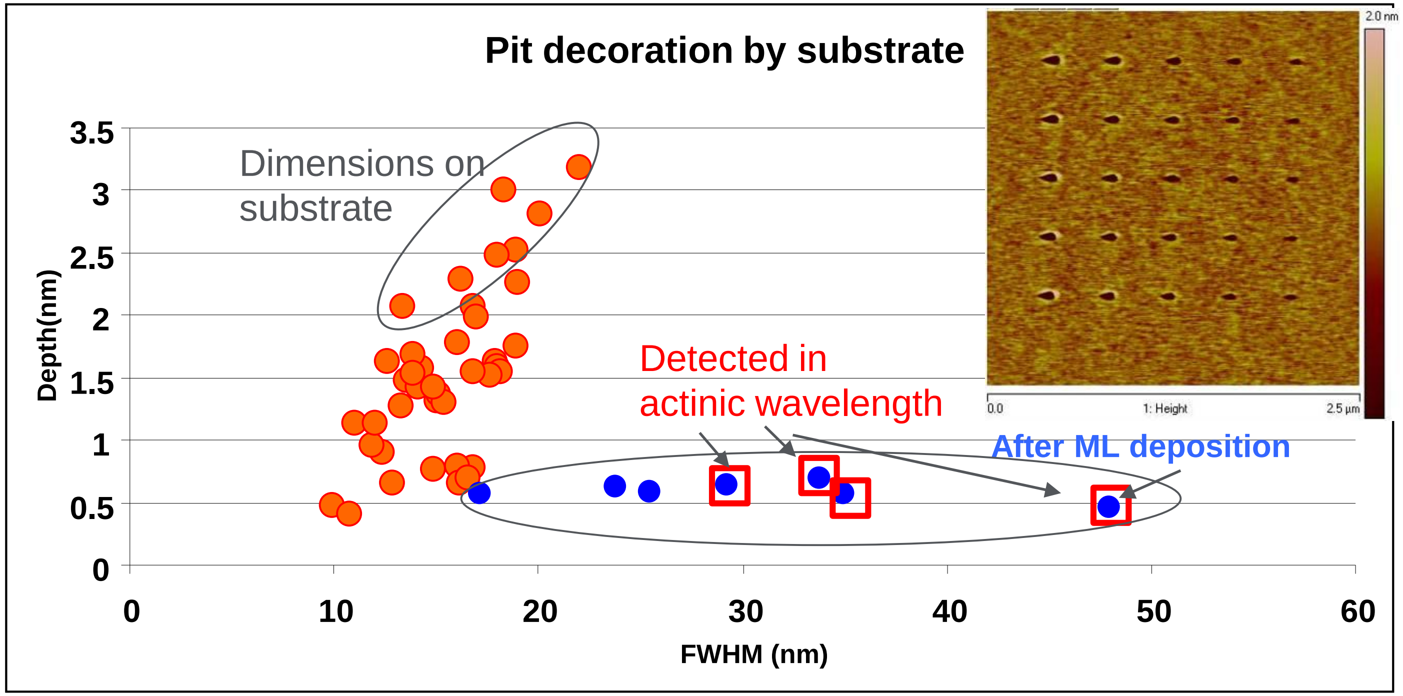




Ken Hrdina &Carlos Duran , EUVL 2012

Printable substrate defects





Rastegar SEMATECH Mask Cleaning Workshop 2011

- All pits defects on substrate with (depth< 2nm, width < 20 nm) were smoothed by deposition process
- Only defects with (depth >0.6nm, width >30 nm) on multilayer were detected by actinic inspection at the time

Substrate defects with (height/depth > 2nm and FWHM > 20 nm) (SEVD=12 nm)are critical

12 nm on mask → 3 nm on wafer

Summary & conclusions

- EUV mask blank performance is determined by many interdependent parameters of substrate that need to be optimized simultaneously
  - Surface flatness (PV, local slope and bow)
  - Surface roughness
  - Defectivity
  - Multiple polishing tools and cleaning tools and process need to be optimized.

Substrate development took > 10 years in industry

- As multilayer deposition processes are becoming efficient, substrate yield will be the main driver for the price of the EUV blanks
- The higher power EUV source and pellicles will generate more heat on substrate that require LTEM materials be optimized for higher temperature (Higher T_{ZC})
- Applied Materials has demonstrated considerable improvement in substrate development within a year
  - Defectivity: 3 order of magnitude reduction→ 6@ 34 nm
  - PV: 6x reductions→ PV=52 nm (16 nm Adv. polishing)
  - Bow: 25x reduction→ bow = 6 nm

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