Enabling the Semiconductor Roadmap from a Multi-Angled Approach

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Steven Welch

Senior Director of Strategy, Advanced Product and Technology Development, Applied Materials
Steven Welch is currently Senior Director of Strategy for Applied Materials’ Advanced Product and Technology Development group. In this role, he is responsible for identifying and synthesizing key inflections in the longer-term Semiconductor technology roadmap, as well as enabling disruptive technology development and business growth strategies to intercept these emerging opportunities. With over 20 years in the industry, Steven started his career in 1998 as a photolithography engineer at IBM’s Storage Systems Division in San Jose, California. Since then, he has held marketing and strategy leadership positions in KLA-Tencor’s wafer inspection, Applied Materials’ etch, and ASML’s holistic lithography businesses. Steven holds a B.S. in Chemistry from Harvey Mudd College and MA & MBA degrees from the University of Pennsylvania’s Wharton School of Business.
Semiconductor Scaling and Enablers

Logic Scaling Advancements

Memory Advancements to Scale A.I. Big Data
Semiconductor Scaling and Enablers

Logic Scaling Advancements

Memory Advancements to Scale A.I. Big Data
Market Growth and Evolution

- **Mainframe Computing** (1988) - 100,000s of units
- **PC + Internet** (1998) - 100 Millions of units
- **Mobile + Social Media** (2008) - Billions of units
- **A.I. Big Data** (2018) - Trillions of units
Industry’s Old Playbook...

MOORE’S LAW

<table>
<thead>
<tr>
<th>COMPONENT PER IC</th>
<th>RELATIVE COST/COMPONENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>100</td>
<td>10</td>
</tr>
<tr>
<td>1000</td>
<td>10</td>
</tr>
<tr>
<td>10000</td>
<td>10</td>
</tr>
</tbody>
</table>

1962 1965 1970

ENABLED BY

“Classic” 2D feature shrinking +
materials engineering to drive power and performance

Now: Apple A12X Bionic
>10 billion transistors

https://wccftech.com/apple-a12x-10-billion-transistors-performance/
In the Future…

ENABLED BY

New architectures
New structures / 3D
New materials
New ways to shrink
Advanced packaging

… New industry playbook needed to drive PPAC
Moore’s Law beyond 5nm Node?

Adapted from Nature Electronics, V1, August 2018, 442–450
AGENDA

Semiconductor Scaling and Enablers

Logic Scaling Advancements

Memory Advancements to Scale A.I. Big Data
CMOS Scaling and Enablers

<table>
<thead>
<tr>
<th>Material</th>
<th>Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strain</td>
<td>High-k Metal Gate</td>
</tr>
<tr>
<td>FinFET</td>
<td>taller/ narrower &amp; fewer fins</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Node</th>
<th>65nm</th>
<th>45nm</th>
<th>22/14nm</th>
<th>10/7nm</th>
<th>5/3nm</th>
<th>3nm</th>
</tr>
</thead>
</table>

New Materials: New metal gate and new contact fill
New Architecture: FinFET to hGAA

Samsung announced GAA 3nm node processor will ship in 2021

Source: AMAT, SMC Korea 2019 conference
Why *Horizontal*-GAA ➔ Evolutional Change

**FinFET**

- Thinner & Taller Fins
  - Better gate control & higher drive current

**hGAA**

- Vertically stackable channel (NW/NS) for increased current per area

**SiGe p-Channel**

- Mobility boosting

**Similar structures & flows: hGAA vs. FinFET**
hGAA CMOS Initial Demonstrations

Transfer Characteristics

Ring Oscillator

Source: IMEC/ Applied Materials, IEDM 2018

Functional CMOS demonstrated – getting ready for ≤3nm-node
hGAA CMOS – Key Challenges

Parasitic capacitance reduction between sheets

Metal-gate Vt tuning in narrow gaps

Source: AMAT, SMC Korea 2019 conference

IBM, IEDM 2017

IBM VLSI-T 2017

Epi defects
Beyond Conventional CMOS (≤2nm)

More new materials

Ge channel

Boosters

SiGe PFET

Buried Power Rail (Ru)

New devices

NCFET/Ferro (HZO)

SpinFET

Tunnel FET

2D TMD (MoS$_2$)

Complementary FET

Co-integration (VFET, TFT)

New scaling

3D integration (M3D)

Source: AMAT, SMC Korea 2019 conference
Selective Processes – Enabling New Ways to Build Chips

Inherent Selective

Selective by Deactivation

Selective by Activation

Selective Deposition

ANALOGY: 3D Printing – putting material only where you want it (materials-enabled not litho)

Selective Removal

ANALOGY: Removing a single weed without damaging adjacent grass or leaving residue

Scaling Opportunities in the Back-end-of-line Interconnect

BEOL Cu wire resistance (R) increasing at smaller geometries due to:

- Inherent bulk conductor resistivity characteristics
- Trade-off fill volume of high-conducting vs. cladding materials
- Scattering at surfaces and grain boundaries

…resulting in slower performance and higher power consumption

Materials-Engineering Solutions:

- New materials (lowest R at CD)
- Full-volume metal fills
- Interface management

Source: AMAT, IEDM 2018 conference
Copper Extension Scenarios

Co-optimization of ALD barriers with thinner liners and new fill technology is key to maximize conductor volume (low line R) and minimize interface resistance (low via R)

Source: AMAT, IEDM 2018 conference
New Metals for Resistance Scaling

Co, Ru, Mo better than Cu at CD’s between 10-15nm
Ir better than Cu at CD’s between 15-20nm

Is a barrier or liner required?
How to fill?
Can it be integrated?

Source: AMAT, IEDM 2018 conference
AGENDA

Semiconductor Scaling and Enablers

Logic Scaling Advancements

Memory Advancements to Scale A.I. Big Data
Emerging Memories for Pervasive Data and Compute

Source: [http://www.imec.be](http://www.imec.be) from techspot.com (February 21, 2019)
Significant investments in memory to enable better bit scaling and performance
3D Architectures

3D architectures extend memory densities

Source: Intel 2015
S. Kang, IMW2018 tutorial
Materials and Interfaces

- Complex stacks with multiple exotic materials are required to enable new memories
- Deposition, etch and CMP are critical process development areas
Example of Elements to Enable New Memories

PCM Selector
- M.K. Lee, IEDM 2012
- G.H. Kim, APL 2012
- L. Zhang, IEDM 2014

STT-MRAM
- K. Ando, JAP 2014

FE-FET
- X. Tian, APL 2018
- A. Pal, APL 2017

CBRAM
- Adesto Technologies, IEEE 2013 talk
Packaging enables higher performance to support more complex workloads

YMTC.com (2018)

Nvidia V100 source: techreport.com 2017
Beyond Chip Scaling: Advanced Packaging

**DRAM ON PCB to STACKED DRAM IN PACKAGE**

- **3x**
  - Logic ↔ DRAM bandwidth performance

- **50%**
  - Power savings per bit

**HETEROGENEOUS INTEGRATION**

System on Chip to System on Package

Integration of chiplets provides **time, cost** and **yield** benefits

Connecting chips together in new ways using advanced packaging

**Sources:** Intel, GLOBALFOUNDRIES

**Table:**

| Component          | Technology | Performance
<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>SUBSTRATE (PCB)</td>
<td>Si Interposer</td>
<td></td>
</tr>
<tr>
<td>DRAM (stacked)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU CORES</td>
<td>10nm</td>
<td></td>
</tr>
<tr>
<td>COMMS</td>
<td>14nm</td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>14nm</td>
<td></td>
</tr>
<tr>
<td>OTHER IP</td>
<td>22nm</td>
<td></td>
</tr>
</tbody>
</table>
Distributed computing further reduces memory bottlenecks
→ SRAM
- MRAM alternative to improve area + energy efficiency
<table>
<thead>
<tr>
<th>Date</th>
<th>Company/Announcement</th>
</tr>
</thead>
<tbody>
<tr>
<td>8/2017</td>
<td>Everspin announced sampling of the world’s first 1Gb MRAM product</td>
</tr>
<tr>
<td>9/2017</td>
<td>Global Foundries announced availability of embedded MRAM on leading 22FDX FD-SOI platform</td>
</tr>
<tr>
<td>7/2018</td>
<td>TSMC “Over 50 customers and 140 tapeout in N22ULP, spanning many application areas… connectivity, digital TV/STB, application processors.”</td>
</tr>
<tr>
<td>11/2018</td>
<td>Spin Memory &amp; Applied Materials commercial agreement to create a comprehensive embedded MRAM solution</td>
</tr>
<tr>
<td>12/2018</td>
<td>Gyrfalcon Technology announced the commercial availability of its AI ASIC that include TSMC’s 22nm eMRAM</td>
</tr>
<tr>
<td>12/2018</td>
<td>Intel described the first FinFET-based MRAM technology (22nm) is production ready</td>
</tr>
<tr>
<td>12/2018 IEDM conference</td>
<td>Samsung showed MRAM design technology co-optimization for hardware neural networks</td>
</tr>
<tr>
<td>3/2019</td>
<td>Global Foundries showed 22nm embedded 40 Mb MRAM for low-power automotive MCU application</td>
</tr>
<tr>
<td>3/2019</td>
<td>Samsung shipped the first 28nm eMRAM</td>
</tr>
</tbody>
</table>
## MRAM Benefits

<table>
<thead>
<tr>
<th>Low Power &amp; Non-Volatile</th>
<th>High Density</th>
<th>More Functionality</th>
<th>Robust</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Graph showing energy vs size for MRAM and SRAM" /></td>
<td><img src="image2" alt="Graph showing cell size in FinFET SRAM and MRAM" /></td>
<td><img src="image3" alt="Diagram showing MRAM implementation in MCU/SoC" /></td>
<td><img src="image4" alt="Image showing MRAM benefits" /></td>
</tr>
</tbody>
</table>

- **IMEC DTCO studied:**
  - MRAM write energy < SRAM @ 5MB
  - MRAM read energy < SRAM @ 0.4MB

- **MRAM is with > 3x cell density than SRAM**

- **Greater benefit in advanced node**

- **MRAM implementation in MCU/SoC:**
  - 45% chip size saving (~ one advanced technology node advantage) **OR**
  - 1.5-2x more processors at same chip size

- **MRAM for high temperature, low-power operations:**
  - 22nm embedded 40 Mb MRAM could be used between -40 to 150 degrees C with good read and write characteristics and immunity to 500 Oersted magnetic fields.

Source:
- IMEC, IEDM 2018
- SpinMemory.com 2019
- Spintec ORaP Forum 2015
- GF, IEDM 2018

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### CMOS Technology Node (nm)

- **FinFET SRAM**
- **MRAM**
- **Planar SRAM**

- ![Image showing CMOS technology node comparison](image5)

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**Source:** Everspin.com
MRAM Capability Demonstrated by Optimization of Complex Stack

Sources: Applied Materials

Roadmap for additional density and performance scaling in development
Analog vector-matrix multiplier: reduced complexity and power; will require further advances in process variability.

- 12x12 array, Bell Labs 1986 cited by LeCuin, ISSCC 2019
- CAS, IEDM 2017
- Tsinghua, IEDM 2017
Emerging Memory for Machine Learning Accelerators

1. Digital Accelerator

SRAM → MRAM available in Foundry

“The 2802M ASIC has 40MB of eMRAM memory, which can support large AI models or multiple AI models within a single chip.” – gyrfalcontech.ai 2019

- MRAM can enable area benefit at lower power versus traditional distributed SRAM techniques

2. Analog Accelerator

eFlash → RERAM, FEFET, PCRAM in Development

In-memory Compute Vector-Matrix Multiplier

Weights: Conductance of NVM

Matrix multiplication in hardware (Ohms, Kirchhoff law)

“1,000 to 10,000 better speed-energy efficiency product than digital ASICs” - HPE, ACM 2016

- New analog memories, once performance at scale is robust, can enable additional performance boosts @ density and new ways of compute
PPAC Optimization Beyond the Chip