EUV Ecosystem Expansion into DRAM Manufacturing

2021 EUVL Workshop

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Scott Light (Micron)
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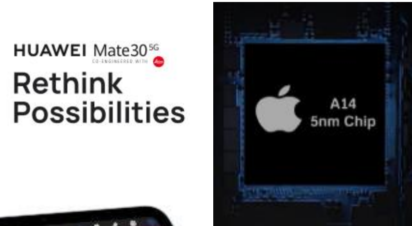
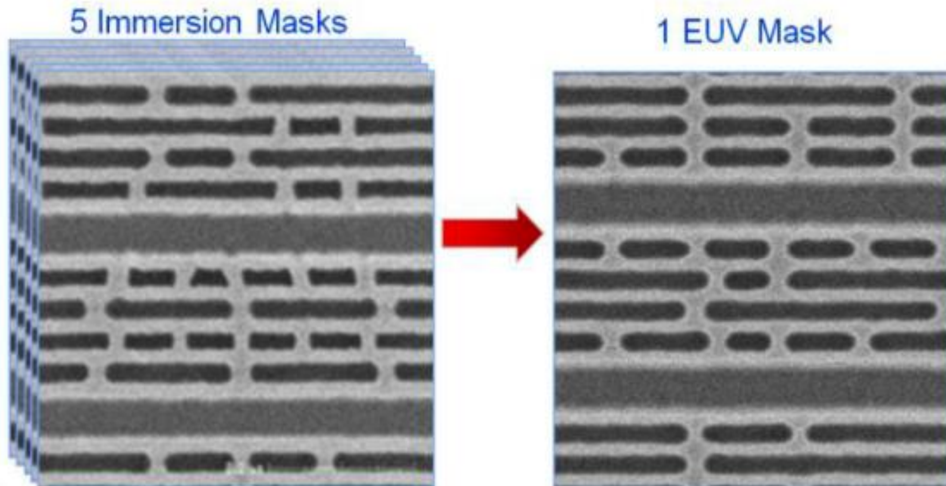
EUV Becomes an HVM Process in 2019 – 2020

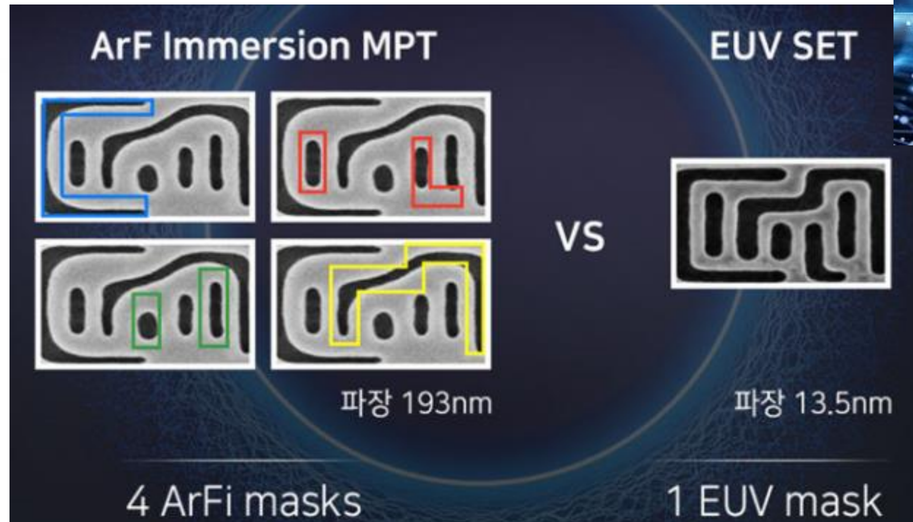
- 7nm+ has EUV at ~3 levels
  - First: Kirin 990, Huawei Mate30 phone in 2019



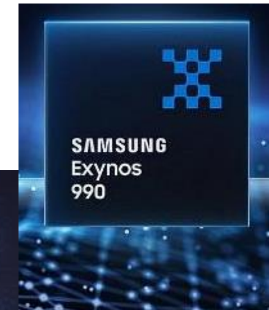
- 5nm uses EUV at >10 levels
  - First: Apple A14 Bionic
  - October 2020 Apple iPad Air
  - Charges **$17,000 per wafer**

- Converts 5 193i masks into 1 EUV level





- 7nm logic is EUV
- Galaxy Note 10 first product with Exynos 9825 EUV CPU in 2019
- Galaxy S20 with Exynos 990 in 2020
- EUV **capacity tripling** in 2020
- DRAM EUV Roadmap 2020
  - D1x used for customer qual
  - D1z 1 level
  - **D1α/D1β >90% critical**



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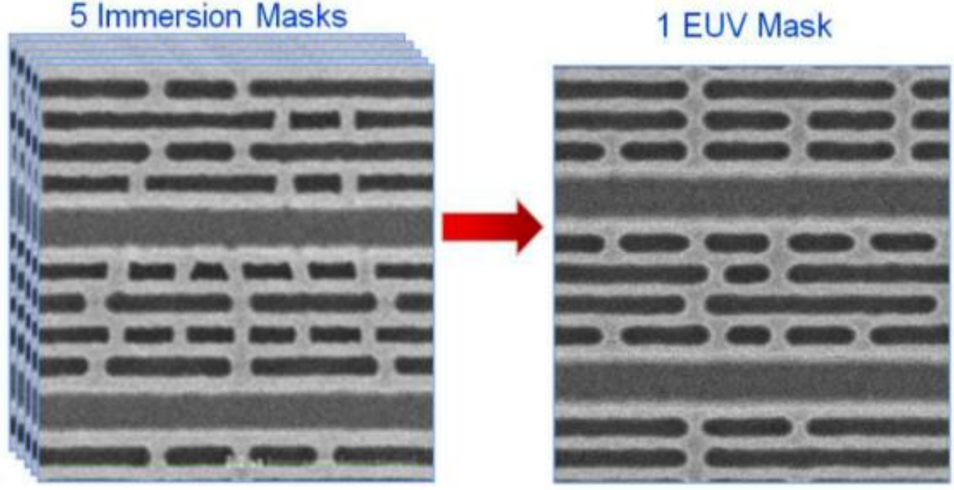

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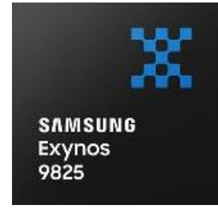
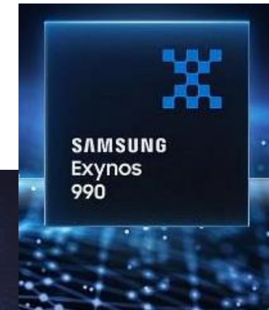
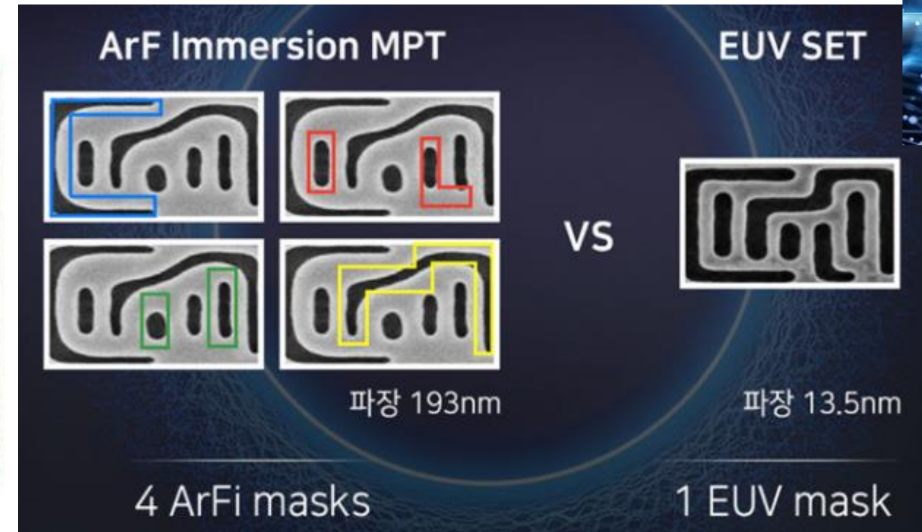
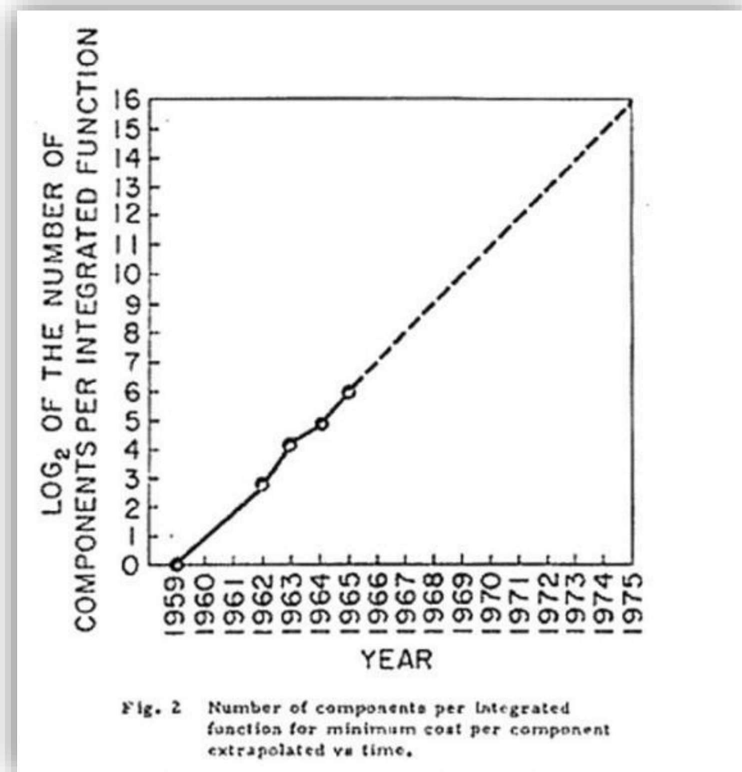


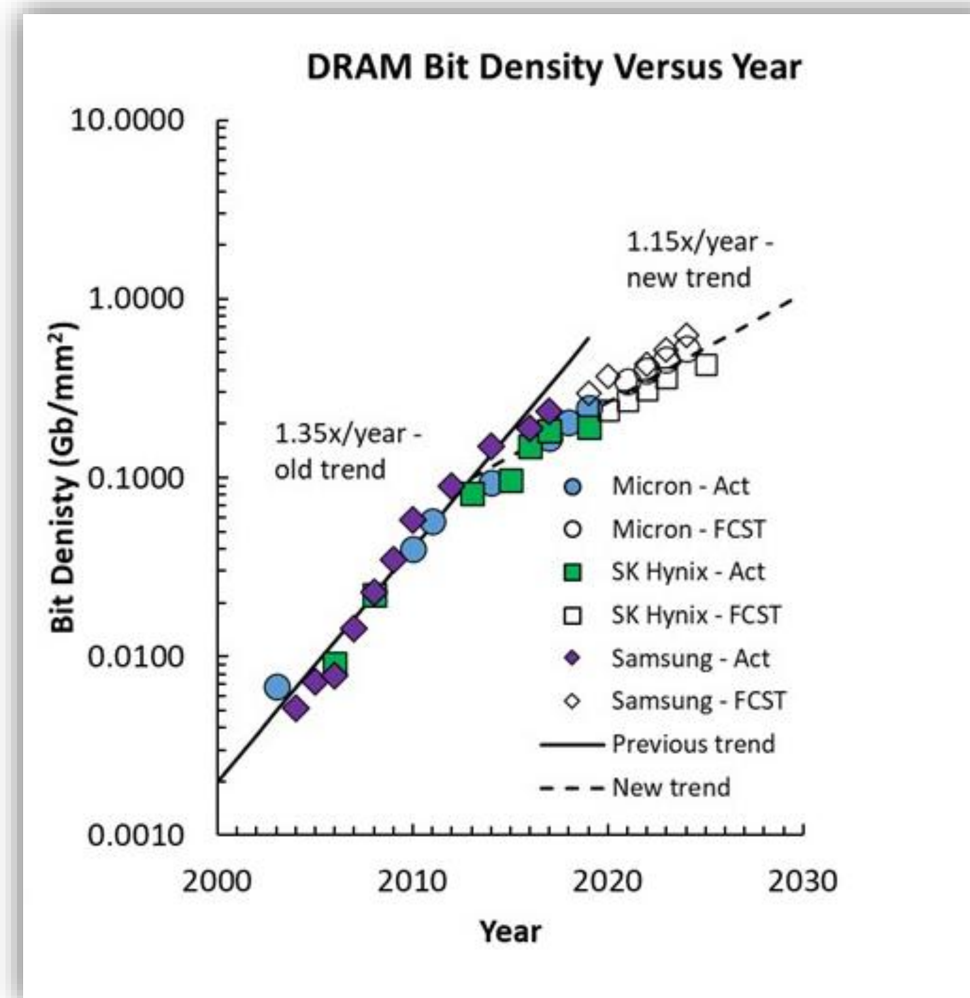




Moore’s Law for DRAM



Gordon Moore - Electronics, Volume 38, Number 8, April 19, 1965 - https://newsroom.intel.com/wp-content/uploads/sites/11/2018/05/moores-law-electronics.pdf



From IC Knowledge - https://semiwiki.com/semiconductor-services/297904-spie-2021-applied-materials-dram-scaling/

- Moore’s Original Prediction from 1965
- DRAM Moore’s law scaling of Bit Density 2000 – 2025
- Both are driven by economics, so where does EUV make economic sense?

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DRAM vs Logic Die Cuts

DRAM – Array with Cap + Periph (CMOS)

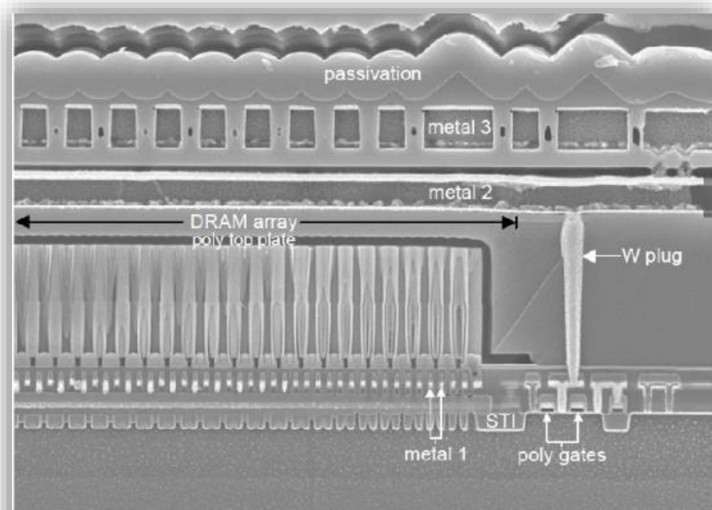
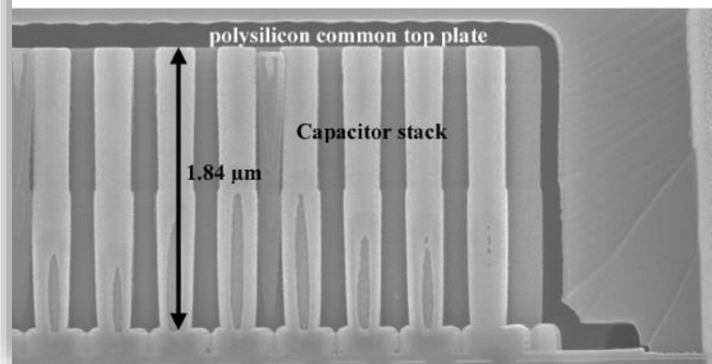
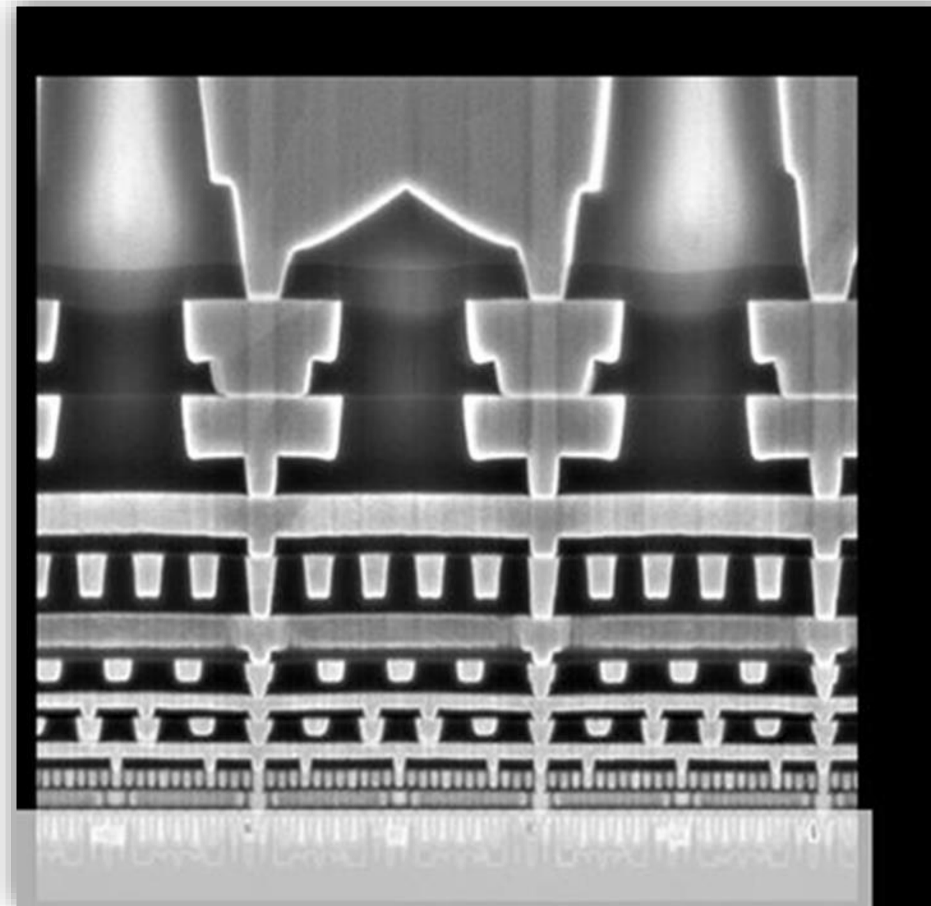


Fig. 2. Cross-Section of Samsung 90-nm 512 Mb SDRAM



Source: D James Recent innovations in DRAM Manufacturing (2010).

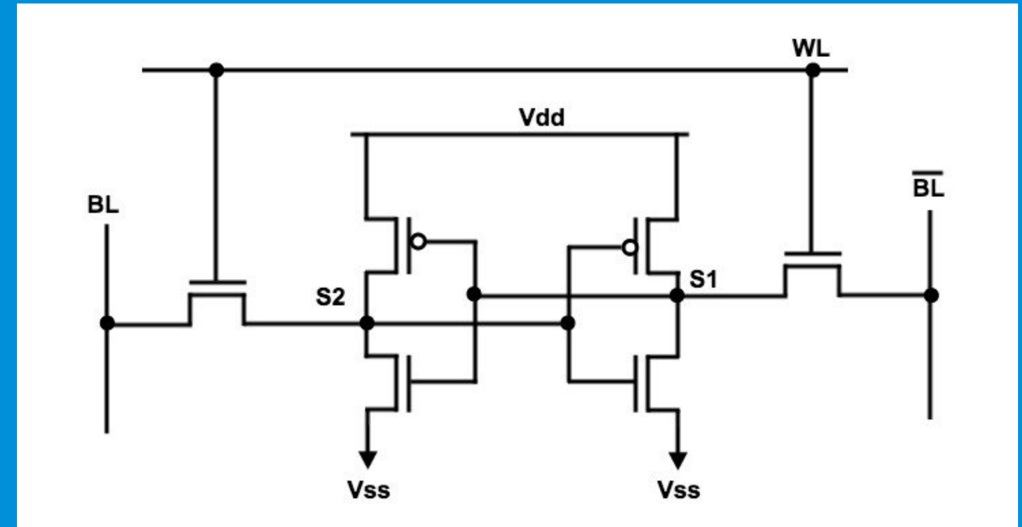
Logic – CMOS Transistors with lots of routing



Source: D Schor WikiChip Fuse (2018).

Logic EUV Use Cases

1. Sparse vias
2. Metal Routing
3. 2D Features

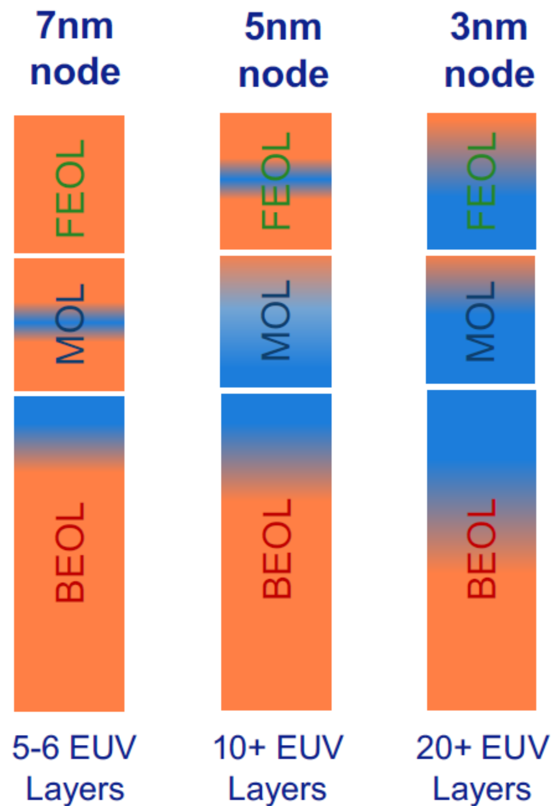


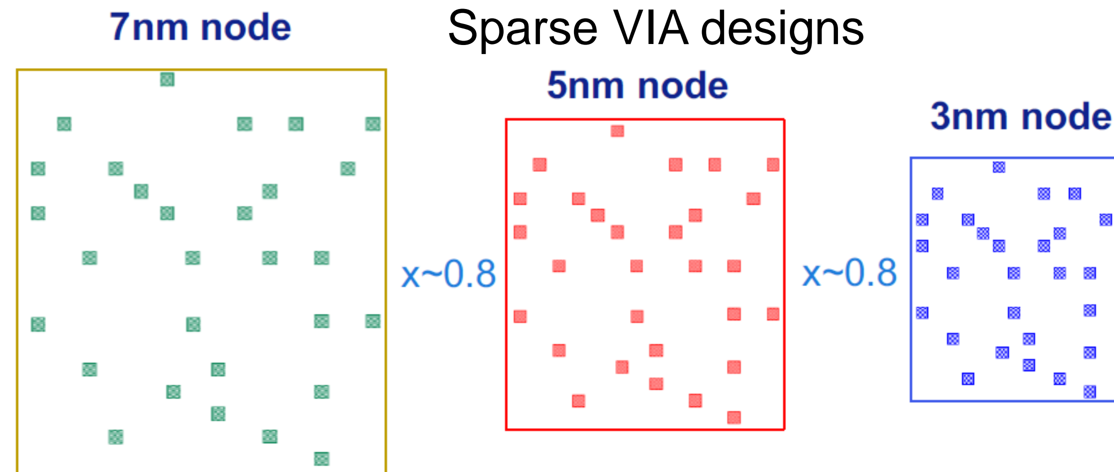
Logic Usage

Source: Eltawil, Ahmed & Niar, Smail & El Sharkasy, Wael & Alouani, Ihsen & Kurdahi, Fadi. (2016). AS8-static random access memory (SRAM): Asymmetric SRAM architecture for soft error hardening enhancement. IET Circuits, Devices & Systems. 11. 10.1049/iet-cds.2015.0318.

EUV Intercept at Logic 7nm Node – ASML

Trends of EUV layers #'s and Via pitches in Logic IC





- Our studies indicate that Via pitches shrink by ~20% node to node
  - Min. pitch of Via layers ranges from 38 – 44nm in the 3nm node
  - EUV SP for Via layers is key to maintaining cost-effectiveness
  - This is still a work in progress

193 immersion process | EUV process

FEOL: Front End of Line; MOL: Middle of Line; BEOL: Back End of Line

- **MOL and lower BEOL levels first to utilize EUV in Logic**
- These would be Contact/M0 and V0/M1 in a FinFET flow
- Note: Tony Yen is at ASML now, but formerly at TSMC

Source: Tony Yen – ASML (VLSI Symposium 2020)

Samsung EUV Usage 7nm

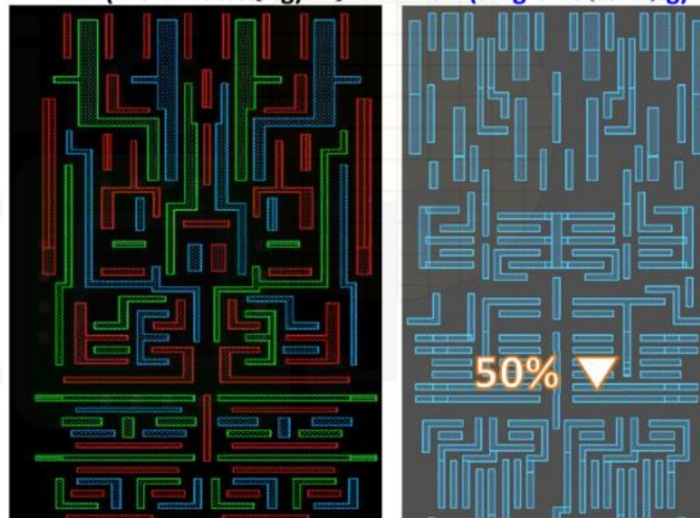
- Notes wider depth of focus
- 7nm **metal routing** images for LELELE(LE) -> EUV conversions

Imaging advantage of EUV

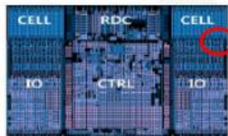
Source: AnandTech

- EUV has bigger depth of focus as well as better resolution

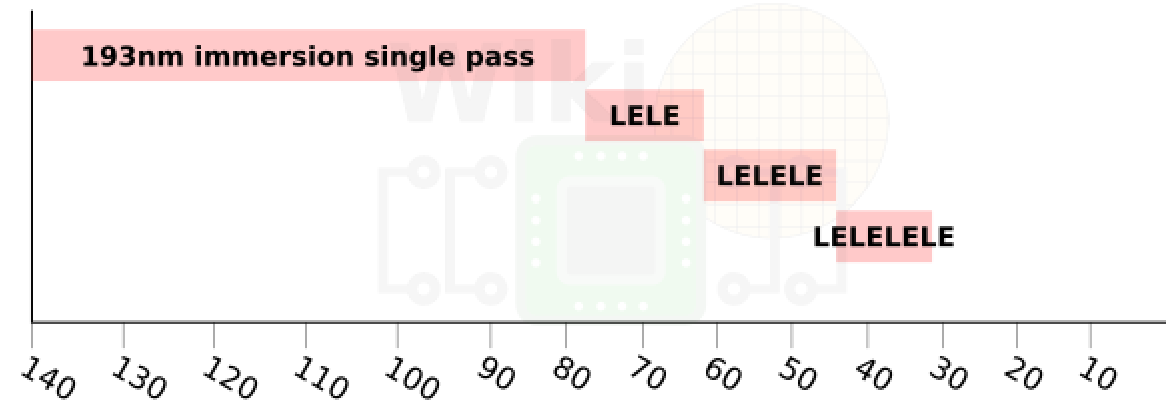
Samsung **7nm** Metal - EUV

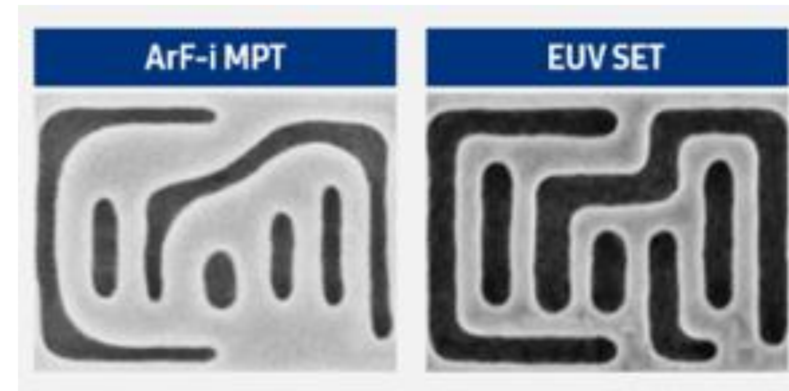


Source: WikiChip



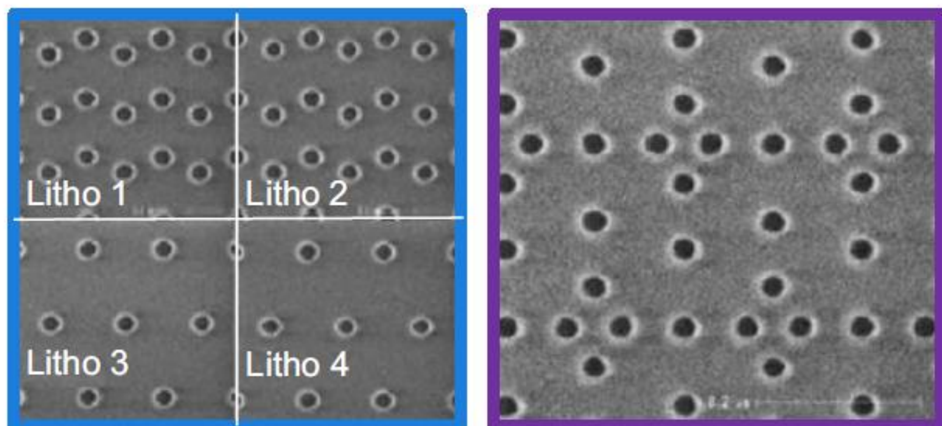
Samsung **10nm** 48nm MMP - LELELE



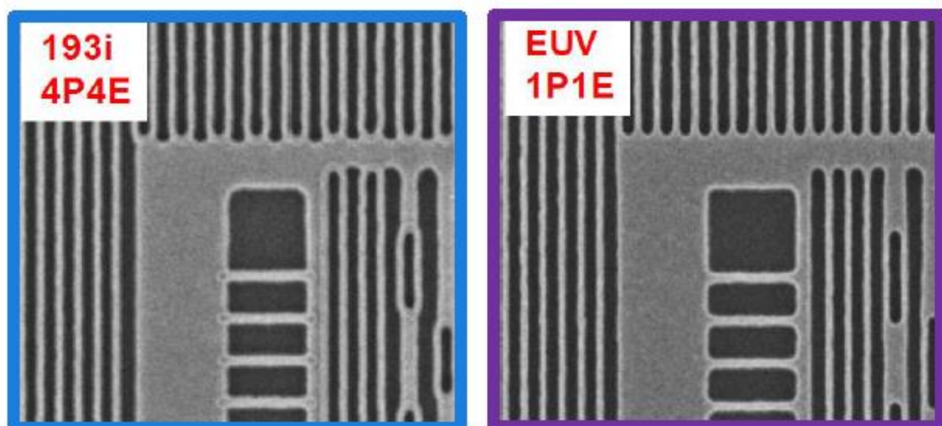


Source: WikiChip

EUV Usage at TSMC 5 and 7nm Nodes



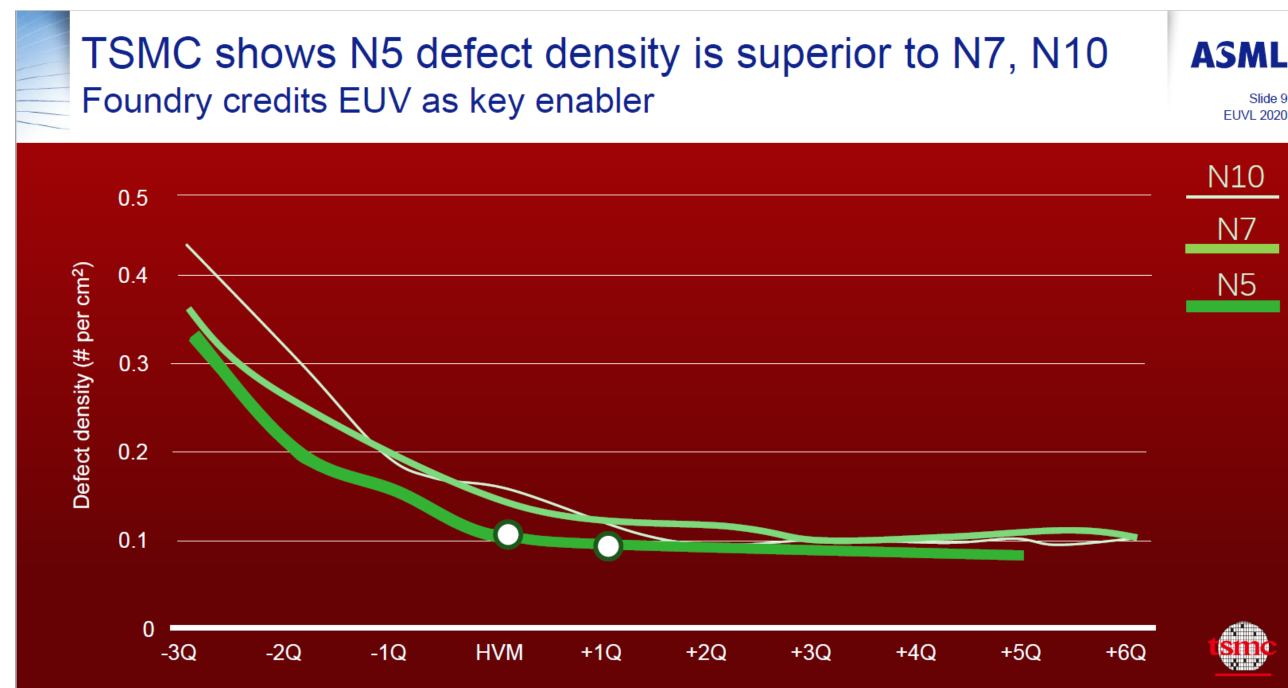
Via with 193i multiple patterning (left) vs. EUV single-patterning (right)



Metal with 193i multiple patterning vs. EUV single patterning

S.-Y. Wu (TSMC), "Key Technology Enablers of Innovations in the AI and 5G Era," IEDM, San Francisco, 11 December 2019

Source: Tony Yen – ASML (VLSI Symposium 2020)



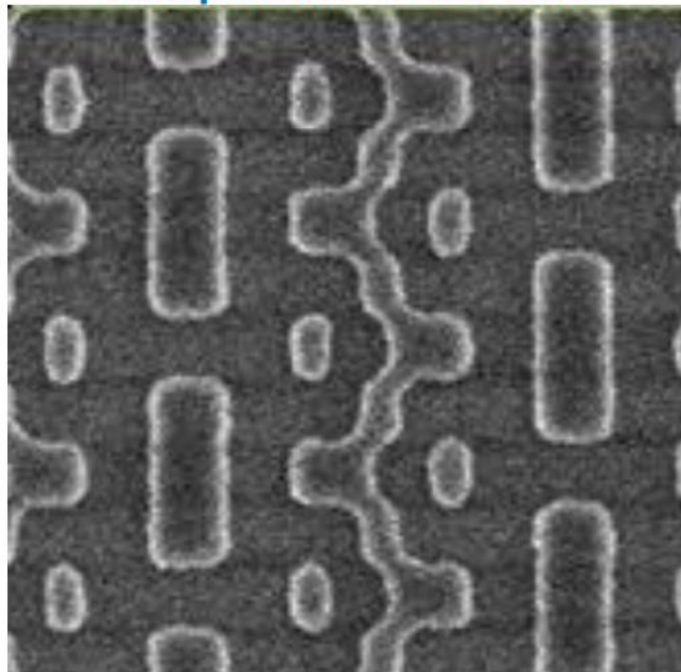
Source: Martin van den Bink – ASML (SPIE EUVL + PM 2020)

- TSMC notes that EUV has led to faster defect density reductions in leading nodes.
- Noting multiple mask reductions for 4 (193i) → 1 (EUV) insertion points
- **Cut, contact, via and metal line all listed as intercepts**

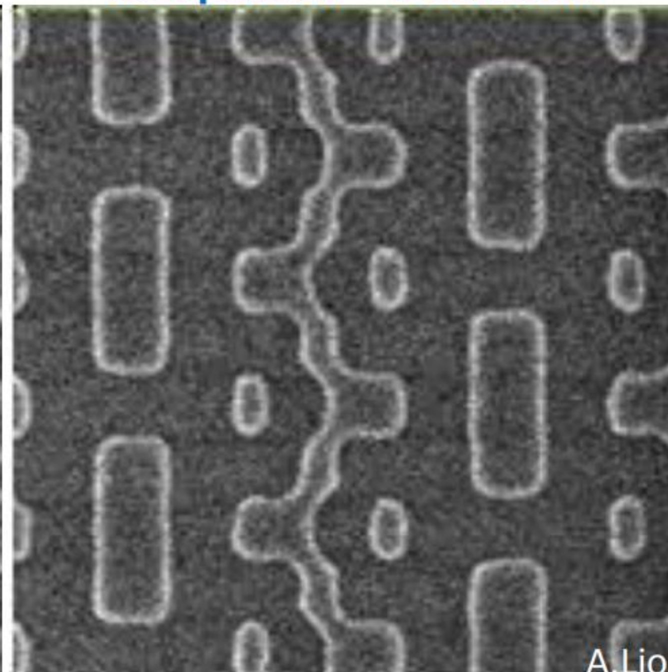
Intel EUV – 2018 Public Disclosure

EUV materials and resolution

Test pattern – Post Litho



Test pattern – Post Etch



- EUV enables 2D design features, e.g. corner segments
- Need materials that can take advantage of improved EUV resolution
- Adequate for EUV introduction
- Need materials that are tunable for desired properties
- Materials development constrained by photon availability (BL, MET, NXE)

For continued material development, suppliers need an understanding of fundamental properties of materials

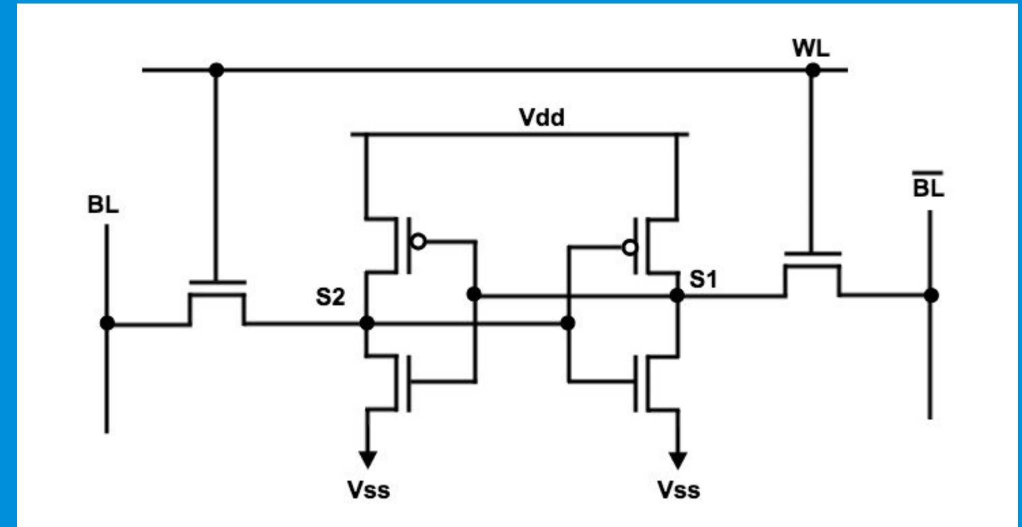
Britt Turkot/Intel 2018 International Workshop on EUV Lithography, 12 June, Berkeley, California intel 23

- Noting the very nice corner fidelity given by EUV and ability to maintain it through etch
- **2D features also noted to be enabled by EUV**

Source: Britt Turkot – International Workshop on EUV 2018

Logic EUV Use Cases

1. Sparse vias
2. Metal Routing
3. 2D Features



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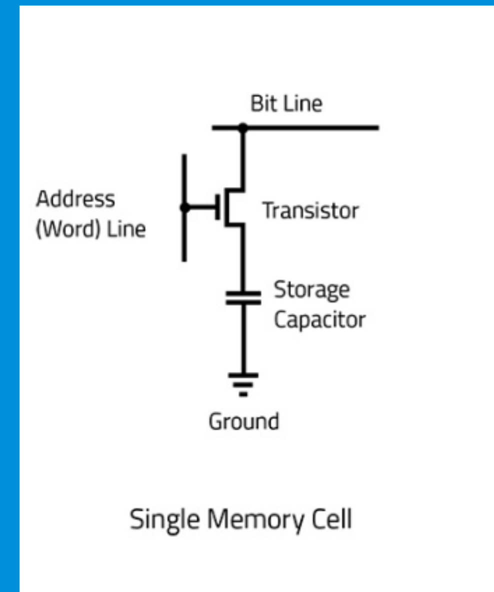
DRAM EUV Use Cases
1. Metal Routing
2. Dense Pillars/Contacts



Source: LAM Research

DRAM Memory Usage

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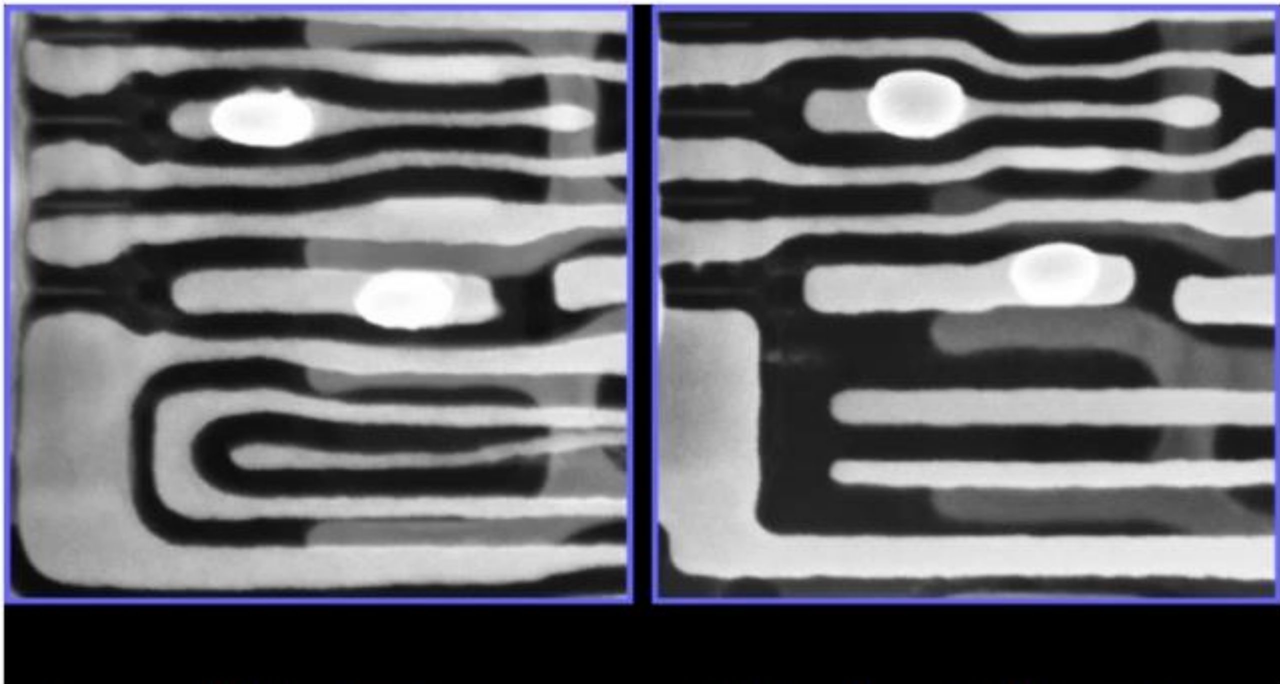
Samsung EUV DRAM Usage

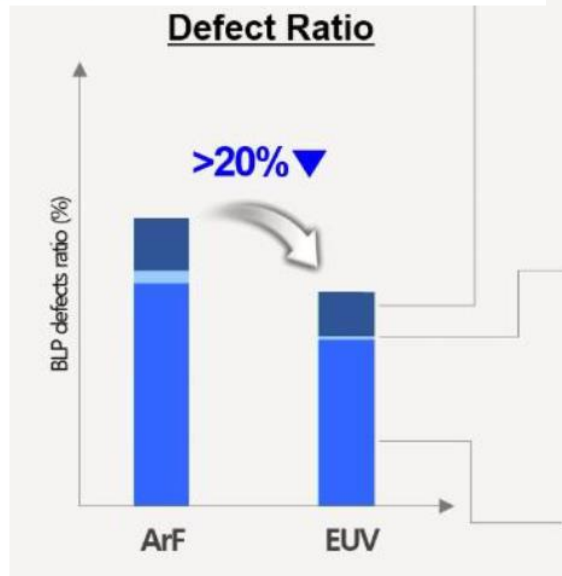
- Samsung has an EUV DRAM product in the market.
- First samples using EUV for SNLP/BLP (Storage Node Landing Pad/Bit Line Pad)
- **Use here is metal routing and dense pillars**



Samsung DRAM cell design, a comparison of BLP patterns on D1z (a) without EUVL and (b) with EUVL.

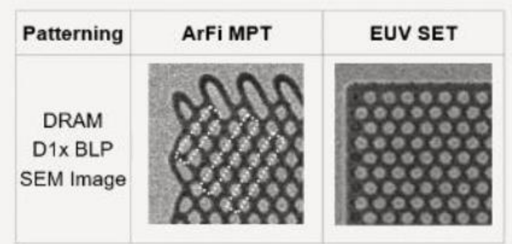
BLP for D1z DRAM

Source: Jeongdong Choe, EE Times/TechInsights (2021)



BLP for D1x DRAM

✓ Eliminating multi-patterning related defects



✓ Enhancing patterning precision and cost

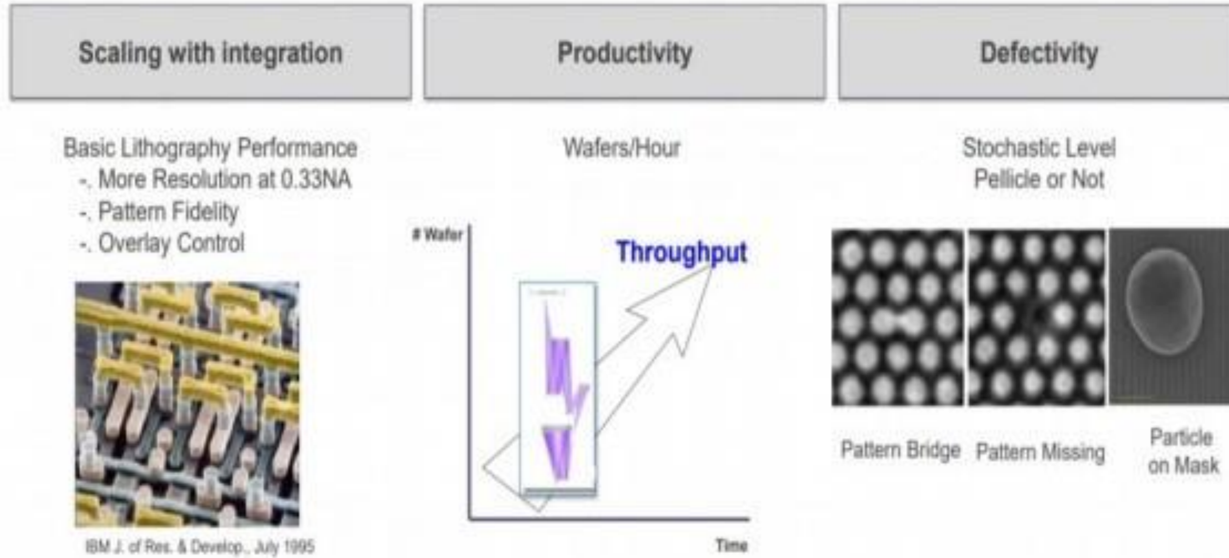
✓ Reducing number of steps and accumulated defects

Source: Samsung Investor Forum – Memory (Nov 2020)

SK Hynix EUV DRAM Usage

- Productivity and defects labeled as biggest obstacles to adoption
- **Examples of dense contact holes/pillar patterning**

What are the EUV challenges in DRAM HVM



BLP DRAM

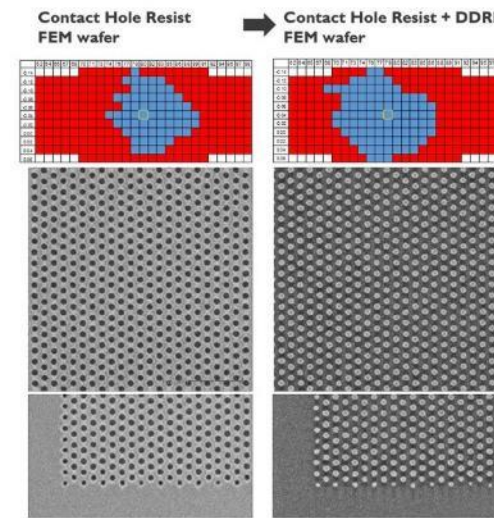
Source: Kang, Hyeryung, Korea IT News (2021)

BLP by C/H Reversal

TONE REVERSAL PROCESS FROM Px70XPy40 HOLES TO PILLARS BY NISSAN DDRP

Contact Hole Resist FEM wafer ➡ Contact Hole Resist + DDRP FEM wafer

DDRP = Dry Development Rinse Process



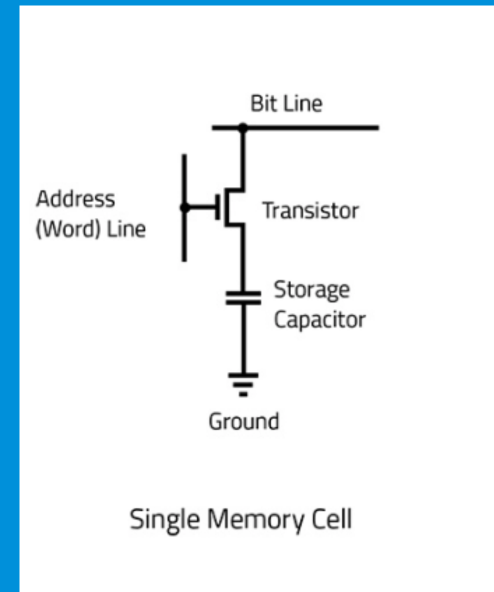
H70V40M23 CDU wafer	Dose mJ/cm2	CD nm	LCDU nm
Contact holes	78	21.41	2.97
Pillars by DDRM	78	22.68	2.69
Pillars by MOR	62	24.28	2.76

- Best LCDU obtained by DDRM Tone Reversal Process
- TPR can be an alternative process to make pillars.
  - Lower CH exposure dose resist to be considered

Source: Danilo De Simone, SPIE 2019.

DRAM EUV Use Cases

1. Metal Routing
2. Dense Pillars/Contacts



Source: LAM Research

DRAM Memory Usage

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> "What's impressive is that Micron is moving to manufacture these new chips without the use of EUV."

1α nm: Industry's Most Advanced DRAM

Volume production in 1H-CY21

1αnm DRAM: 8Gb DDR4

- ✓ Lowest power mobile DRAM with 15% improvement vs. prior gen
- ✓ Roadmap for highest speed DRAM available across comprehensive portfolio

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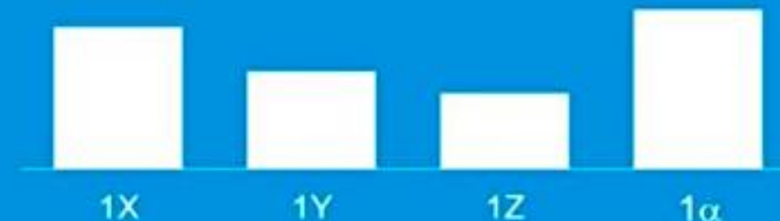
Achieved with Leading Design Efficiency and Process Technology

- ✓ Industry's most advanced lithography
- ✓ **40%** improvement in density vs. 1Z with **~10%** driven by design efficiency

DDR4 % Gb/Wafer Increase from Prior Node



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Source: Joel Hruska, Extreme Tech 2021, Micron Ships First DRAM Manufactured on Its 1 Alpha Node – ExtremeTech.

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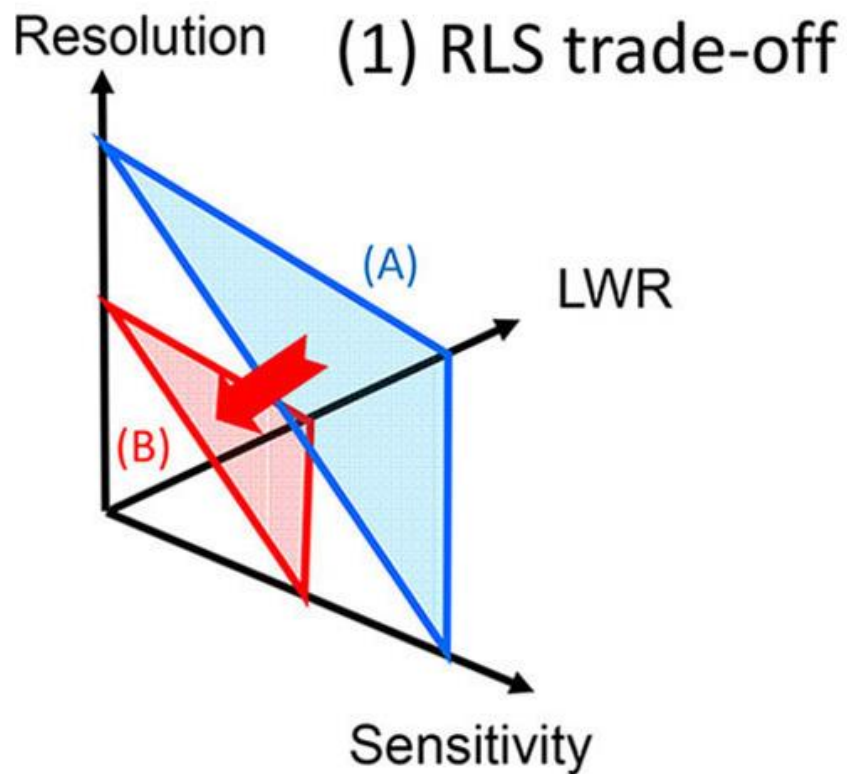
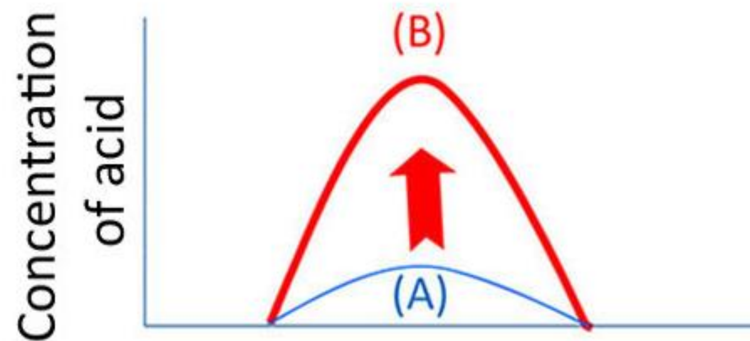
Famous RLS Tradeoff

- Reproduced from 2014 publication
- Still relevant today.





Seiichi Tagawa, SPIE 2014: https://spie.org/news/5311-photosensitized-chemically-amplified-extreme-uv/electron-beam-resist

DRAM Single Exposure EUV

1 defect identified out of 148.5M CHs at dose of 54mJ

Defect rate of $7x10^{-9}$ meets target of $1x10^{-8}$

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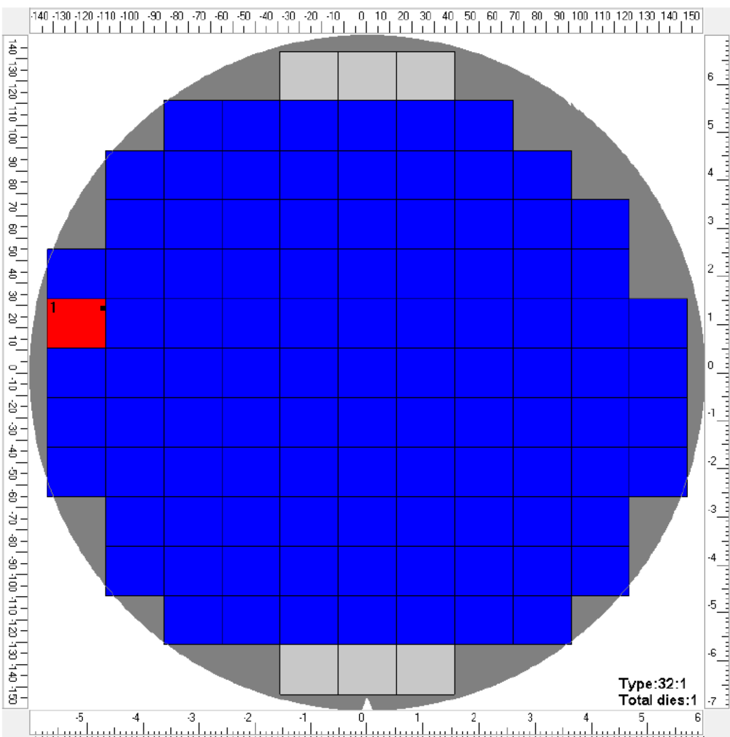
Slide 14
SPIE Feb 26 2020



- 102 fields
- 1.45 million holes/field

- CD = 20.4 nm
- LCDU = 2.7 nm

- 148.5 million holes
- 1 defect

- **Defect rate: ~$7x10^{-9}$**

- Hex C/H Array for Micron DRAM
- High Dose and high LCDU

No imaging stochastic defects are visible in 148.5 Million holes

The observed defect looks like an external particle

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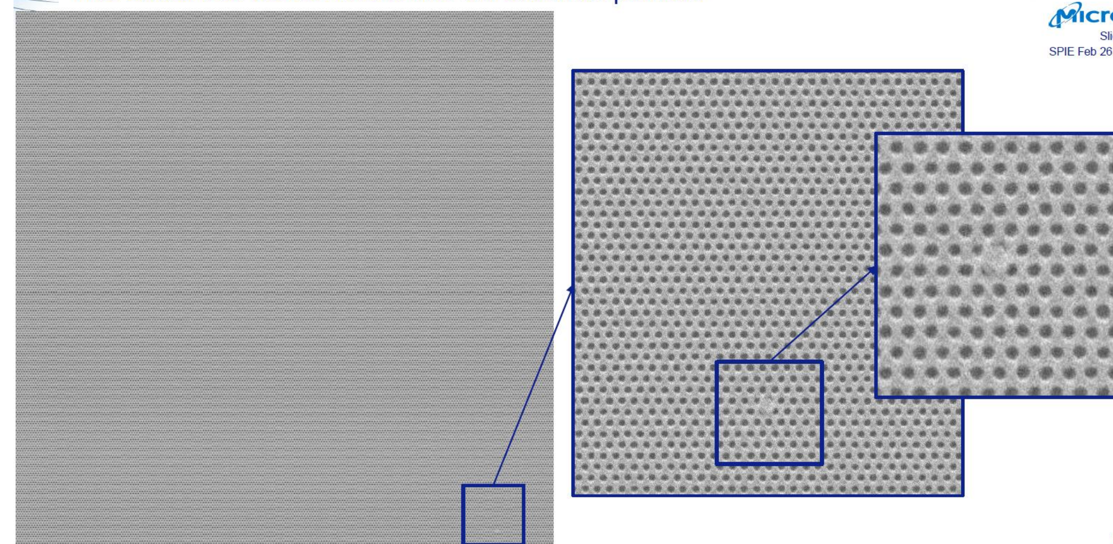
SPIE Feb 26 2020



Public

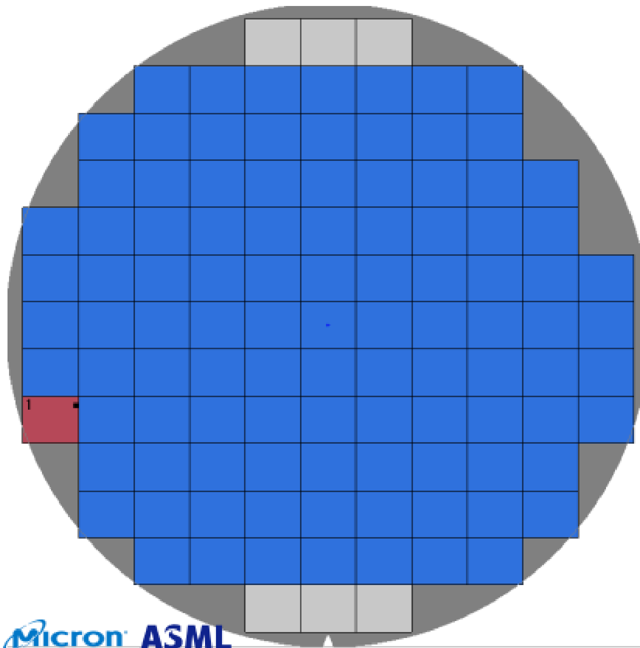
Source: ASML/Micron/IMEC SPIE 2020

Defect verification AEI

1 defect identified in >150million holes

ASML

Slide 11
26 February 2021



- 103 fields
- 1.45 million holes/field
- CD = 20.3 nm
- LCDU = 2.6 nm
- >150 million holes
- 1 defect
- **Defect rate: ~7x10^{-9}**

imec Micron ASML

- Hex C/H Array for Micron DRAM
- High Dose and high LCDU

DRAM Single Exposure EUV

Full solution for EUV lithography single exposure

By tuning the etch recipe, the LCDU after litho can be retained

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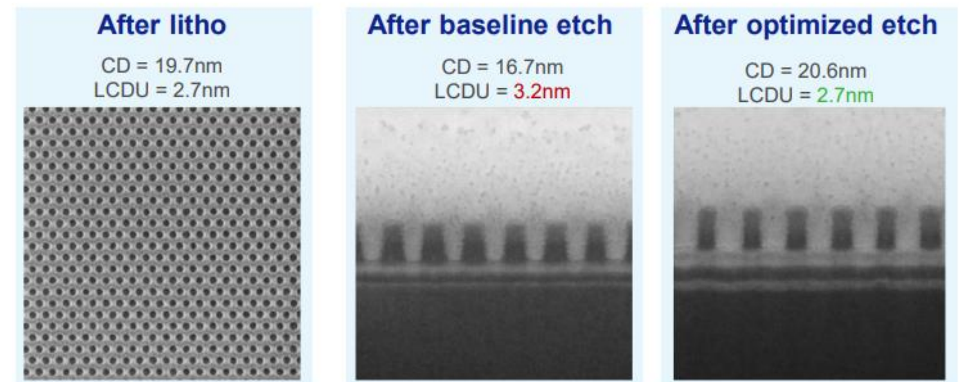
Slide 10
26 February 2021



imec Micron ASML

Source: ASML/Micron/IMEC SPIE 2021

Public

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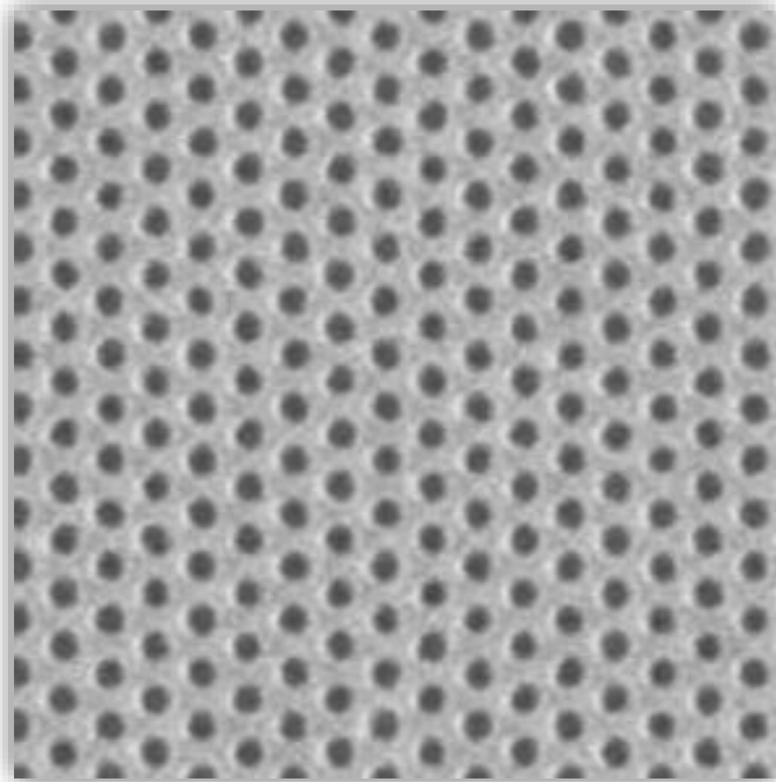
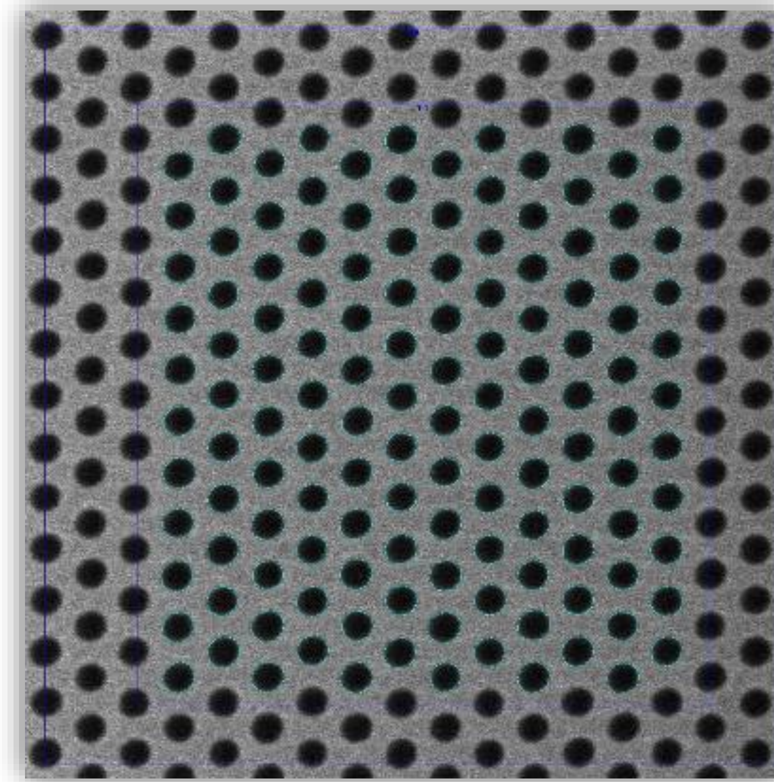
DRAM Hexagonal Arrays

EUV has trouble with dose vs LCDU trade-off for dense contact holes

EUV



DUV



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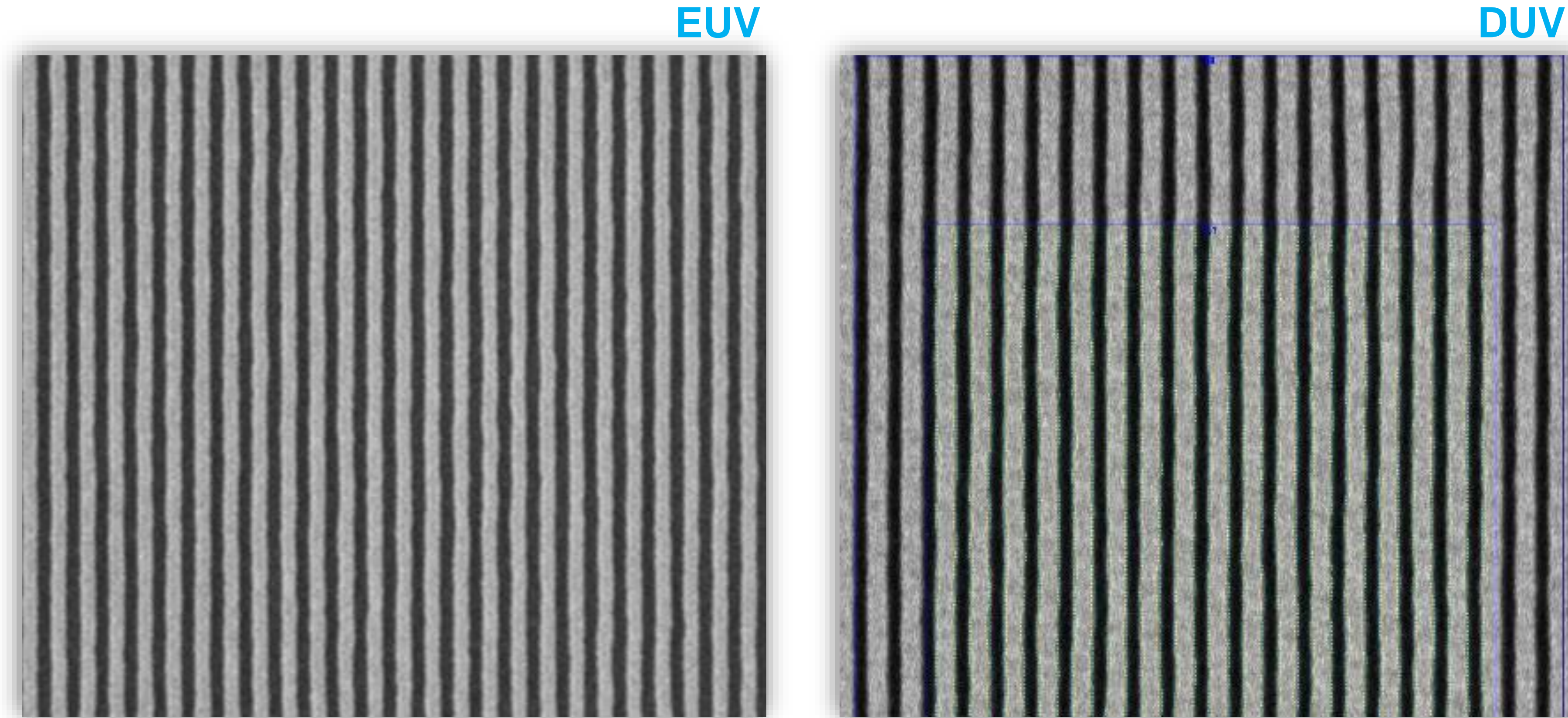
DRAM Line/Space

EUV has trouble with dose vs LWR trade-off for dense lines



Comparable pitches shown here

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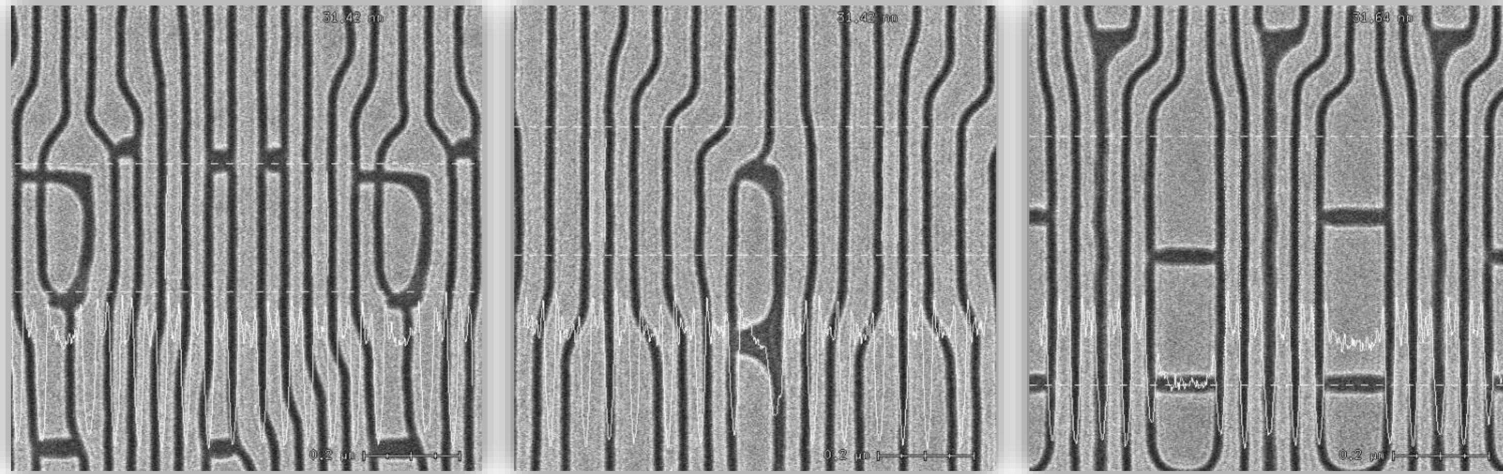
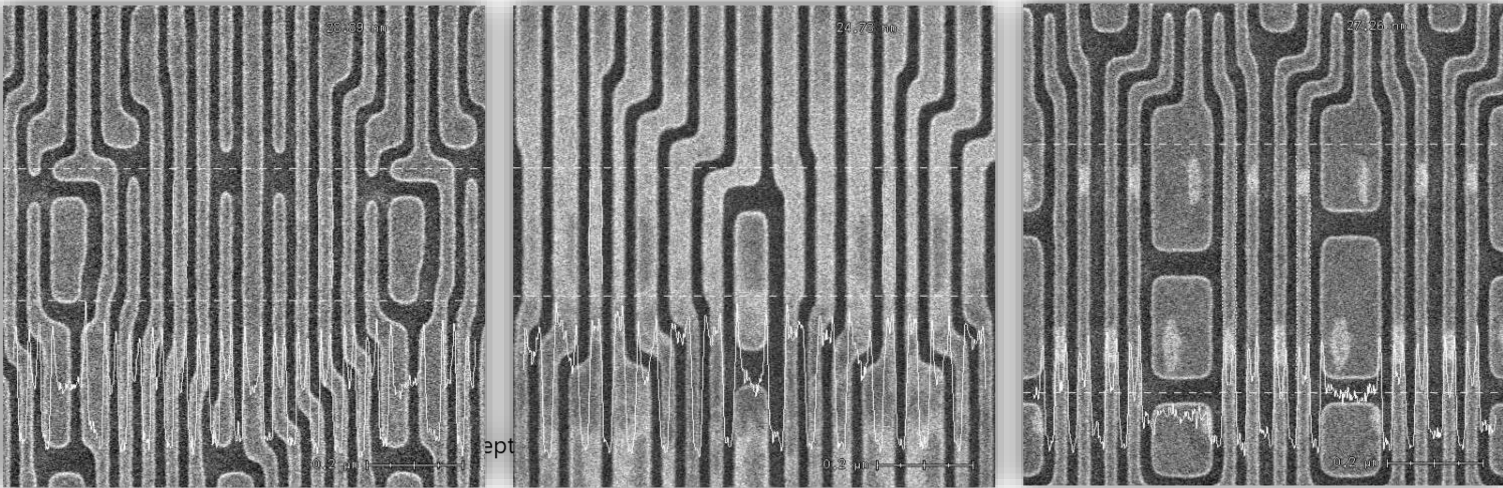
DRAM Metal 0

DUV



EUV

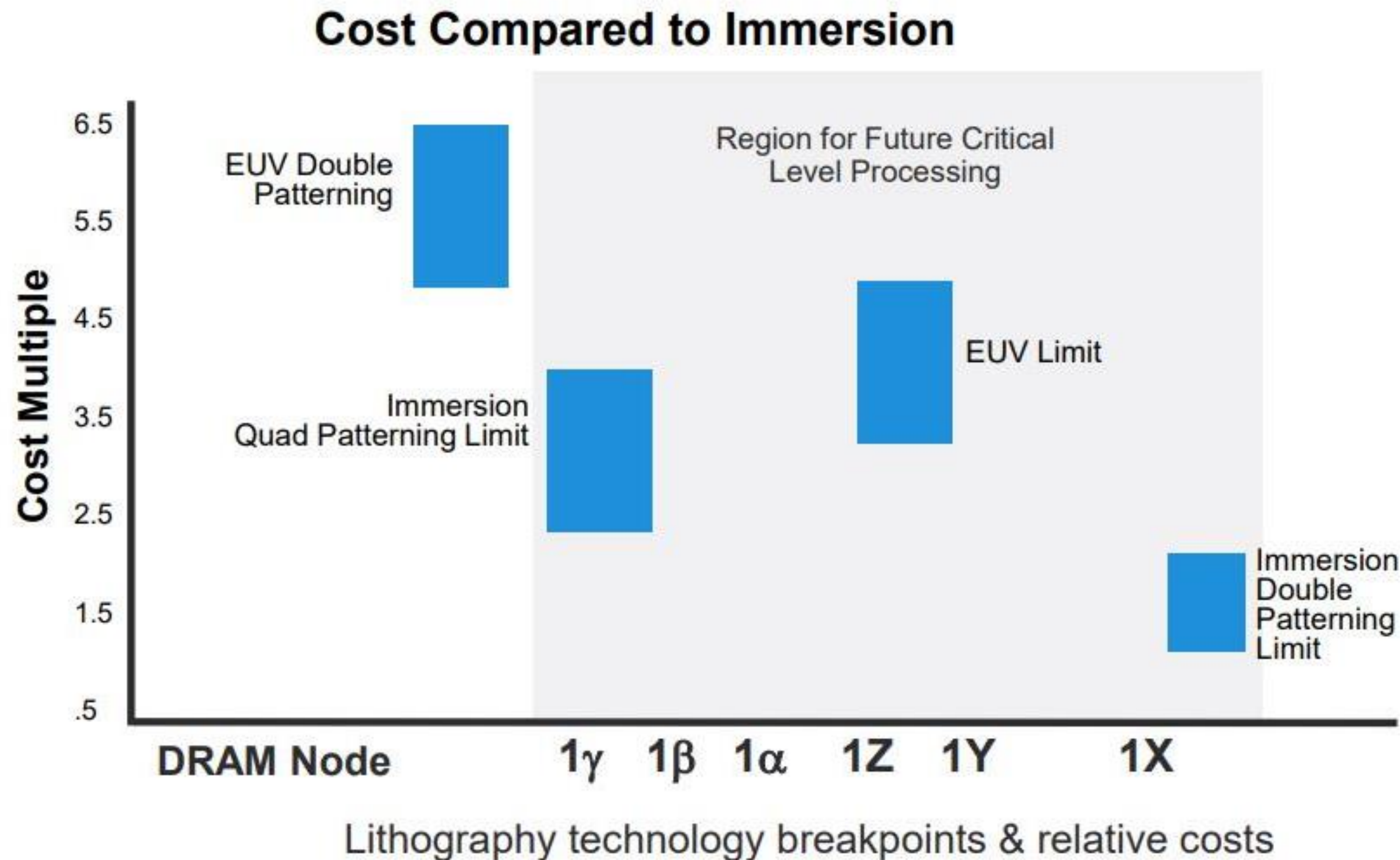


EUV does really well with 2D features especially for metal routing

Optimized Approach to Lithography

Multiple Patterning Technology Optimized for Micron Future DRAM Nodes

- Micron's pattern multiplication technology is a strategic advantage
- Proven technology capability and cost efficiency for 1Znm through 1γnm
- Ongoing evaluation of EUV Lithography for DRAM
- Prepared for implementation of EUV when beneficial to Micron



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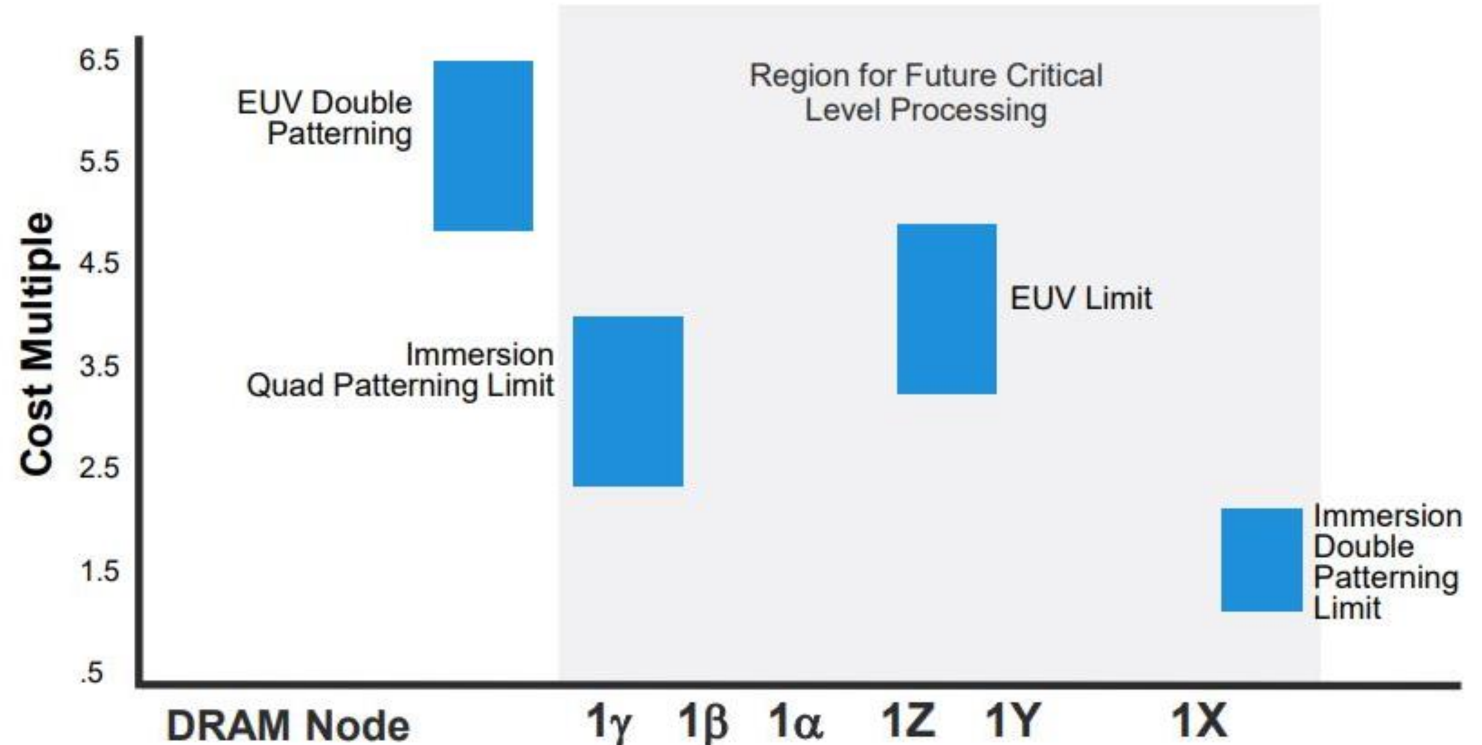
- Proven technology capability and cost efficiency for 1Znm through 1γnm
- Ongoing evaluation of EUV Lithography for DRAM
- Prepared for implementation of EUV when beneficial to Micron



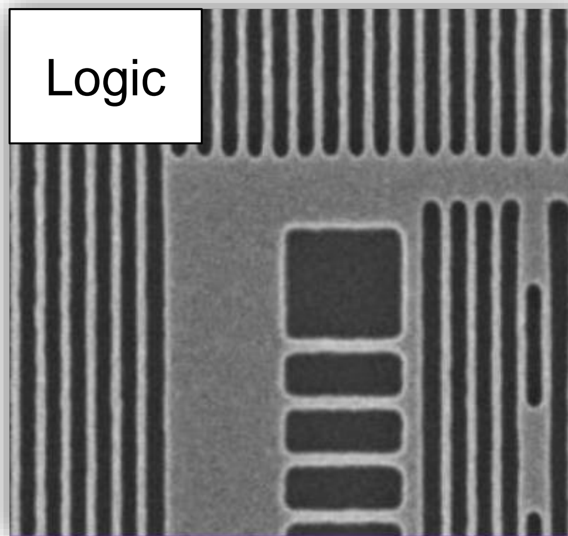
Lithography technology breakpoints & relative costs

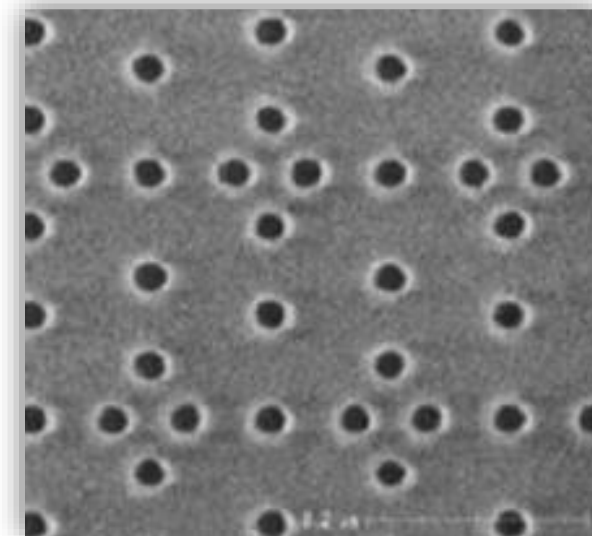
Micron

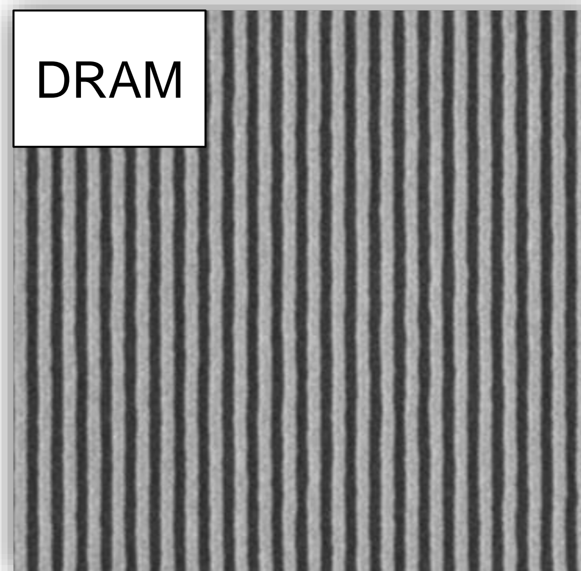
Conclusions

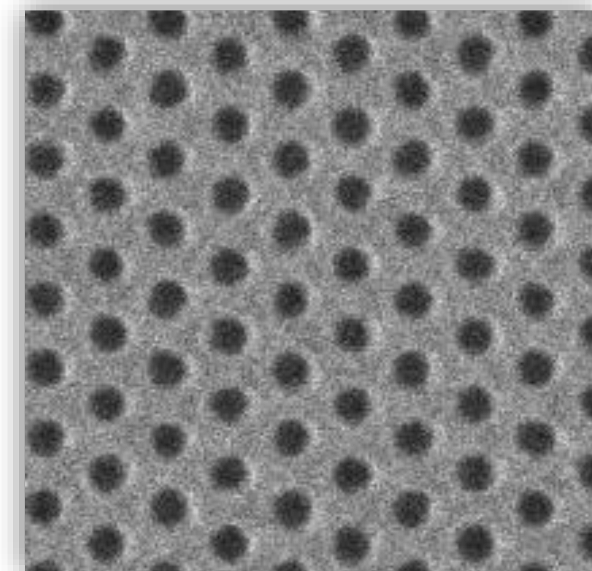
- **Logic (Random Layout) EUV Use Cases**
1. Sparse vias
2. Metal Routing
3. 2D Features
- **DRAM (Regular Layout) EUV Use Cases**
1. Metal Routing
2. Dense Pillars/Contacts

EUV ecosystem improvements for LCDU/LWR at low dose still needed to enable cost/performance tradeoff in DRAM manufacturing.





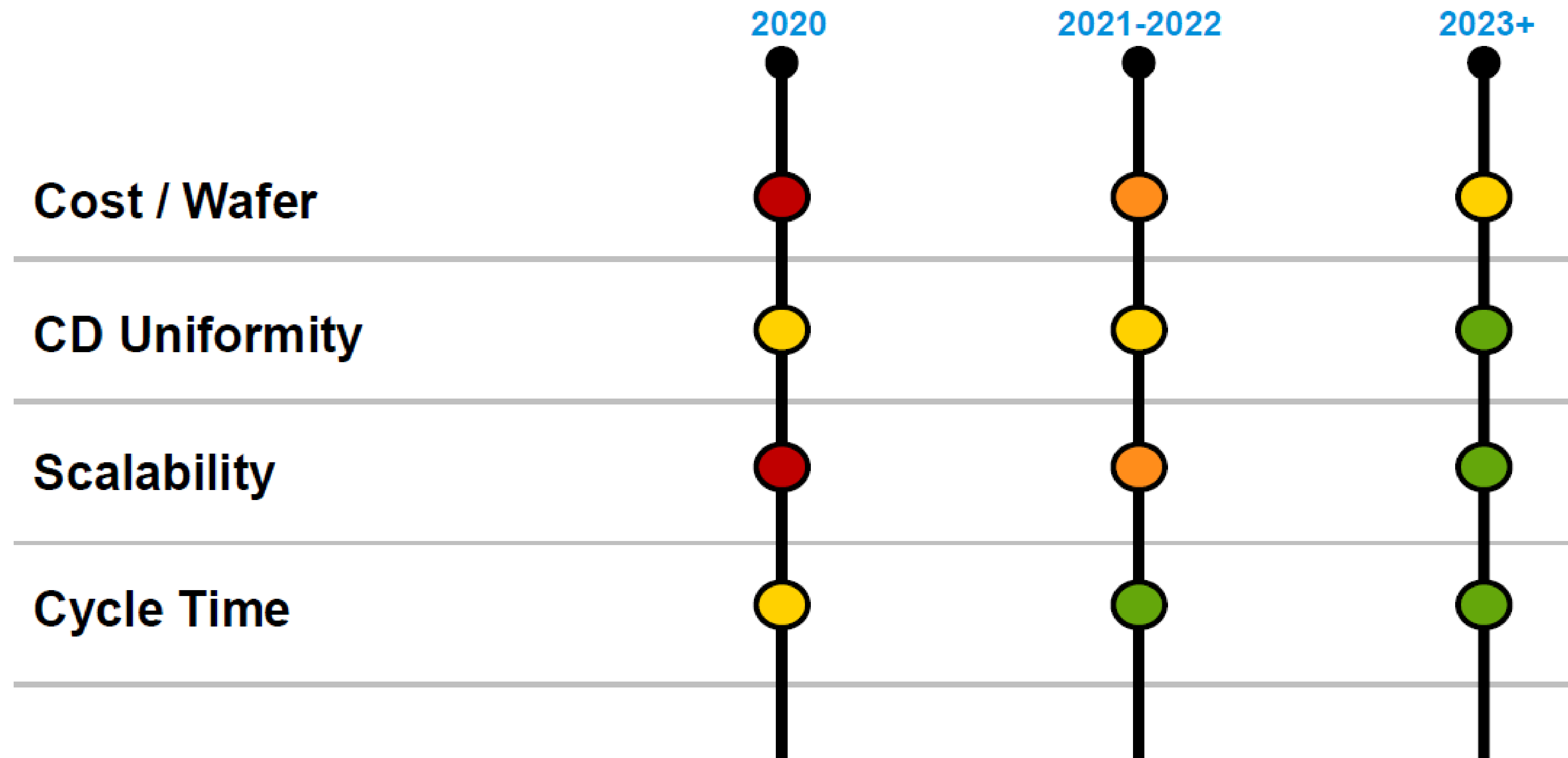




DRAM EUV Performance Improving

Potential future option for Micron DRAM lithography

DRAM EUV Capability*



*Micron Performance analysis relative to Micron DRAM requirements

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