Mask-Wafer Co-Optimization for High-NA EUV Readiness in Advanced DRAM

Vineet Vijayakrishnan Nair

Micron Semiconductor Inc., 8000 S Federal Way; Boise, ID 83707, USA

As DRAM scaling approaches angstrom-level patterning tolerances, variability budgets have become significantly tighter than in comparable logic technologies. The introduction of EUV lithography into DRAM manufacturing has already required operation near stochastic limits while sustaining high-volume throughput. The transition to High-NA EUV further exacerbates these challenges, increasing sensitivity to mask-induced variability as feature sizes and pitches continue to shrink.

High-NA EUV is under active evaluation for advanced DRAM applications, particularly for dense contact arrays at pitches beyond the practical imaging limits of low-NA EUV. Achieving acceptable local critical dimension uniformity (LCDU) and pattern placement error (PPE) is essential for assessing High-NA EUV viability. While resist-driven stochastic effects dominate wafer-level variability in low-NA EUV, mask-related contributions—typically ~20%—are expected to increase with continued scaling, positioning mask design and write strategies as critical enablers for future DRAM nodes.

Meeting High-NA EUV requirements for DRAM will therefore require a mask-centric co-optimization approach, including systematic evaluation of mask data type, mask write process correction, mask blank selection, and mask tonality. Such optimization is essential to control variability within tightening budgets and to enable a viable transition to high-volume manufacturing.

Presenting Author

Vineet earned his PhD in Materials Science & Engineering from the University of California, Irvine in 2015, where his research focused on photo-electrochemistry and device fabrication. Prior to this, he completed an MS in Materials Science & Engineering from the University of Pennsylvania, and a B.Tech in Metallurgical & Materials Engineering from the National Institute of Technology, Warangal (India).

Before joining Micron, Vineet worked as a Senior R&D Engineer at Imec (Leuven, Belgium) as part of the Advanced Patterning Center, collaborating closely with ASML on Low-NA and High-NA EUV lithography pathfinding, scanner hardware, and patterning strategies. Earlier in his career, he was a Process Development Engineer at Intel, where he contributed to 10 nm and 14 nm logic

technology development with a focus on lithography and process integration.
In his current position as SMTS at Micron Technology, Vineet has worked in advanced photo and EUV pathfinding, contributing to patterning strategies, mask lifetime characterization, new material enablement and High-NA EUV exploration. He is also an active contributor to the international lithography community, with multiple peer-reviewed publications and presentations at SPIE Advanced Lithography.